

FIG.1

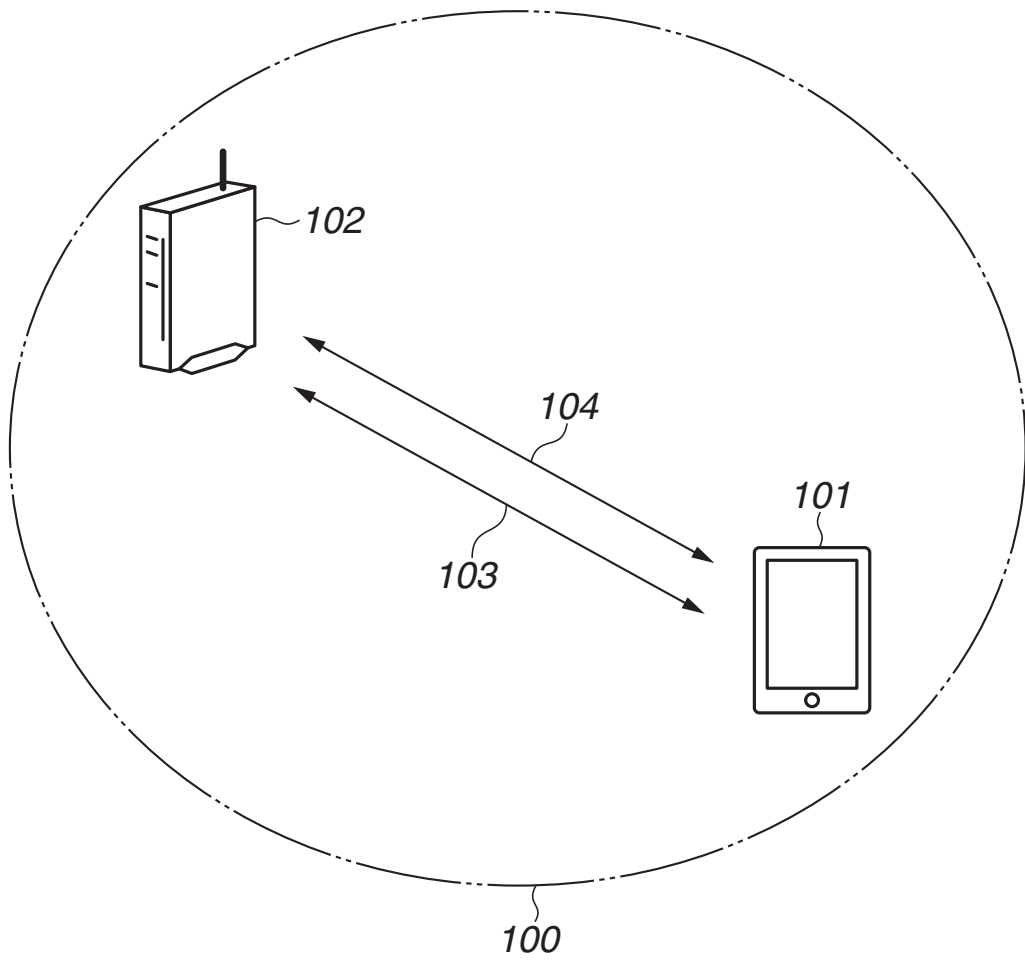


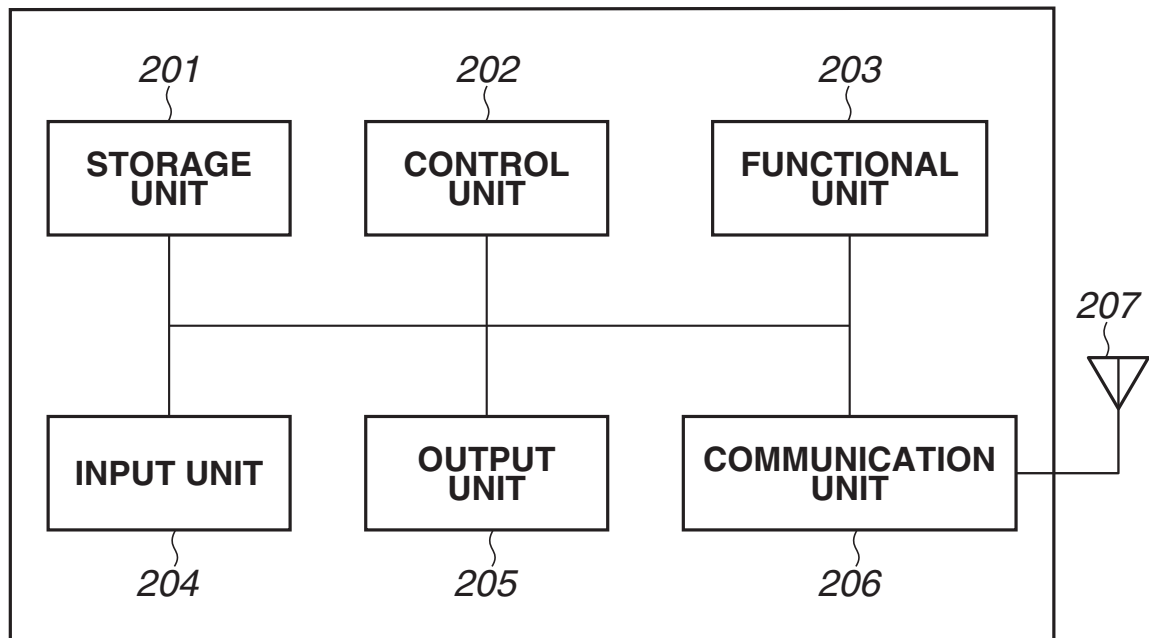
FIG.2

FIG.3

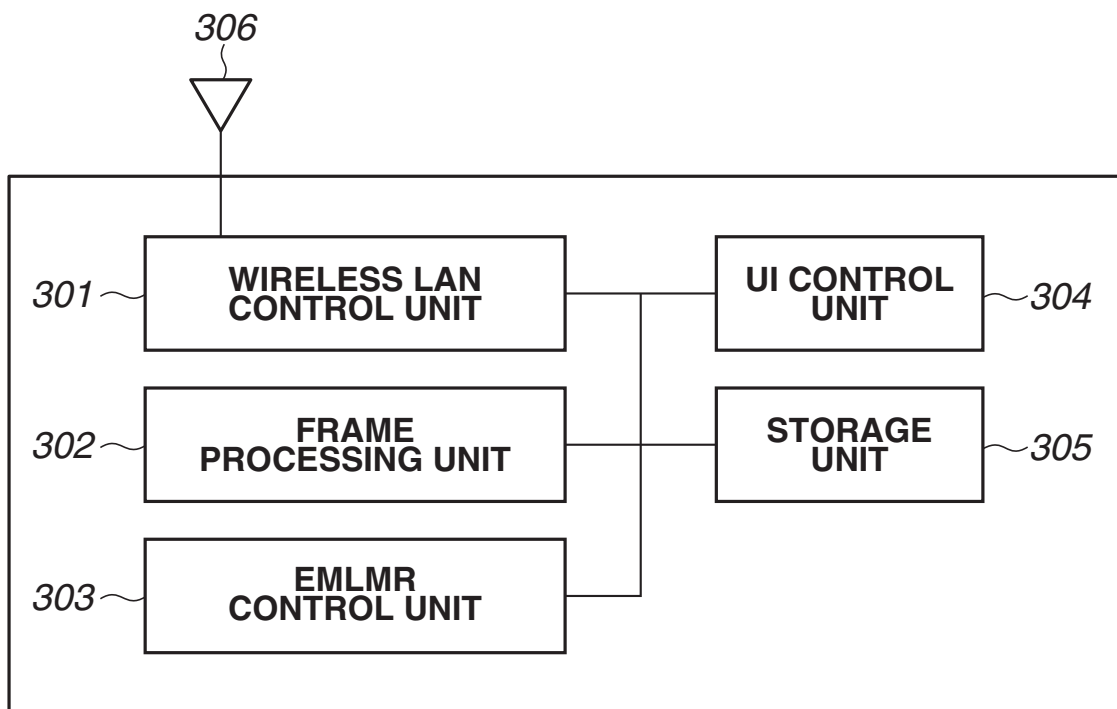


FIG.4

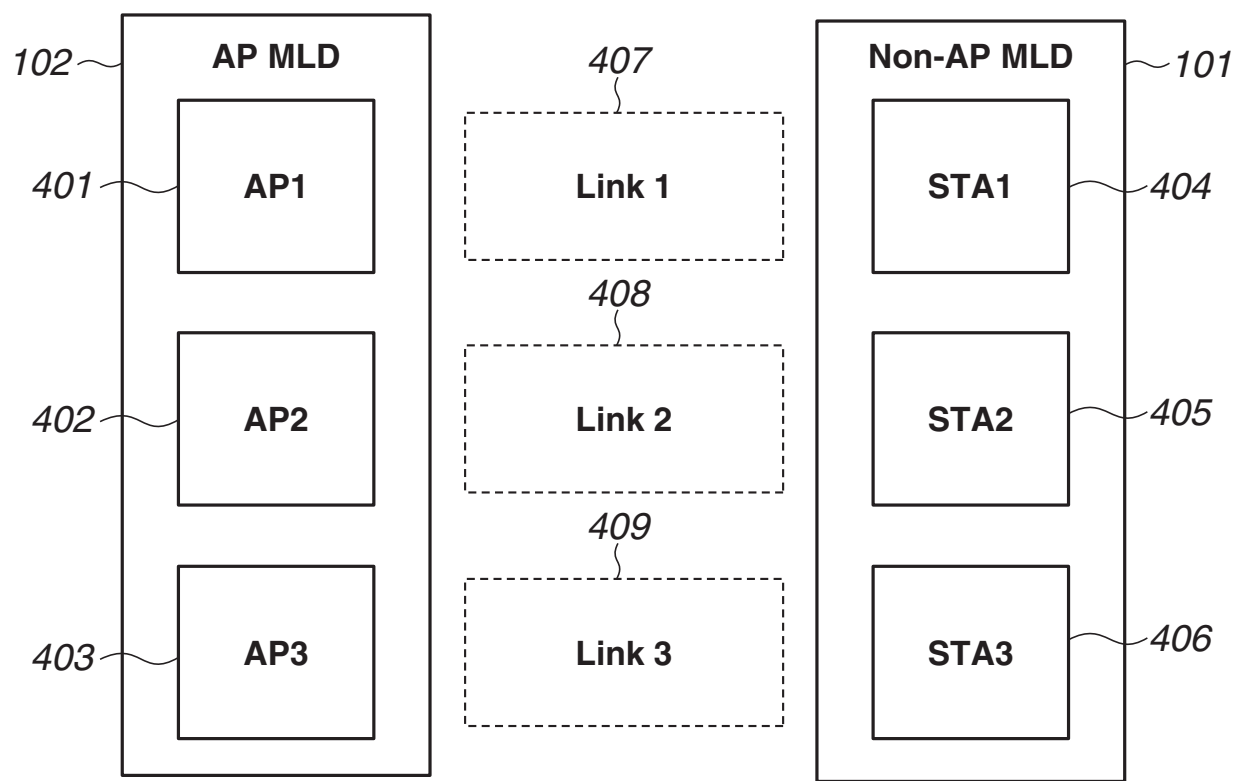


FIG. 5A

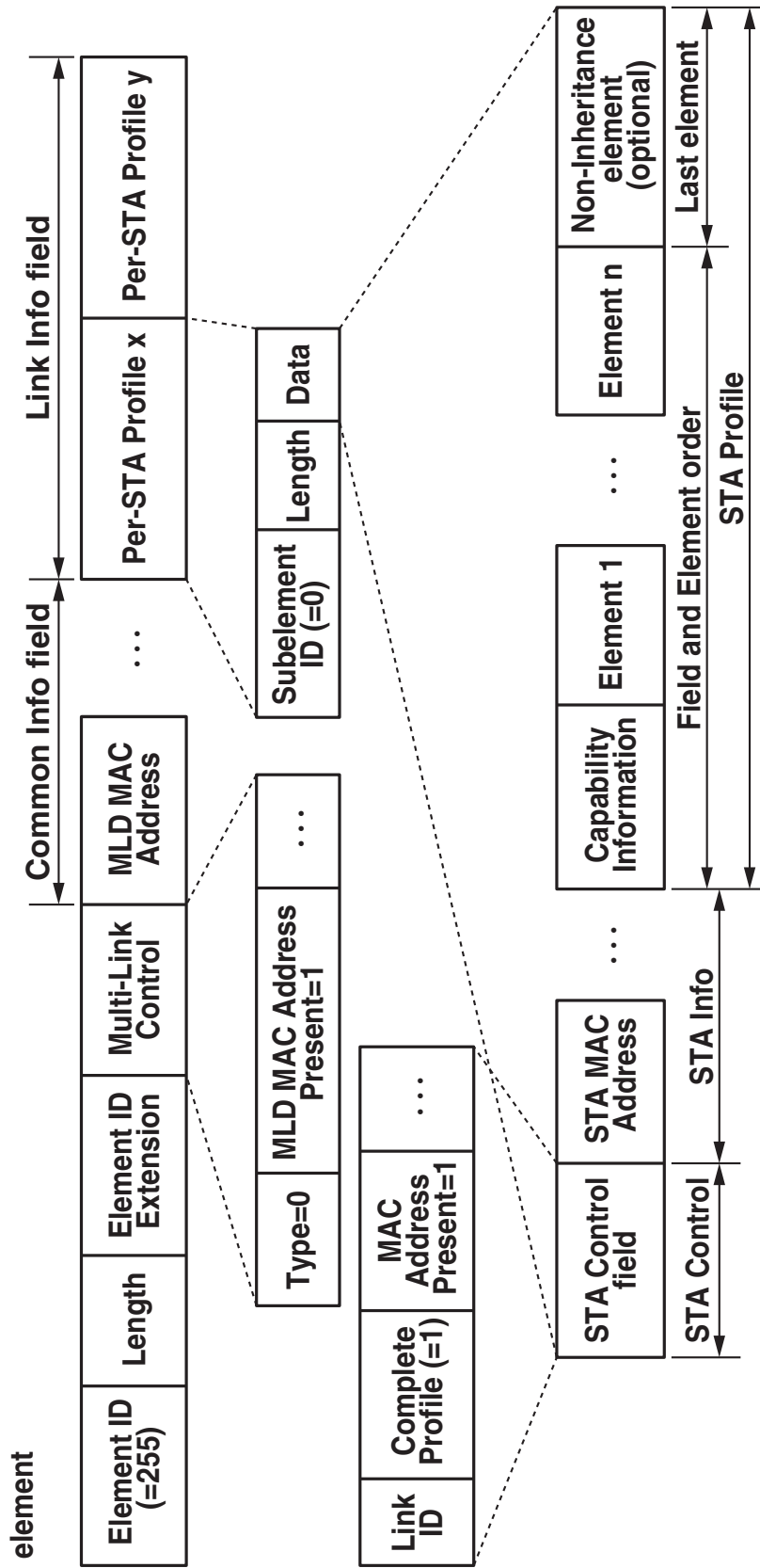


FIG. 5B

	B0	B1	B3	B4	B5	B7	B8	B11	B12	B13	B14	B15	B16	B39/63/87
	EMLSR Support	EMLSR Delay	EMLMR Support	EMLMR Delay	Transition Timeout	MCS Map Count	Reserved	EMLMR Supported MCS And NSS Set						
Bits:	1	3	1	3	4	2	2	Variable						

FIG.6A

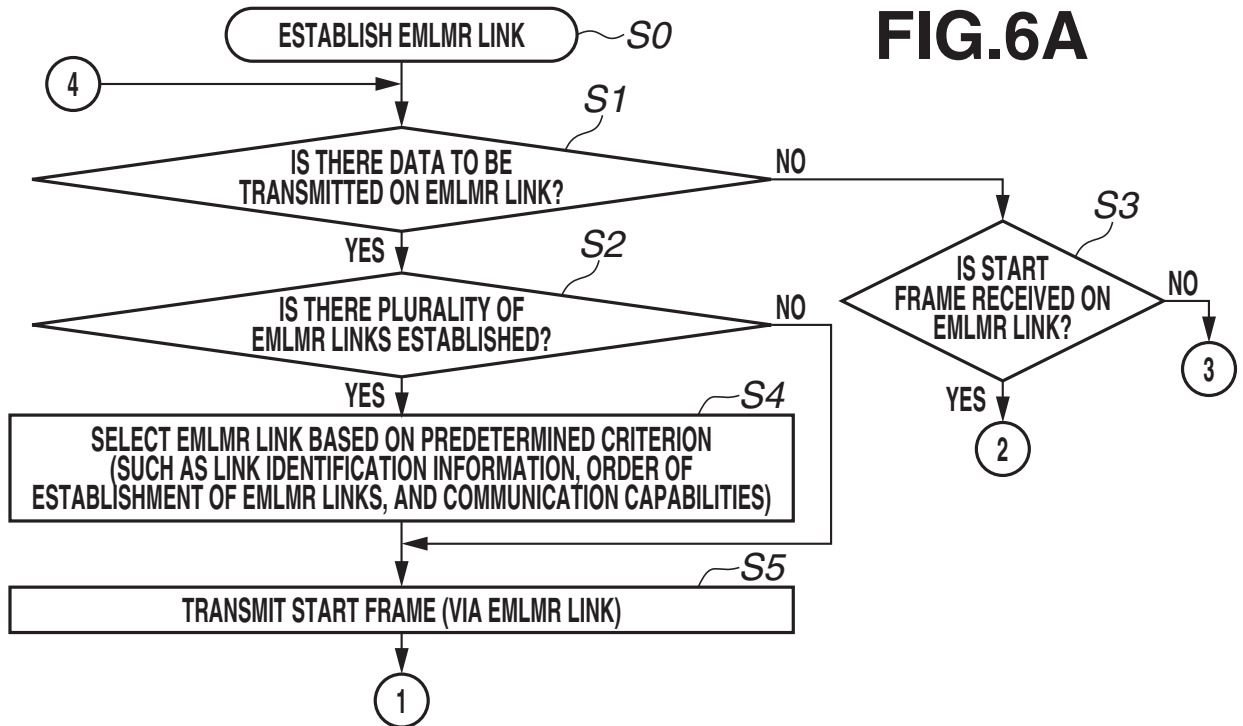


FIG.6B

