

Description

This invention relates to a digital signal clamp circuit.

The invention will be described in the environment of digital video signal processing though it is to be understood to have much wider applications.

Signals, such as television signals, have a brightness component which must be referenced to a DC value to extract its information content. However, broadcasting such a signal tends to eliminate or lose the DC value. In order to reestablish a DC reference for the brightness component, television receivers are equipped with clamp circuitry. Typically this clamp circuitry is energized during the horizontal synchronization pulse, and responsive to the amplitude of this pulse sets the DC level for the remainder of the signal. This approach has proven to be quite satisfactory for most video signal processing applications.

It will be readily recognized by those skilled in the art of video signal processing that the amplitudes of horizontal sync pulses may vary from channel to channel. A consequence of this variation is that the absolute value of the clamped DC level will change from channel to channel.

The channel to channel variation is normally of little consequence in standard receivers. However in pix-in-pix receivers, which simultaneously display images from two channels in exclusive portions of the display screen, a difference in the brightness of the two images may be annoying to certain viewers. Therefore, it is desirable to be able to clamp the DC level of at least one of the signals to a specific value. GB-A-1,583,927 discloses a system for the digital clamping of pulse code modulated video signals having one signal input for receiving a digital signal and a combining circuit having a first input coupled to said signal input, a second input, and an output for providing a clamped signal including signal samples having a polarity bit.

The present invention is specified in the claims to which attention is invited.

In an embodiment of the present invention the DC level is clamped to the blanking level of the brightness signal. The blanking level of the brightness signal immediately precedes the active portion of a standard television signal and is relatively easily sampled. The embodiment includes a digital clamp circuit including an up/down counter, an adder and circuitry for enabling the up/down counter during a predetermined interval of a digital signal to be clamped. The adder has a first input port coupled to receive the signal to be clamped and a second input port coupled to a count value output from the counter. During intervals that the counter is enabled it is conditioned to count up or down by the polarity bit of the sum signal provided by the adder. In one embodiment the direction of counting is selected to drive the output of the

adder toward zero. Ultimately, the output of the counter that is applied to the adder will equal the negative of the value exhibited by the signal during the interval that the counter is enabled. This value is applied to the adder during the remainder of the signal, thereby establishing the DC value of the signal.

FIGURE 1 is a waveform drawing of a portion of a video signal useful in describing the invention.

FIGURE 2 is a block diagram of an exemplary digital clamp circuit embodying the invention.

The upper waveform shown in FIGURE 1 depicts one horizontal interval of a typical baseband composite video signal. The signal includes a horizontal synchronizing component, a blanking level, a burst component, and a video information component corresponding to one line of the displayed image. In the NTSC standard the blanking level is established at zero IRE units; the tip of the horizontal synchronizing component is established at minus 40 IRE units; the burst component swings between plus and minus 20 IRE units; and the peak of the information component is limited to 100 IRE units. The blanking level may be detected in the horizontal interval between the burst component and the information component of the video signal.

Color television receivers include circuitry for generating a burst gate signal, BG, which occurs during the burst interval and is utilized in detecting the burst signal. A sampling signal, EN, which occurs during the blanking level may readily be derived from a delayed burst gate signal BG_D, as will be discussed hereinafter.

In receivers which include digital signal processing apparatus, the received analog video signal is typically demodulated to baseband and clamped to the sync tip value. This signal is applied to the analog input terminal of an analog-to-digital converter ADC. The ADC, responsive to a system clock signal F_c converts the signal to pulse code modulated, PCM samples (e.g., binary samples) occurring at a sample rate equal to the frequency of the clock signal F_c.

In the following discussion it is assumed that the analog video signal is converted to 8-bit, two's complement, PCM samples. In this instance the range of sample values extends from minus 128 to plus 127 inclusive (decimal). The negative limit of -128 units corresponds to minus 40 IRE or sync tip; the positive limit of +128 units corresponds to 100 IRE; and zero corresponds to 30 IRE. The blanking level corresponds to a value of approximately minus 55 units, for an uncorrupted signal. However, whether or not the sync tip is greater or lesser than minus 40 IRE, the blanking level will be represented by a negative PCM number.

Keeping these conditions in mind refer to FIGURE 2. In FIGURE 2 the broad arrows represent multibit parallel busses. A number adjacent a slash through a bus indicates the number of parallel con-

nections in the bus.

An analog video signal is coupled to an ADC 36 which converts the signal to 8-bit two's complement PCM samples as described above. These samples are applied to a lowpass filter 34 which attenuates the burst component so that the blanking level extends from the horizontal synchronizing pulse to the start of the video information component. Output samples from the lowpass filter are coupled to element 32 which adds an extra bit to the samples by replicating the sign bit. That is, the input to element 32 are 8-bit samples with the most significant bit being the sign bit. The output from element 32 are nine bit samples with the two most significant bits corresponding to the sign bit of the input samples. Output samples from element 32 are coupled to one input port of a 9-bit adder 28. (Note the 8-bit samples from filter 34 are extended to 9-bits and a 9-bit adder is utilized in this arrangement to prevent the sum from the adder from being limited by the capacity of the adder, i.e., to preclude fold over.)

The output samples provided by the adder 28 are coupled to the data input port of a D-type latch 30. Latch 30 responsive to the system clock Fc delays the samples from adder 28 by one sample period. Output samples OUT from latch 30 represent the clamped video output signal.

A value of magnitude equal to the blanking level but of opposite polarity is coupled to a second input port of the adder 28. This value is generated by an $n+m+1$ bit up/down counter 18. The up/down control of the counter 18 is responsive to the sign or most-significant-bit of the output signal OUT. If the output signal is negative (positive), the counter is conditioned to count up (down). The sign bit applied to the up/down control input of the counter is taken from the output of the latch 30 to insure that it is stable for the sampling period. Assume that the counter is enabled to count for one sample period during the blanking interval each line time. If during a sequence of horizontal line intervals the output signal is negative during the blanking interval, indicating that the value provided to the adder by the counter is less in magnitude than the blanking value applied to the other input port of adder 28, the counter will be conditioned to increment by one unit each line interval until the output signal is positive. Conversely if the output signal is positive during the blanking interval, the counter will be conditioned to decrement by one unit each line interval. Conceptually, once the magnitude of the value provided by the counter equals the magnitude of the blanking level, the counter will alternately increment and decrement by one unit on successive horizontal lines.

Since the counter is only enabled to increment/decrement during the blanking interval, the value provided to the adder 28 by the counter 18 does not change during the remainder of the horizontal in-

terval. Thus, if the value provided by counter 18 is equal to A and the value of the signal samples provided by element 32 is S the value of the output samples will equal $S + A$.

The counter 18 is indicated as being an $n+m+1$ bit counter. The number represented by $n+m+1$ (where n and m are integers) may equal the number of bits per sample provided by the ADC 36. However, this is undesirable for two reasons. First, the count value will be susceptible to noise attendant the blanking signal and the counter may provide erroneous values to the adder 28. Second, from horizontal line-to-horizontal line the count value will alternate up and down by one unit. To preclude both of these conditions the counter is provided with excess bit capacity over the bits provided by the ADC. The lesser significant bits of the counter are truncated, and only the more significant bits from the counter are applied to the adder. This truncation effectuates a division of the count value which in turn tends to effectuate a low pass function to the measured values. Since the counter increments/ decrements by one unit, and K bits of the counter are truncated, the output value applied to the adder may only change every 2^{K-1} line intervals depending on the direction of signal changes. During these 2^{K-1} line intervals, if the blanking level is contaminated by noise only during a few of these intervals the output count value may not change at all since during successive lines the counter has the opportunity to self correct.

In FIGURE 2 the lesser significant counter output bits 0 to n are truncated and only the more significant bits $n+1$ to $n+m$ are coupled to the adder. The number m of more significant bits must be at least large enough to represent the value of the signal level to be clamped. In the example indicated by FIGURE 1 the number m of bits must be at least 6 to represent the magnitude 55 of the blanking level. To the m most significant bits from the counter 18, R zero valued bits are concatenated to the most significant bit positions. The number R is selected so that the sum of bits $m+R$ is equal to the number of sample bits provided by element 32 which is equal to the input bit capacity of the adder. (The R bits are assigned zero value because the system was assumed to be operating with two's complement samples and the counter is assumed to be providing unsigned magnitude values.)

Another feature of the FIGURE 2 clamp arrangement is that the blanking or clamp level measurement is performed using the truncated output from the counter but a rounded value from the counter is added to the remaining signal. This feature is implemented via an AND circuit 26. The most significant bit (n) of the truncated bits not applied to the adder is coupled to one input terminal of the AND circuit 26. A twice delayed and inverted burst gate signal BG_{DD} developed in D-type latches 12, 13 and 15 is coupled to a second input terminal of the AND circuit 26. The

delayed and inverted burst gate signal enables the AND circuit 26 to pass the n^{th} truncated bit during the active video intervals and disables the AND circuit during the measurement portion of the blanking interval. The output signal from the AND circuit 26 is coupled to the carry input (CI) terminal of the adder 28. This adds a half unit (when present) to the counter output provided to the adder to effectuate rounding and improve the clamp level accuracy.

The enable signal for the counter is developed by the D-type latches 12 and 14 and the AND circuit 16. A burst gate signal such as the signal BG illustrated in FIGURE 1 is applied to the data input terminal 10 of latch 12 wherein it is delayed one clock period. The Q output of latch 12 is coupled to the data input of latch 14 wherein it is delayed a second clock period. The inverted output $\bar{Q}$ of latch 12 and the output Q of latch 14 are applied to respective input terminals of the AND circuit 16 which produces an enable signal EN which is one clock period wide as illustrated in FIGURE 1. The clock signal Fc which controls the latches 12 and 14 is also coupled to the clock input of counter 18. The clock signal conditions the counter to increment/decrement by one unit when the enable signal is high. Note, if desired, the enable pulse can be made several pulses wide enabling the counter to perform several successive measurements during a particular blanking interval.

In the foregoing discussion it has been assumed that the counter output values are coupled directly to the adder 28 and AND circuit 26. The system described is operable with these connections because the counter values are always positive valued and the blanking levels are always negative valued. However, in a more generalized system where the input signal clamping value is also positive valued the counter values must be inverted in polarity or complemented. This may be accomplished by including a complementing circuit 24 in the counter output signal paths. In this instance the sign bit coupled to the up/down control terminal must also be inverted. In an alternative arrangement the more significant R bits concatenated to the counter bits may be constrained to be one valued rather than zero valued which produces negative output values. In a still further alternative a subtractor circuit may be substituted for the adder circuit 28. Since in the general case either an adder circuit or a subtractor circuit may be implemented for adder 28, in the claims the generic term "combining circuit" will be used to describe this element.

Finally, regarding the counter 18, it is desirable that it be designed such that its output count does not fold over once it reaches its maximum or minimum count value. That is, if its count value is represented by all ones (all zeroes), a further increment (decrement) command will not produce a count value of all zeroes (all ones), but will retain an output of all ones (all zeroes).

Claims

1. A digital clamp circuit comprising:
 - a signal input port for applying a digital signal having periodically recurring reference intervals;
 - a combining circuit (28) having a first input port coupled to said signal input port, having a second input port and having an output port for providing a clamped signal output including signal samples having a polarity bit; characterized by:
 - an up/down counter (18) having an up/down control input coupled to receive said polarity bit and having a count value output port;
 - means (20) for coupling said count value output port to the second input port of said combining circuit; and
 - means (16) for enabling said up/down counter to increment/decrement once only during each of said predetermined reference intervals of said input signal.
2. The digital clamp circuit set forth in claim 1 further characterized in that said up/down counter (18) is arranged to provide count values up to a count value equal to 2^{n+m} , which values are represented by bits 0, 1, 2, ..., n, n+1, ..., n+m (m and n are integers greater than 0), where bit 0 is the least significant bit and bit m+n is the most significant bit, and in that the means (20) for coupling said count value output port to said combining circuit (28) couples only the m more significant bits representing the count values to the combining circuit (28).
3. The digital clamp circuit set forth in claim 2 further characterized in that said combining circuit (28) further includes a carry input terminal and in that said digital clamp circuit further includes:
 - a gating circuit (26) for coupling said n^{th} bit of said count value to said carry input terminal, wherein said gating circuit is conditioned to pass values represented by said n^{th} bit of said count value during signal intervals exclusive of said predetermined reference intervals.
4. The digital clamp circuit set forth in claim 1 further characterized in that said coupling means (20) includes means for providing truncated count values to said combining circuit (28) during said predetermined reference intervals and for providing truncated and rounded count values during intervals exclusive of said predetermined reference intervals.



delayed and inverted burst gate signal enables the AND circuit 26 to pass the n^{th} truncated bit during the active video intervals and disables the AND circuit during the measurement portion of the blanking interval. The output signal from the AND circuit 26 is coupled to the carry input (CI) terminal of the adder 28. This adds a half unit (when present) to the counter output provided to the adder to effectuate rounding and improve the clamp level accuracy.

The enable signal for the counter is developed by the D-type latches 12 and 14 and the AND circuit 16. A burst gate signal such as the signal BG illustrated in FIGURE 1 is applied to the data input terminal 10 of latch 12 wherein it is delayed one clock period. The Q output of latch 12 is coupled to the data input of latch 14 wherein it is delayed a second clock period. The inverted output $\bar{Q}$ of latch 12 and the output Q of latch 14 are applied to respective input terminals of the AND circuit 16 which produces an enable signal EN which is one clock period wide as illustrated in FIGURE 1. The clock signal Fc which controls the latches 12 and 14 is also coupled to the clock input of counter 18. The clock signal conditions the counter to increment/decrement by one unit when the enable signal is high. Note, if desired, the enable pulse can be made several pulses wide enabling the counter to perform several successive measurements during a particular blanking interval.

In the foregoing discussion it has been assumed that the counter output values are coupled directly to the adder 28 and AND circuit 26. The system described is operable with these connections because the counter values are always positive valued and the blanking levels are always negative valued. However, in a more generalized system where the input signal clamping value is also positive valued the counter values must be inverted in polarity or complemented. This may be accomplished by including a complementing circuit 24 in the counter output signal paths. In this instance the sign bit coupled to the up/down control terminal must also be inverted. In an alternative arrangement the more significant R bits concatenated to the counter bits may be constrained to be one valued rather than zero valued which produces negative output values. In a still further alternative a subtractor circuit may be substituted for the adder circuit 28. Since in the general case either an adder circuit or a subtractor circuit may be implemented for adder 28, in the claims the generic term "combining circuit" will be used to describe this element.

Finally, regarding the counter 18, it is desirable that it be designed such that its output count does not fold over once it reaches its maximum or minimum count value. That is, if its count value is represented by all ones (all zeroes), a further increment (decrement) command will not produce a count value of all zeroes (all ones), but will retain an output of all ones (all zeroes).

Claims

1. A digital clamp circuit comprising:
 - a signal input port for applying a digital signal having periodically recurring reference intervals;
 - a combining circuit (28) having a first input port coupled to said signal input port, having a second input port and having an output port for providing a clamped signal output including signal samples having a polarity bit; characterized by:
 - an up/down counter (18) having an up/down control input coupled to receive said polarity bit and having a count value output port;
 - means (20) for coupling said count value output port to the second input port of said combining circuit; and
 - means (16) for enabling said up/down counter to increment/decrement once only during each of said predetermined reference intervals of said input signal.
2. The digital clamp circuit set forth in claim 1 further characterized in that said up/down counter (18) is arranged to provide count values up to a count value equal to 2^{n+m} , which values are represented by bits 0, 1, 2, ..., n, n+1, ..., n+m (m and n are integers greater than 0), where bit 0 is the least significant bit and bit m+n is the most significant bit, and in that the means (20) for coupling said count value output port to said combining circuit (28) couples only the m more significant bits representing the count values to the combining circuit (28).
3. The digital clamp circuit set forth in claim 2 further characterized in that said combining circuit (28) further includes a carry input terminal and in that said digital clamp circuit further includes:
 - a gating circuit (26) for coupling said n^{th} bit of said count value to said carry input terminal, wherein said gating circuit is conditioned to pass values represented by said n^{th} bit of said count value during signal intervals exclusive of said predetermined reference intervals.
4. The digital clamp circuit set forth in claim 1 further characterized in that said coupling means (20) includes means for providing truncated count values to said combining circuit (28) during said predetermined reference intervals and for providing truncated and rounded count values during intervals exclusive of said predetermined reference intervals.



Patentansprüche

1. Digital-Klemmschaltung, enthaltend:

- einen Signal-Eingangsport zum Zuführen eines Digital- Signals mit periodisch wiederkehrenden Reverenz-Intervallen; 5
- eine Kombinierschaltung (28) mit einem ersten Eingangsport, der mit dem Signal-Eingangsport gekoppelt ist, mit einem zweiten Eingangsport und mit einem Ausgangsport zum Bereitstellen eines geklemmten (clamped) Ausgangs-Signals, das Signal-Abtastwerte mit einem Polaritäts-Bit enthält; gekennzeichnet durch 10
- einen Aufwärts/Abwärts-Zähler (18) mit einem Aufwärts/Abwärts-Steuereingang, der zum Erhalt des Polaritäts-Bits gekoppelt ist, und mit einem Zählstand-Ausgangsport; 15
- Mittel (20) zum Koppeln des Zählstand-Ausgangsports an den zweiten Eingangsport der Kombinierschaltung; und 20
- Mittel (16) zur Freigabe des Aufwärts/Abwärts-Zählers um nur einmal während jeder der vorbestimmten Referenz-Intervalle des Eingangs-Signals zu inkrementieren / dekrementieren. 25

2. Digital-Klemmschaltung nach Anspruch 1, dadurch gekennzeichnet, 30
- daß der Aufwärts/Abwärts-Zähler (18) so aufgebaut ist, daß er Zählstände bis zu einem Zählstand 2^{n+m} bereitstellt, welche Zählstände durch Bits 0, 1, 2, ..., n, n+1, ..., n+m repräsentiert sind (n und m sind ganze Zahlen größer als Null), wobei Bit 0 das 35
- geringstwertigste Bit und Bit m+n das höchstwertigste Bit ist, und daß das Mittel (20) zum Koppeln des Zählstand-Ausgangsports an die Kombinierschaltung (28) nur die die Zählstände repräsentierenden m signifikanteren Bits an die Kombinierschaltung (28) koppelt. 40

3. Digital-Klemmschaltung nach Anspruch 2, weiter dadurch gekennzeichnet, 45
- daß die Kombinierschaltung (28) weiter einen Übertrags-Eingangsanschluß beinhaltet und daß die Digital-Klemmschaltung weiter beinhaltet:
- eine Torschaltung (26) zum Koppeln des n-ten Bits des Zählstandes an den Übertrags-Eingangsanschluß, wobei die Torschaltung konditioniert wird, während Signal-Intervallen mit Ausnahme der vorbestimmten Referenz-Intervalle durch das n-te Bit des Zählstandes repräsentierte 50
- Werte durchzulassen. 55

4. Digital-Klemmschaltung nach Anspruch 1, weiter dadurch gekennzeichnet,

daß das Kopplungsmittel (20) Mittel beinhaltet, um der Kombinierschaltung (28) während der vorbestimmten Referenz-Intervalle verkürzte (abgeschnittene) Zählstände zur Verfügung zu stellen und um während Intervallen mit Ausnahme der vorbestimmten Referenz-Intervalle verkürzte und gerundete Zählstände zur Verfügung zu stellen.

Revendications

1. Circuit de verrouillage numérique comprenant :

- un point d'accès d'entrée de signal pour appliquer un signal numérique présentant des intervalles de référence périodiquement récurrent ;
- un circuit de combinaison (28) ayant un premier point d'accès d'entrée couplé audit point d'accès d'entrée de signal, ayant un second point d'accès d'entrée et ayant un point d'accès de sortie pour délivrer une sortie de signal verrouillé incluant des échantillons de signal ayant un bit de polarité, caractérisé par :
- un compteur/décompteur (18) ayant une entrée de commande de comptage/décomptage couplée de manière à recevoir ledit bit de polarité et ayant un point d'accès de sortie de la valeur du compte ;
- des moyens (20) pour coupler ledit point d'accès de sortie de valeur de compte audit second point d'accès d'entrée dudit circuit de combinaison ; et
- des moyens (16) permettant au compteur/décompteur d'incrémenter/décrémenter seulement pendant chacun des intervalles de référence déterminés dudit signal d'entrée.

2. Circuit de verrouillage numérique selon la revendication 1, caractérisé en outre en ce que le compteur/décompteur (18) est disposé de manière à fournir des valeurs de compte allant jusqu'à une valeur de compte égale à 2^{n+m} , lesquelles valeurs sont représentées par des bits 0, 1, 2... n, n+1, ...n+m (m et n étant des nombres entiers supérieurs à 0), où le bit 0 est le bit le moins significatif et le bit m+n est le plus significatif, et en ce que les moyens (20) pour coupler ledit point d'accès de sortie de valeur de compte audit circuit de combinaison (28) ne couplent que les bits les plus significatifs m, représentant les valeurs de compte pour le circuit de combinaison (28).

3. Circuit de verrouillage numérique selon la revendication 2, caractérisé en outre en ce que ledit circuit de combinaison (28) comprend en outre une



borne d'entrée de report et en ce que ledit circuit de verrouillage numérique comprend en outre :

- un circuit de déclenchement (26) pour coupler ledit nième bit de ladite valeur de compte à ladite borne d'entrée de report, dans lequel ledit circuit de déclenchement est conditionné de manière à faire passer des valeurs représentées par ledit nième bit de ladite valeur de compte pendant des intervalles de signaux exclusifs desdits intervalles de référence prédéterminés.

4. Circuit de verrouillage numérique selon la revendication 1, caractérisé en outre en ce que lesdits moyens de couplage (20) comprennent des moyens pour fournir des valeurs de compte tronquées audit circuit de combinaison (28) pendant lesdits intervalles de référence prédéterminés et pour fournir des valeurs de compte tronquées et arrondies pendant des intervalles exclusifs desdits intervalles de référence prédéterminés.

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