

A B S T R A C T

A memory device controlling method according to one
embodiment is receiving, by a first semiconductor memory, a
read command transmitted from a controller; receiving, by a
5 second semiconductor memory, a write command transmitted
from the controller; reading, from the first semiconductor
memory, data based on the read command, and transmitting,
by the first semiconductor memory, the data and a control
signal indicating that the data is output; and receiving,
10 by the second semiconductor memory, the data based on the
write command at a timing based on the control signal, and
writing the received data into the second semiconductor
memory.