

FIG. 1

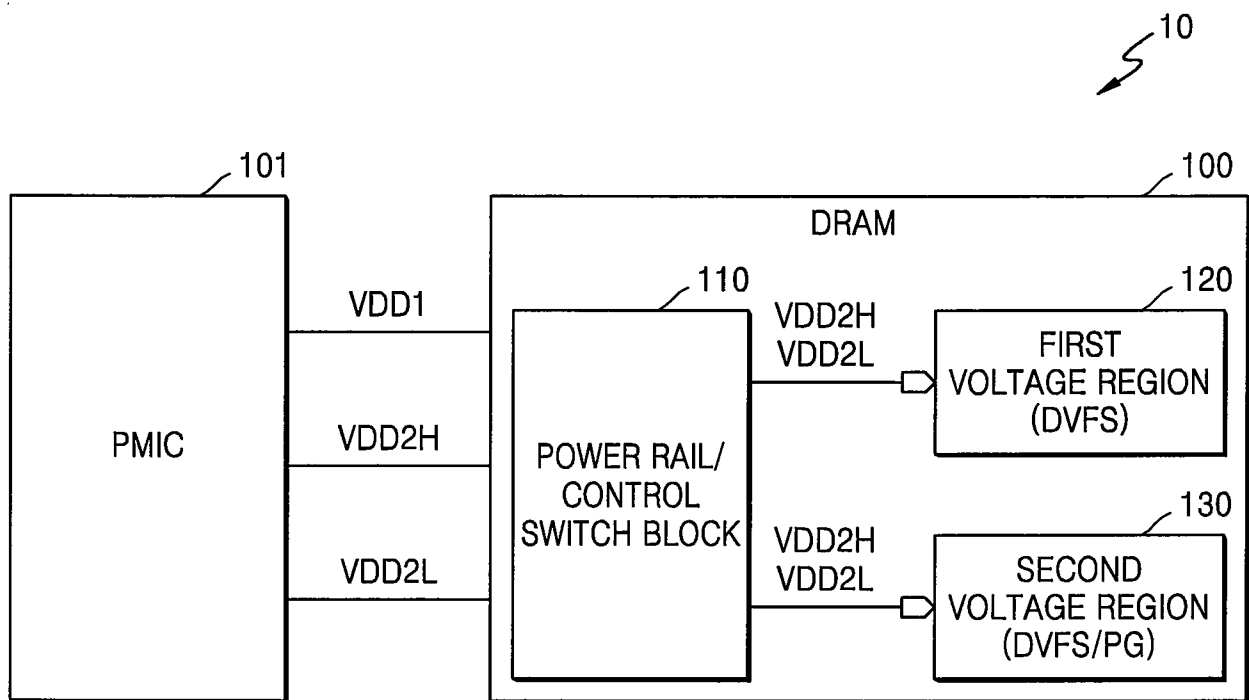


FIG. 2

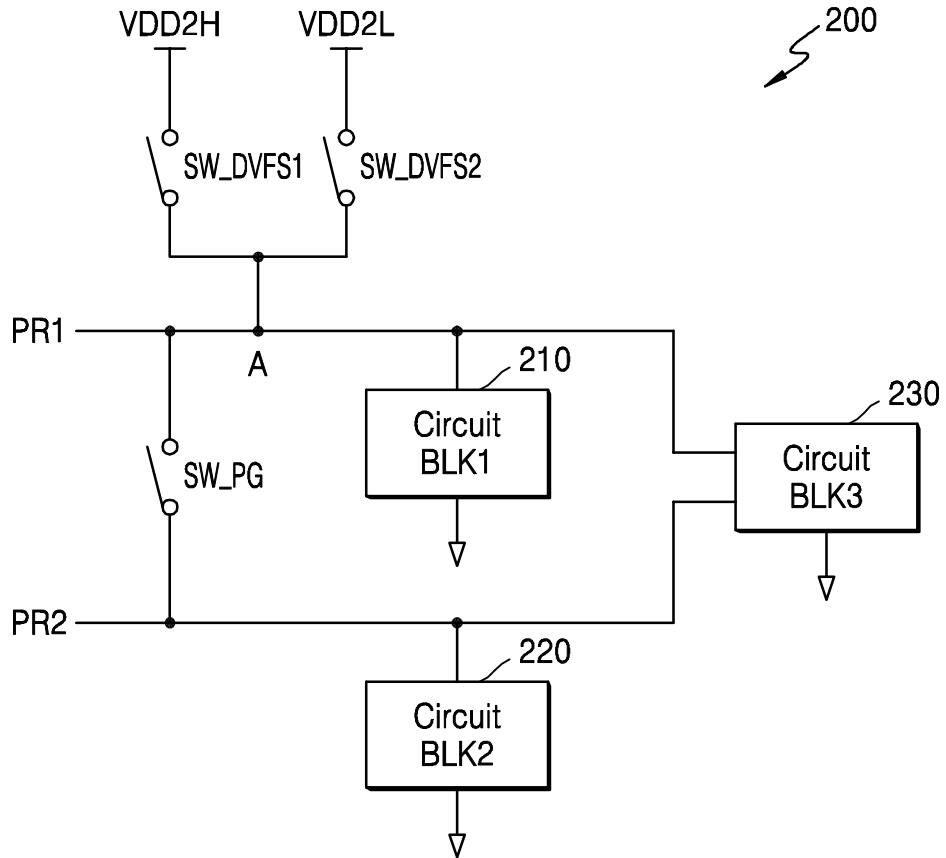


FIG. 3

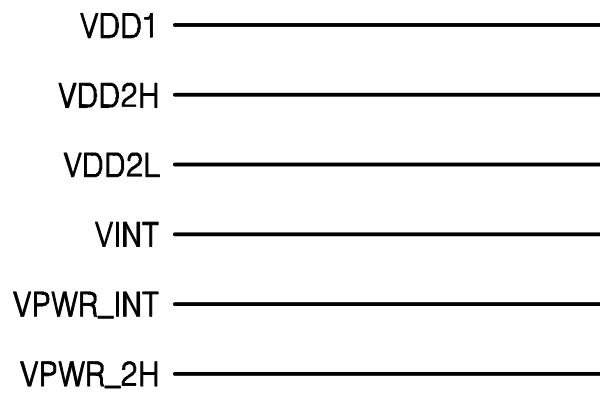


FIG. 4A

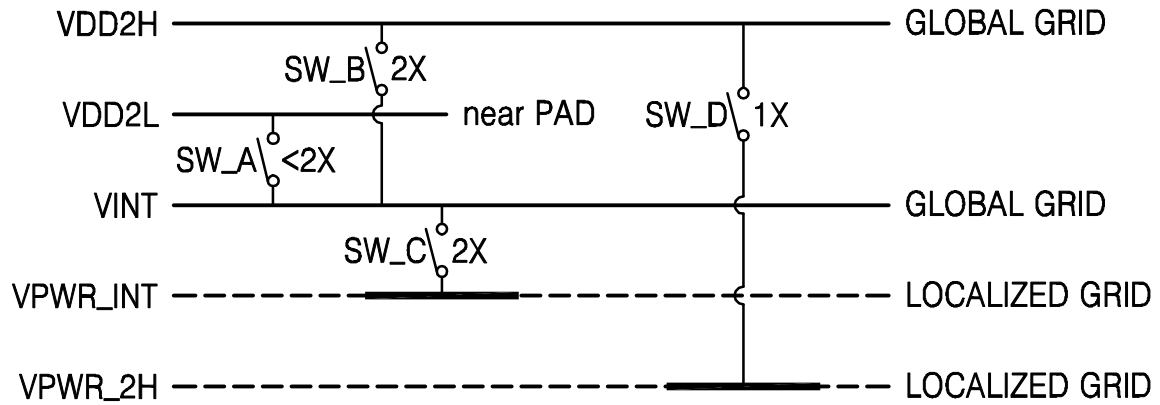


FIG. 4B

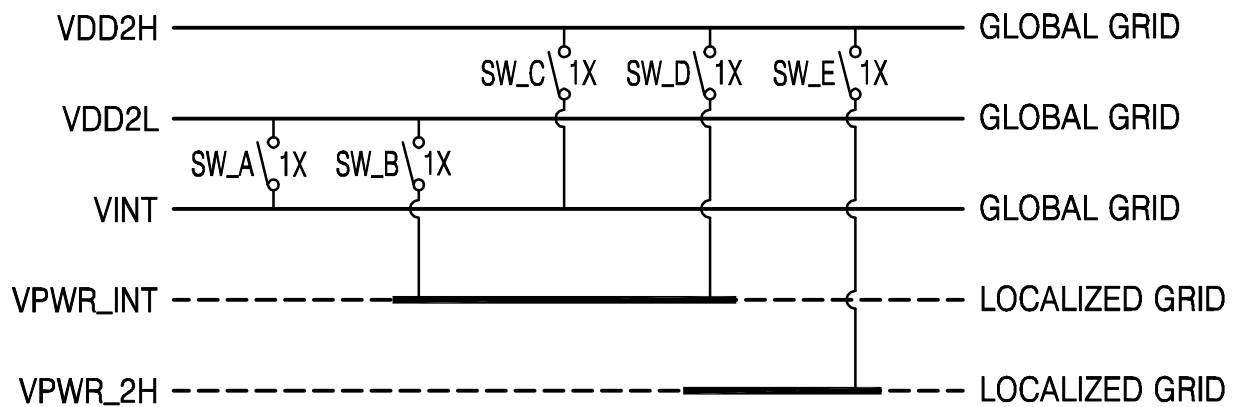


FIG. 5A

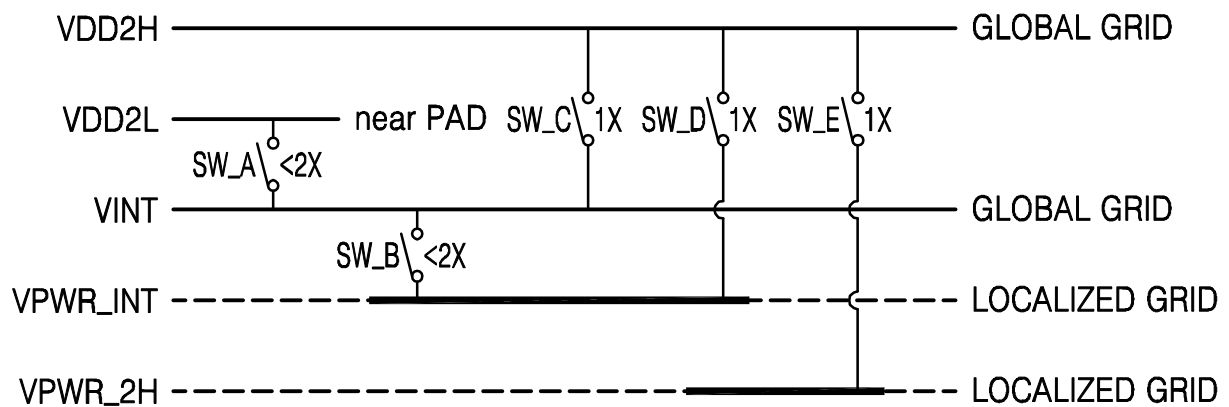


FIG. 5B

		SW_A	SW_B	SW_C	SW_D	SW_E
VDD2H only+PG=VPWR_2H		X	X	X	X	1/0
D V F S	VINT=VDD2L	1	X	0	X	X
	VINT=VDD2H	0	X	1	X	X
	VPWR_INT=VDD2L+PG	1	1/0	0	0	X
	VPWR_INT=VDD2H+PG	0	1/0	1	1/0	X

FIG. 6A

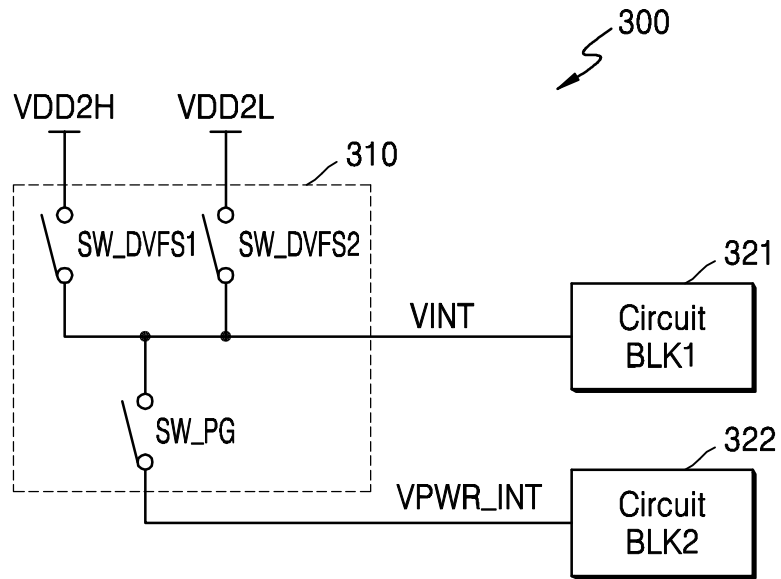


FIG. 6B

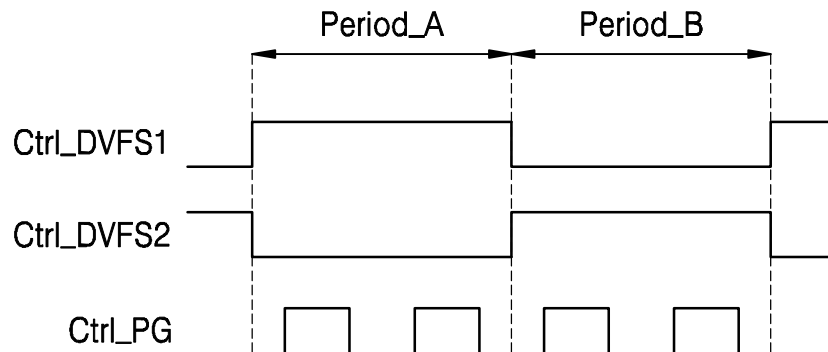


FIG. 7

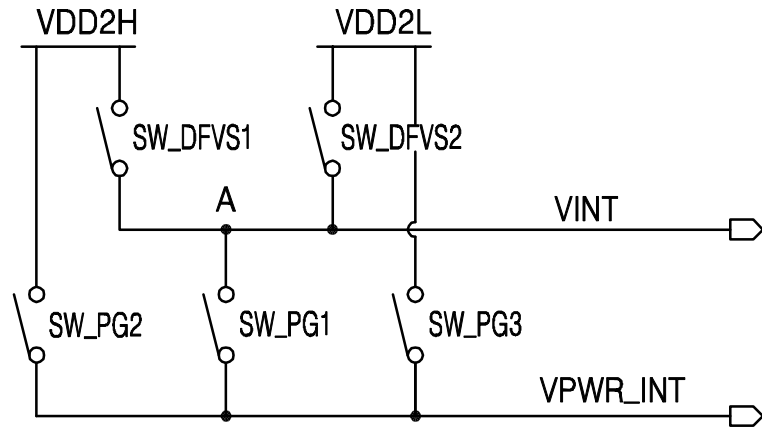


FIG. 8

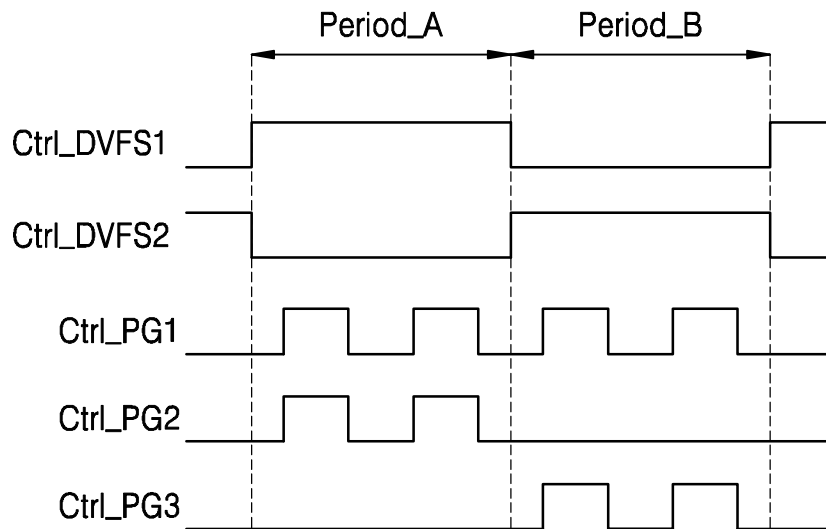


FIG. 9

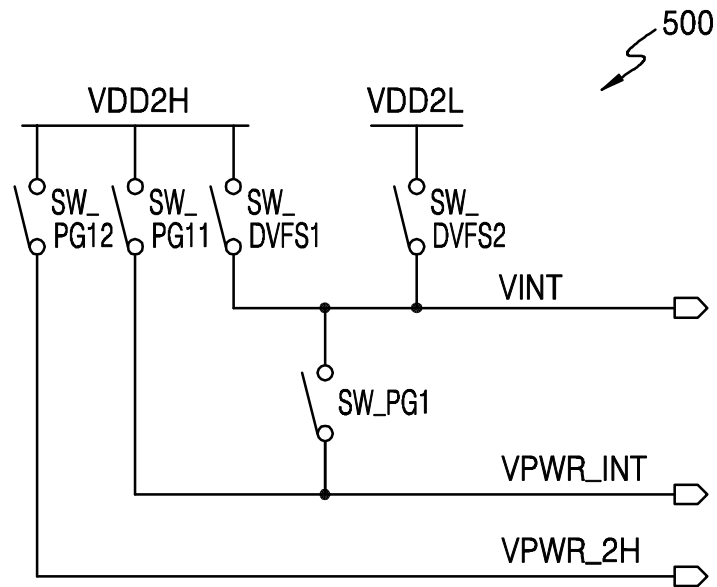


FIG. 10

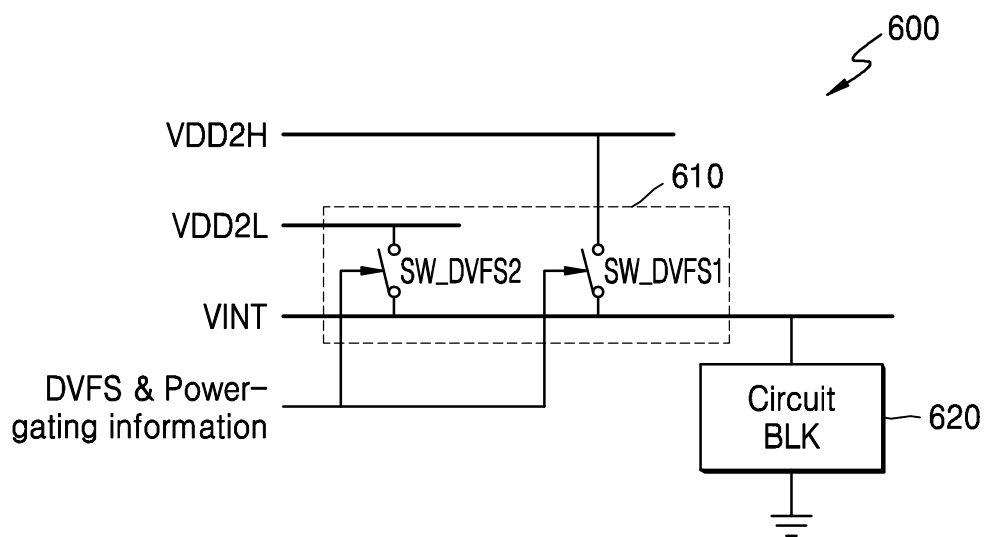


FIG. 11

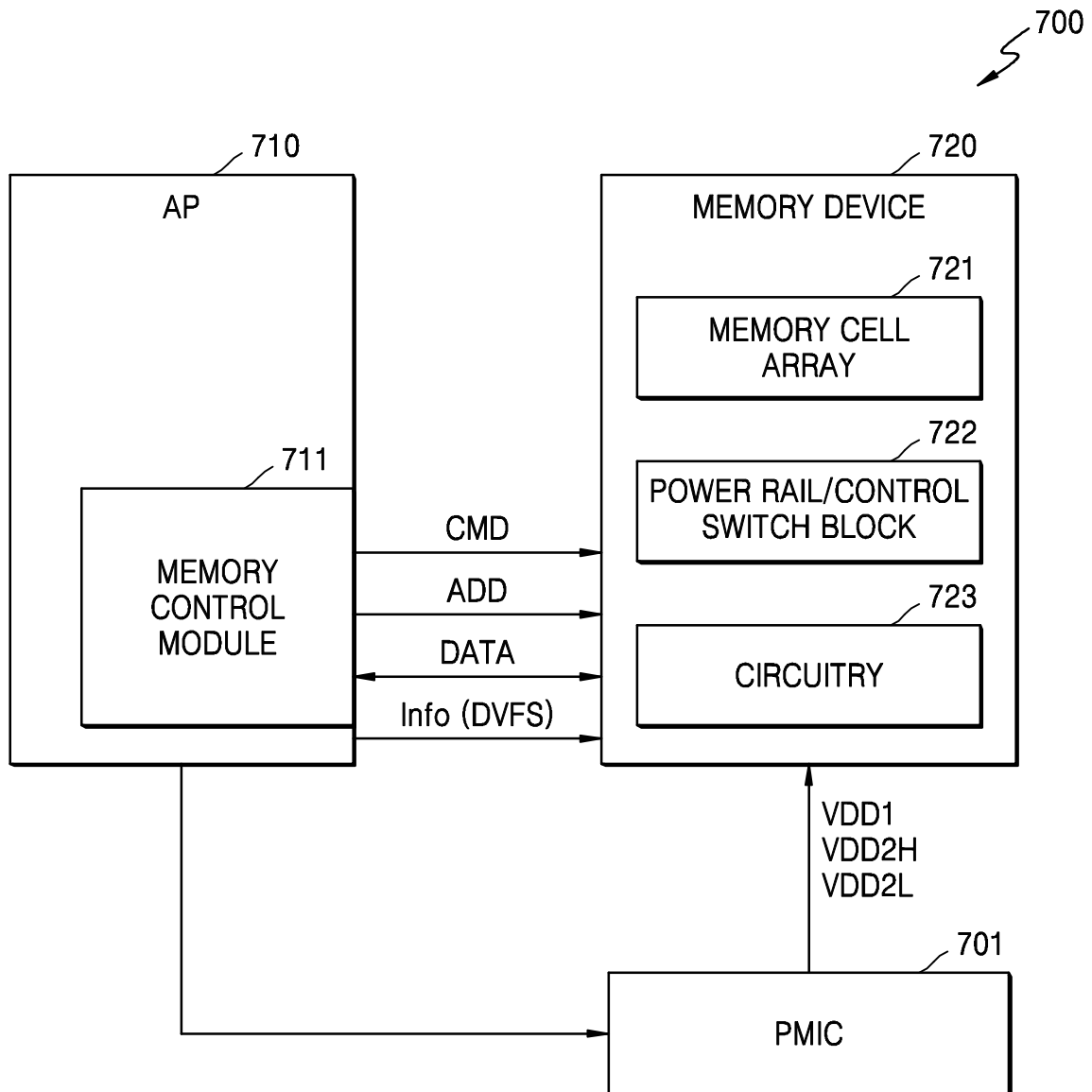


FIG. 12

