

Description

The present invention relates to a data processor having two modes of operation.

A conventional data processor, for example the 16-bit microprocessor HD68000 of Hitachi, Ltd., has program execution states such as an operation mode called a supervisor state and a mode called a user state. The processor operates either of the two modes (for details, refer to page 52 of the "HMCS 68000 Hitachi Microcomputer System HD68000, HD68000Y, HD68000PHD, 68000PS Micro Processing Unit (MPU)").

The supervisor state is a "higher" state of the program execution states and the central processing unit (CPU) can use any instruction and can access any register in this state. On the other hand, the user state is a "lower" state of the program execution states and the CPU is not permitted to use the instructions and registers which significantly affect the system in this state. Thus, in the supervisor state, the CPU can execute predetermined instructions which the CPU cannot execute in the user state.

As described above, with the provision of two program execution states, the microprocessor can efficiently execute e.g. multitask processing.

Furthermore, a microcomputer having two program execution states, as described above, normally has a bit in the status register of the CPU for indicating whether the current state is the supervisor state or the user state. Thus, the bit indicates the current program execution state.

However, when for example, a device such as a RAM for which a data access is possible is integrated in a microprocessor having two program execution states as discussed above, there arises the following problem.

When the CPU uses the integrated RAM as a data area in the supervisor state, if the CPU accesses by mistake that area in the user state, there is the risk that important data may possibly be destroyed in some cases.

The present invention therefore seeks to prevent an invalid access to, for example, an RAM area used in the supervisor state from being mistakenly effected in a microcomputer having at least two program execution states including a supervisor state and a user state. This prevents or at least reduces the risk of, the destruction of important data and hence improves the reliability of the system.

In an article by B Furht et al entitled "A Survey of Microprocessor Architectures for Memory Management", published in Computer, Vol 20, No 3 (March 1987) p 48 to 67, there is a discussion of microprocessor architectures that support memory management. It describes a microprocessor system having three levels, one being for access to a high speed cache, one being for access to a main memory, and one being for access to a large capacity storage device, such as a disk. A central processing unit (CPU) of the microprocessor system is controlled for memory access by data stored in segment registers. However, this disclosure does not address the different operation needed in the user and supervisor states.

Therefore, according to the present invention as defined in claim 1, there is provided a microcomputer formed on a single semiconductor chip comprising a central processing unit (CPU) which is operable in either a supervisor mode which is permitted to execute all instructions of the microcomputer or a user mode which is limited in the instructions it is permitted to execute, and which includes a status register (SR) having a bit (s/u) for indicating the mode in which the central processing unit is operating, the microcomputer also having memory means for storing data;

wherein:

the microcomputer has a register (RCR) having a bit (ALV) for indicating whether the central processing unit can access the memory means in the user mode, the bit being settable only when the central processing unit is operating in the supervisor mode;

the central processing unit (CPU) is restricted from accessing the memory means when the bit (s/u) of the status register indicates that the central processing unit (CPU) is operating in the user mode, and the bit of the register indicates that the central processing unit is restricted from using the memory means in the user mode;

and the central processing unit (CPU) is arranged to access the memory means regardless of the bit of the register when the bit (s/u) of the status register (SR) indicates that the central processing unit (CPU) is operating in the supervisor mode.

Thus, it is possible to determine if a CPU of the processor has invalidly accessed the memory, a signal can be sent to the CPU to indicate the invalid access. Then, the selection of that memory can be disabled.

When it is desired that the CPU uses the RAM in the supervisor state, with the data then being kept permanently, when the processor is in use, a new flag or register is set, so that the processor is in a state which automatically prevents access to the associated RAM in the user state. Hence destruction or reading of important data may be prevented. It may also be possible to restore data destroyed by incorrect processing, thereby to improve the reliability of the system.

Embodiments of the present invention will now be described, by way of example, with reference to the

accompanying drawings, in which:

Fig 1 is a block diagram showing schematically a first embodiment when the present invention is applied to a microprocessor;

Fig 2 is a block diagram showing schematically a second embodiment of the present invention applied to a microprocessor;

Fig. 3 is a block diagram showing schematically a third embodiment of the present invention, as applied to a microprocessor; and

Fig. 4 is a diagram showing an example of a bit configuration of a bank mode register including an access level specifying bit of an integrated RAM of a processor according to the present invention.

Fig. 1 shows an embodiment in which the present invention is applied to a microprocessor having an integrated RAM. In this embodiment each circuit block enclosed by dot-and-dash lines in Fig. 1 is formed on a single semiconductor chip, such as a monocrystalline silicon substrate.

The microprocessor of this embodiment has a central processing unit (CPU) operating according to a microprogram control method. The central processing unit (CPU) has a micro read only memory (ROM) 1 in which a microprogram is stored and the micro ROM 1 is accessed from a microaddress decoder 2 so as sequentially to read out microinstructions constituting the microprogram.

The microaddress decoder 2 is supplied with an address signal generated by a microaddress generate circuit 4 based on an operation code of a microinstruction fetched into an instruction register 3, and when the address signal is decoded, there is read out a first instruction of a group of microinstructions in a sequence executing the macro instruction. The microinstruction thus read out is then decoded by a decoder 5 for control, thereby generating control signals for an execution unit 6 and the like including various registers and an arithmetic logic unit (ALU). Of the group of microinstructions in a sequence corresponding to the macro instruction, the second and subsequent micro instructions each are read out based on the next address in the previous microinstruction and the address supplied from the microaddress generate circuit 4 when a code of the next address field of the microinstruction previously read out is supplied to the microaddress decoder 2.

In addition, in the CPU, there is disposed a group 7 of control registers including a status register SR indicating the internal control state, a condition code register, CCR, program counter PC, a system stack pointer SSP, an I/O base register IBR enabling a group of the control registers above to be reallocatable in the address space of the CPU, an exception vector base register EBR for establishing relocatability of a vector for an exception processing in the CPU address space, and the like.

Moreover, the microprocessor of this embodiment is provided, in addition to an integrated RAM 11 to be used as work areas of the CPU including a temporary storage area of data and a stack area, although not particularly limited to, with a memory control circuit 12 formed on the same chip for achieving a refresh control, a chip selection control, and a wait state control. These circuits and the CPU are connected to each other via an address bus 21 and a data bus 22.

In addition, in the microprocessor of this embodiment, there are disposed an address setting register 16 for setting an address space in which the integrated RAM 11 is to be allocated, an address compare circuit 17 for comparing an address on the address bus 21 with an address set to the address setting register 16 so as to judge to determine whether or not the address generated by the CPU is used to access the integrated RAM, and an access level judge circuit 13 comprising an AND gate G_1 of which an input signal is a coincidence signal C outputted from the address compare circuit 17 and an AND gate G_2 of which the input signals include a signal obtained by inverting through an inverter INV_1 a state signal of the bit S/U indicating the supervisor/user state of the status register SR in the CPU and an output signal from the AND gate G_1 . Incidentally, "0" of the bit S/U indicates the user state, whereas "1" thereof designates the supervisor state. In addition, the coincidence signal C delivered from the address compare circuit 17 is supplied as a selection signal CS for selecting the RAM to the integrated RAM 11.

In addition, although not particularly limited to, there are disposed in the memory control circuit 12 a plurality of control registers RCR_1 to RCR_n including a bank mode register and a refresh control register each supplied with an address. Of these registers, a bit of the register RCR_1 accessible only in the supervisor state is employed as a bit ALV indicating whether or not the integrated RAM is accessible in the user state. The state signal of this bit ALV is supplied to the other input terminal of the AND gate G_1 constituting the access level judge circuit 13. Although not particularly limited to, when the access level specify bit ALV is "0", a state in which the RAM is accessible is indicated; whereas when the bit ALV contains "1", it is indicated that the RAM is not accessible.

In the memory control circuit 12, there is provided a decoder for decoding an address outputted from the CPU onto the address bus 21 so as to select one of the control registers RCR_1 to RCR_n . The system is configured such that a bit of a specified control register can be set via the data bus 22. In addition, according to this embodiment, in order to easily reallocate the group of control registers RCR_1 to RCR_n in the address space

by use of the I/O base register IBR, successive addresses are assigned to the registers RCR₁ to RCR_n.

In consequence, in the microprocessor of this embodiment, when the access level specify bit ALV in the control register RCR₁ is set to "1" and the bit S/U of the status register in the CPU is "0" indicating the user state, an address in the address space of the integrated RAM 11 is outputted to the address bus 21, and when the coincidence signal C at a high level is delivered from the address compare circuit 17, the output from the AND gate G₁ is set to the high level. As a result, the output of the AND gate G₂ of which the input is a signal obtained by inverting the state signal of the bit S/U is changed to the high level. The output signal is supplied as an access violation signal AV to the exception processing circuit 8 of the CPU.

As a result, the CPU recognizes that the integrated RAM is invalidly accessed and then controls the microaddress generate circuit 4 so as to call, for example, a trap routine from the micro ROM 1 for passing control to an associated exception processing, for example, thereby reading from an external memory a program to restore the data in the vector address method and to return to the state prior to the access. If the microprocessor possesses an integrated ROM, the program to restore the data may be stored in the integrated ROM.

Incidentally, the exception processing circuit 8 is configured so as to be supplied with a signal from the bit S/U in the status register SR for indicating the supervisor/user state such that an exception processing for a privilege violation other than that described above can also be executed.

In this fashion, in the embodiment above, according to the state of the status signal of the access level specify bit ALV of the integrated RAM 11 and that of the signal of the bit S/U in the status register SR for indicating the supervisor/user state, whether or not the integrated RAM 11 is accessible is discriminated so as to generate an access violation signal.

Table 1 shows the accessibility of the integrated RAM in the case above.

Table 1

Access level of integrated RAM	CPU execution state (S/U bit)	
	User state	Supervisor state
User level allowed	○	○
User level not allowed	X	○

○ : Accessible

X : Not accessible

In consequence, when it is desired that the CPU uses the integrated RAM in the supervisor state and keeps the data therein, "1" need only be set to the access level specify bit ALV in the control register RCR before the mode is changed to the user state. As a result of this operation, when the integrated RAM is used in the user state, a condition that the RAM is invalidly accessed can be recognized. On the other hand, when the data in the integrated RAM is unnecessary, only by setting the access level specify bit ALV to "0", the integrated RAM can be freely used in the user state, which enables the integrated RAM, even if the capacity thereof is small, to be effectively used. However, in place of the operation to supply the access violation signal AV to the microaddress generate circuit 4, there may be disposed a bit indicating whether or not a violation exists in a register of the group 7 of control registers of the CPU so as to set "1" to the pertinent register.

Incidentally, as an address setting register 16, there may be disposed a register specifying, in addition to the address designating an address space of the integrated RAM 11, a partial area of the integrated RAM 11. As a result, in a case where the area to be used in the supervisor state is a portion of the integrated RAM 11, the access can be inhibited in the user state only to the area thus used. In addition, according to the embodiment above, although the access level specify bit ALV is located in the control register RCR of the control circuit 12, the present invention is not limited thereto; namely, there may be provided a flag or a register dedicated for the access inhibition.

In addition, the register may be positioned at an outside or inside location with respect to the CPU; furthermore, a free bit of a status register or a control register in the CPU may also be used.

Moreover, by configuring the register having the access level specify bit such that the register can be set to the reset or set state in response to a reset signal R, an invalid access to the integrated RAM attempted

prior to an initialization immediately after the power is turned on can be prevented.

FIG. 2 shows the second embodiment of a microprocessor according to the present invention.

In the microprocessor of this embodiment, there is disposed a new register 18 having the access level specify bit ALV; in addition, by using the access violation signal AV outputted from the access level judge circuit 13 configured in the same fashion as that of the embodiment of FIG. 1, the selection signal CS supplied to the integrated RAM 11 is forcibly negated so as to inhibit the access itself to the RAM 11.

That is, there is disposed an AND gate G_3 of which the input signals include the address coincidence signal C delivered from the address compare circuit 17 and a signal attained by inverting through an inverter INV_2 the access violation signal AV outputted from the access level judge circuit 13 such that an output from this gate G_3 is supplied as a selection signal CS to the integrated RAM 11.

In consequence, according to this embodiment, if "1" is set to the ALV bit of the control register 18, even when an address in the address space of the RAM 11 is outputted to the address bus 21, an access to the integrated RAM 11 is not accomplished. As a result, the data in the RAM 11 used in the supervisor state can be protected.

FIG. 3 shows the third embodiment of a microprocessor according to the present invention.

In the embodiment above, description has been given of a case where the integrated RAM assigned as a work area of the CPU cannot be used in the user state; whereas, in this third embodiment, in a case where a register bank employed in a multitask processing comprises the RAM, the register bank is set so as to be used or not to be used in the user state. That is, a group 14 of general-purpose registers comprising the RAM possesses 16 register banks BN_0 to BN_{15} each including 16 registers, and there are disposed a register bank number specify bit for specifying one of the register banks BN_0 to BN_{15} and a bank mode register BMR supervising a change-over bit and the like of the register banks as one of the control registers in the register group 7. Moreover, a bit of the bank mode register BMR is employed as the access level specify bit ALV such that the state signal of this bit ALV is inputted to the AND gate G_1 of the access level judge circuit 13 configured in the same fashion as that of the embodiment of FIG. 1.

In addition, according to this embodiment, the address setting register 16 and the address compare circuit 17 of the embodiment of FIG. 1 are located in the memory control circuit 12 effecting the selection control of the general-purpose register group 14 and the control register group 7, and when an address on the address bus 21 is within the address range of the general-purpose register group 14, an address coincidence detection signal C is to be supplied from the memory control circuit 12 to the AND gate G_1 of the access level judge circuit 13. Moreover, in this embodiment, if an address coincidence is detected when the ALV bit is "1", the selection signal CS for selecting the RAM constituting the register group 14 is not to be changed to the selection level.

As a result, in this embodiment, by setting "1" to the access level specify bit ALV in the bank mode register BMR by use of a dedicated instruction, an access to a register bank used in the supervisor state can be inhibited in the user state, thereby smoothly and safely effecting the change-over of the multitask processing.

FIG. 4 shows a configuration example of the bank mode register provided with an access level specify bit associated with the RAM.

The bank mode register BMR of this embodiment includes eight bits comprising an RAM enable control bit RAME, a bank permit mode specify bit BPM, an internal RAM access level specify bit ALV according to the present invention, a bank mode specify bit BMD, a system stop mode specify bit SSTOP, a bus retry enable control bit BRTE, and bank select bits SLCT1 and SLCT0.

Among these bits, when the RAM enable control bit RAME is set to "1", the integrated RAM is enabled to be effective; whereas, when RAME is cleared to "0", the integrated RAM as a memory is set to be ineffective. In this situation, if an access is issued to a data area of the integrated RAM by use of an address thereof, the same address of an external device is to be accessed.

In addition, the bank permit mode specify bit BPM is disposed to determine whether or not a portion of the integrated RAM associated with the register bank area of the CPU can be accessed as a memory. When the bit BPM is set to "1", this area above can be accessed as a memory; whereas, when the bit BPM is cleared to "0", the area cannot be accessed as a memory. When a read operation is accomplished on this area in a case of $BPM = 0$, all bits are attained as undefined bits; whereas, even when a write operation is attempted thereon, the RAM is not influenced with the write operation and the value stored therein is kept unchanged.

Incidentally, the bit BPM is effective when "1" is set to the bit RAME. If the bit RAME is cleared to "0", an external device is accessed regardless of whether the bit BPM is "1" or "0".

The system stop mode specify bit SSTOP is used to select a low consumption power state of the CPU when a particular instruction called an SLEEP is executed. If an SLEEP instruction is executed when the bit SSTOP is "0", the system enters the sleep mode in which only the operation of the CPU is stopped with the operations of the peripheral devices remained unchanged. On the other hand, if the SLEEP instruction is exe-

cutted when the bit SSTOP is set to "1", the system is set to the system stop mode in which the operations of the CPU and peripheral devices excepting the refresh controller of the integrated RAM are stopped. Incidentally, in the sleep mode, the CPU is initiated again only in response to an interruption from a peripheral device or an external device; whereas, in the system stop mode, the CPU is reactivated only in response to an external interruption.

The bus retry enable control bit BRTE is employed to specify a countermeasure procedure to be effected when a bus error takes place. When the bit BRTE is cleared to "0", the system enters the bus error mode in which the bus error exception processing sequence is achieved; whereas, when the bit BRTE is set to "1", the bus retry mode is set so as to effect the same bus cycle again.

In addition, the bank mode specify bit BMD is disposed to specify a utilization method of the register banks of the integrated RAM together with the bank select bits SLCT1 and SLCT0. When the bit BMD is cleared to "0", the system enters the global mode in which only one of a plurality of register banks can be used; whereas, when the bit BMD is set to "1", one half of the integrated RAM is used as eight global banks and the remaining half thereof is employed such that the RAM provides an infinite number of successive banks. Incidentally, in any mode above, for the global banks, the bank number register can be rewritten by use of a dedicated bank switch instruction when an interruption takes place, thereby effecting a switching or change-over operation between global banks.

Furthermore, the bank select bits SLCT1 and SLCT0 can be used to change the configuration of the banks according to the combination of SLCT1 and SLCT0 in the global mode in which the bank mode specify bit BMD is "0". That is, when SLCT1 and SLCT0 are "0, 0", "0, 1", "1, 0", and "1, 1"; there are established the 2-bank, 4-bank, 8-bank, and 16-bank configurations, respectively.

Incidentally, like in the case of the embodiment of FIG. 1, the access violation signal AV outputted from the access level judge circuit 13 may be supplied to the CPU to notify the access level violation to the CPU, thereby effecting the restoration thereof and the countermeasure processing.

Furthermore, according to the embodiment above, in a case where an access violation is detected, the condition is notified to the CPU so as to return to the original state through an exception processing or an access to the integrated RAM itself is inhibited; however, there may be disposed an access inhibit bit in the control register RCR₁, the control register 18, or other register such that whether the access to the RAM is inhibited or the data is to be restored after the invalid access can be selected when an access violation takes place. In addition, it is also possible in this situation to dispose a read/write specify bit such that a read access is allowed and only a write access is inhibited depending on the setting of the read/write specify bit.

In addition, in a case where there is configured a microprocessor not having a function in which the allocation address of the integrated RAM 11 can be freely reallocated in the address space possessed by the microprocessor, the address compare circuit 17 can be replaced with a decode circuit having a relatively simple circuit configuration. The address compare circuit 17 compares the address on the address bus 21 with the allocation address of the integrated RAM 11 and is hence completely operable even if the allocation address is changed. However, if the allocation address is fixed, the same function can be possessed with a decode circuit having a smaller circuit size.

Incidentally, according to the embodiment above, there is disposed a register or a flag to which the access level of the integrated RAM is set so as to enable the control to be effected by means of the program; however, for example, if there is a margin in the number of pins of the microprocessor, there may be disposed a terminal to set the access level from an external device, thereby enabling the hardware control to be achieved by the external circuit.

In addition, with reference to the embodiment above, description has been given of a prevention of the data destruction in the integrated RAM; however, the protection of secrecy of the ROM data can be effected by applying the present invention to a read only memory (ROM) integrated in the microprocessor, a programmable ROM (PROM), an erasable PROM (EPROM) of which data is erasable by means of a ultraviolet ray, an electrically EPROM (EEPROM) of which data is electrically writable and erasable, and the like.

In addition, the RAM as an object of the control above need not be limited to the integrated RAM, namely, an external RAM is also applicable.

Moreover, in place of the provision of the access level specify bit ALV in the control register, the bit may be disposed as a flag.

According to the present invention, there are attained the following effects.

That is, there are disposed a flag or a register having such a flag indicating whether or not an RAM area used by the CPU in the supervisor state can be used in the user state and a judge circuit for judging to determine based on the content of the register and that of the supervisor/user state indication bit of the status register whether or not the CPU has attempted an invalid access to the RAM in the user state, and when an access violation occurs, a violation signal is sent to the CPU and a selection signal of the RAM is negated (is set to

the invalid state). Consequently, in a case where the CPU uses the RAM in the supervisor state and the data is desired to be kept therein, by setting a state inhibiting the access to the new flag or register thus disposed, an access to the corresponding RAM in the user state is automatically inhibited. Through this operation, a destruction or a read out operation of important data can be prevented and the data destroyed by an exception processing or the like can be restored. This leads to an effect that the reliability of the system is greatly improved.

A concrete description has been given of the invention accomplished by the present inventor with reference to the embodiments; however, the present invention is not limited by those embodiments. It is to be appreciated that the embodiments can be changed and modified without departing from the scope of the present invention. For example, in the embodiments above, there is disposed a register or flag indicating the access level of the RAM such that depending on the state thereof, the integrated RAM can be used only in the supervisor state or in the supervisor and user states; however, there may be disposed two integrated RAMs each having the same address space such that depending on the content of the register designating the access level, either one of the RAMs is set to be accessible so as to prevent an access in the user state to the RAM used in the supervisor state, thereby protecting the data in the RAM. However, when the integrated RAM is shared between the supervisor and user states like in the case of the embodiment, a higher utilization rate of the memory is developed.

In addition, according to the embodiment above, when an access violation with respect to the integrated RAM is detected, the access is inhibited or a restoration of the data is effected; however, the present invention is also applicable to a case where the CPU simply wants to know whether or not the user has referenced the integrated RAM.

Furthermore, although the description has been given of a memory access violation and the countermeasure processing thereof in conjunction with the embodiment, the present invention is also applicable to a case where the access in the user state is to be inhibited with respect to the peripheral I/O devices other than the memory, for example, a particular I/O port.

The description above is associated with cases where the invention primarily accomplished by the present inventor is applied to a microprocessor as an utilization field as the background of the invention; however, the present invention is not restricted by those cases but can be utilized in a single-chip microcomputer comprising a timer, a serial communication circuit, DMA controller, and the like disposed on the same chip, a microcomputer of a board type, and a general data processor having a function associated with a data access.

Claims

1. A microcomputer formed on a single semiconductor chip comprising a central processing unit (CPU) which is operable in either a supervisor mode which is permitted to execute all instructions of the microcomputer or a user mode which is limited in the instructions it is permitted to execute, and which includes a status register (SR) having a bit (s/u) for indicating the mode in which the central processing unit is operating, the microcomputer also having memory means (11) for storing data;
 - characterised in that:
 - the microcomputer has a register (RCR) having a bit (ALV) for indicating whether the central processing unit can access the memory means in the user mode, the bit being settable only when the central processing unit is operating in the supervisor mode;
 - the central processing unit (CPU) is restricted from accessing the memory means (11) when the bit (s/u) of the status register indicates that the central processing unit (CPU) is operating in the user mode, and the bit of the register indicates that the central processing unit (CPU) is restricted from using the memory means (11) in the user mode;
 - and the central processing unit (CPU) is arranged to access the memory means (11) regardless of the bit of the register when the bit (s/u) of the status register (SR) indicates that the central processing unit (CPU) is operating in the supervisor mode.
2. A microcomputer according to claim 1, further including an address register (16) for allocating address space to the memory means (11).
3. A microcomputer according to claim 2, further comprising:
 - a comparator means (17) for comparing an address of the address register (16) and an address located on an address bus of the microcomputer; and
 - an outputting means for outputting a resultant signal of the comparison.

the invalid state). Consequently, in a case where the CPU uses the RAM in the supervisor state and the data is desired to be kept therein, by setting a state inhibiting the access to the new flag or register thus disposed, an access to the corresponding RAM in the user state is automatically inhibited. Through this operation, a destruction or a read out operation of important data can be prevented and the data destroyed by an exception processing or the like can be restored. This leads to an effect that the reliability of the system is greatly improved.

A concrete description has been given of the invention accomplished by the present inventor with reference to the embodiments; however, the present invention is not limited by those embodiments. It is to be appreciated that the embodiments can be changed and modified without departing from the scope of the present invention. For example, in the embodiments above, there is disposed a register or flag indicating the access level of the RAM such that depending on the state thereof, the integrated RAM can be used only in the supervisor state or in the supervisor and user states; however, there may be disposed two integrated RAMs each having the same address space such that depending on the content of the register designating the access level, either one of the RAMs is set to be accessible so as to prevent an access in the user state to the RAM used in the supervisor state, thereby protecting the data in the RAM. However, when the integrated RAM is shared between the supervisor and user states like in the case of the embodiment, a higher utilization rate of the memory is developed.

In addition, according to the embodiment above, when an access violation with respect to the integrated RAM is detected, the access is inhibited or a restoration of the data is effected; however, the present invention is also applicable to a case where the CPU simply wants to know whether or not the user has referenced the integrated RAM.

Furthermore, although the description has been given of a memory access violation and the countermeasure processing thereof in conjunction with the embodiment, the present invention is also applicable to a case where the access in the user state is to be inhibited with respect to the peripheral I/O devices other than the memory, for example, a particular I/O port.

The description above is associated with cases where the invention primarily accomplished by the present inventor is applied to a microprocessor as an utilization field as the background of the invention; however, the present invention is not restricted by those cases but can be utilized in a single-chip microcomputer comprising a timer, a serial communication circuit, DMA controller, and the like disposed on the same chip, a microcomputer of a board type, and a general data processor having a function associated with a data access.

Claims

1. A microcomputer formed on a single semiconductor chip comprising a central processing unit (CPU) which is operable in either a supervisor mode which is permitted to execute all instructions of the microcomputer or a user mode which is limited in the instructions it is permitted to execute, and which includes a status register (SR) having a bit (s/u) for indicating the mode in which the central processing unit is operating, the microcomputer also having memory means (11) for storing data;
 - characterised in that:
 - the microcomputer has a register (RCR) having a bit (ALV) for indicating whether the central processing unit can access the memory means in the user mode, the bit being settable only when the central processing unit is operating in the supervisor mode;
 - the central processing unit (CPU) is restricted from accessing the memory means (11) when the bit (s/u) of the status register indicates that the central processing unit (CPU) is operating in the user mode, and the bit of the register indicates that the central processing unit (CPU) is restricted from using the memory means (11) in the user mode;
 - and the central processing unit (CPU) is arranged to access the memory means (11) regardless of the bit of the register when the bit (s/u) of the status register (SR) indicates that the central processing unit (CPU) is operating in the supervisor mode.
2. A microcomputer according to claim 1, further including an address register (16) for allocating address space to the memory means (11).
3. A microcomputer according to claim 2, further comprising;
 - a comparator means (17) for comparing an address of the address register (16) and an address located on an address bus of the microcomputer; and
 - an outputting means for outputting a resultant signal of the comparison.



4. A microcomputer according to any one of the preceding claims wherein said memory means (11) is a RAM .
5. A microcomputer according to claim 4, wherein said RAM is a memory constituting a group of general registers of said central processing unit.
6. A microcomputer according to claim 4 or claim 5, further including a control register in said central processing unit (CPU) for controlling a utilization of register banks in said RAM, said register having a bit for specifying an access level of said RAM.
7. A microcomputer according to any one of claims 4 to 6, further including an array base address register, wherein the array base address register controls placement location of a RAM within the memory means (11), the placement location allowing one of, access to RAM only when the central processing unit (CPU) is in supervisor mode and access to RAM when the central processing unit (CPU) is in supervisor or user mode.
8. A microcomputer according to any one of the preceding claims, comprising ignore means (8,13) for ignoring access of the central processing unit to the memory means (11) when the bit (s/u) of the status register (SR) indicates that the central processing unit (CPU) is operating in the user mode and the bit (ALV) of the register (RCR) indicates that the central processing unit (CPU) is restricted from use of the memory means (11) while in the user mode.
9. A microcomputer according to any one of the preceding claims, further including access control means (8,13) responsive to the bit of said register (RCR) for overriding said restriction on access of said memory means (11) by said central processing unit in said user mode if the bit of said register (RCR) represents permitting said central processing unit in said supervisor mode to access said memory means.
10. A microcomputer according to claim 9, wherein said access control means (8,13) includes judging means coupled to said status register (SR) and to said register (RCR) for judging whether accessing of said memory means by said central processing unit is to be overridden on the basis of both the bit of said status register and the bit of said register (RCR).
11. A microcomputer according to claim 10, wherein said single chip microcomputer further comprises address defining means for allocating a predetermined address to said memory means, wherein said central processing unit (CPU) further comprises address signal generating means for generating address signals, and wherein said access control means (8,13) further comprises comparing means for comparing said predetermined address with address signals generated by said address signal generating means to judge whether or not said memory means (11) is accessed by said central processing unit (CPU).
12. A microcomputer according to any one of the preceding claims, having further access control means responsive to the bit of said register for ignoring access to said memory means by said central processing unit (CPU) when it is in said user mode when the bit of said register (RCR) represents said supervisor mode.
13. A microcomputer according to claim 12, wherein said further access control means includes judging means coupled to said status register (SR) and to said register (RCR) for judging whether accessing of said memory means (11) by said central processing unit (CPU) is to be inhibited on the basis of both the bit of said status register (SR) and the bit of said register (RCR).
14. A microcomputer according to claim 12, wherein said single chip microcomputer further comprises address defining means for allocating a predetermined address to said memory means, wherein said central processing unit (CPU) further comprises address signal generating means for generating address signals, and wherein said further access control means further comprises comparing means for comparing said predetermined address with address signals generated by said address signal generating means to judge whether or not said memory means (11) is accessed by said central processing unit (CPU).
15. A microcomputer according to any one of the preceding claims, further including third access control means responsive to the bit of said register (RCR) for ignoring accessing for said memory means (11) by said central processing unit (CPU) in said user mode if the bit of said register (RCR) represents permitting



said central processing unit (CPU) in said supervisor mode to access said memory means (11).

16. A microcomputer according to claim 15, wherein said third access control means includes judging means coupled to said status register (SR) and to said register for judging whether or not accessing for said memory means (11) by said central processing unit (CPU) is to be ignored on the basis of both the bit of said status register (SR) and the bit of said register (RCR).
17. A microcomputer according to claim 16, wherein said microcomputer further comprises address defining means for allocating a predetermined address to said memory means (11), wherein said central processing unit (CPU) further comprises address signal generating means for generating address signals, and wherein said third access control means further comprises comparing means for comparing said predetermined address with address signals generated by said address signal generating means to judge whether or not said memory means (11) is accessed by said central processing unit (CPU).

Patentansprüche

1. Auf einem einzelnen Halbleiterchip ausgebildeter Mikrocomputer mit einer zentralen Verarbeitungseinheit (CPU), die entweder in einem Kontrollmodus, in dem alle Anweisungen des Mikrocomputers ausgeführt werden, oder einem Benutzermodus betrieben werden kann, der hinsichtlich der zur Ausführung freigegebenen Anweisungen beschränkt ist, und die ein Statusregister (SR) mit einem Bit (s/u) zum Kennzeichnen des Modus, in dem die zentrale Verarbeitungseinheit arbeitet, beinhaltet, und der Mikrocomputer auch eine Speichereinrichtung (11) zum Abspeichern von Daten aufweist; dadurch gekennzeichnet, daß:
 - der Mikrocomputer ein Register (RCR) mit einem Bit (ALV) zum Kennzeichnen, ob die zentrale Verarbeitungseinheit im Benutzermodus auf die Speichereinrichtung zugreifen kann, aufweist, wobei das Bit nur dann setzbar ist, wenn die zentrale Verarbeitungseinheit im Kontrollmodus arbeitet;
 - die zentrale Verarbeitungseinheit (CPU) nicht auf die Speichereinrichtung (11) zugreifen darf, wenn das Bit (s/u) des Statusregisters anzeigt, daß die zentrale Verarbeitungseinheit (CPU) im Benutzermodus arbeitet und das Bit des Registers anzeigt, daß die zentrale Verarbeitungseinheit (CPU) im Benutzermodus die Speichereinrichtung (11) nicht verwenden darf;
 - und die zentrale Verarbeitungseinheit (CPU) so ausgebildet ist, daß sie unabhängig vom Bit des Registers auf die Speichereinrichtung (11) zugreift, wenn das Bit (s/u) des Statusregisters (SR) anzeigt, daß die zentrale Verarbeitungseinheit (CPU) im Kontrollmodus arbeitet.
2. Mikrocomputer nach Anspruch 1, ferner mit einem Adreßregister (16) zum Zuordnen von Adreßraum zur Speichereinrichtung (11).
3. Mikrocomputer nach Anspruch 2, ferner mit:
 - einer Komparatoreinrichtung (17) zum Vergleichen der Adresse im Adreßregister (16) und einer Adresse, die auf dem Adressenbus des Mikrocomputers liegt; und
 - einer Ausgabeeinrichtung zum Ausgeben des sich ergebenden Vergleichssignals.
4. Mikrocomputer nach einem der vorstehenden Ansprüche, bei dem die Speichereinrichtung (11) ein RAM ist.
5. Mikrocomputer nach Anspruch 4, bei dem der RAM ein Speicher ist, der eine Gruppe von Universalregistern der zentralen Verarbeitungseinheit bildet.
6. Mikrocomputer nach Anspruch 4 oder Anspruch 5, ferner mit einem Steuerregister in der zentralen Verarbeitungseinheit (CPU) zum Steuern der Verwendung der Registerbänke im RAM, wobei das Register ein Bit zum Spezifizieren des Zugriffsangs für den RAM aufweist.
7. Mikrocomputer nach einem der Ansprüche 4 bis 6, ferner mit einem Arraybasis-Adreßregister, das die Anordnungsstelle eines RAM innerhalb der Speichereinrichtung (11) steuert, die entweder einen Zugriff auf den RAM nur dann zuläßt, wenn sich die zentrale Verarbeitungseinheit (CPU) im Kontrollmodus befindet, oder einen Zugriff auf den RAM dann zuläßt, wenn sich die zentrale Verarbeitungseinheit (CPU) im Kontrollmodus, oder im Benutzermodus befindet.



8. Mikrocomputer nach einem der vorstehenden Ansprüche, mit einer Ignoriereinrichtung (8, 13) zum Ignorieren eines Zugriffs der zentralen Verarbeitungseinheit auf die Speichereinrichtung (11), wenn das Bit (s/u) des Statusregisters (SR) anzeigt, daß die zentrale Verarbeitungseinheit (CPU) im Benutzermodus arbeitet und das Bit (ALV) des Registers (RCR) anzeigt, daß die zentrale Verarbeitungseinheit (CPU) die Speichereinrichtung (11) nicht benutzen darf, während sie sich im Benutzermodus befindet.
9. Mikrocomputer nach einem der vorstehenden Ansprüche, ferner mit einer Zugriffssteuerungseinrichtung (8, 13), die auf das Bit des Registers (RCR) anspricht, um das Verbot für den Zugriff auf die Speichereinrichtung (11) durch die zentrale Verarbeitungseinheit im Benutzermodus zu übergehen, wenn das Bit des Registers (RCR) anzeigt, daß die zentrale Verarbeitungseinheit im Kontrollmodus auf die Speichereinrichtung zugreifen darf.
10. Mikrocomputer nach Anspruch 9, bei dem die Zugriffssteuerungseinrichtung (8, 13) eine mit dem Statusregister (SR) und dem Register (RCR) verbundene Beurteilungseinrichtung aufweist, um zu beurteilen, ob ein Zugriff auf die Speichereinrichtung durch die zentrale Verarbeitungseinheit auf Grundlage sowohl des Bits des Statusregisters als auch des Bits des Registers (RCR) zu übergehen ist.
11. Mikrocomputer nach Anspruch 10, bei dem dieser Ein-Chip-Mikrocomputer ferner eine Adreßdefiniereinrichtung zum Zuordnen einer vorgegebenen Adresse zur Speichereinrichtung enthält, bei dem die zentrale Verarbeitungseinheit (CPU) ferner eine Adreßsignal-Erzeugungseinrichtung zum Erzeugen von Adreßsignalen enthält, und bei dem die Zugriffssteuerungseinrichtung (8, 13) ferner eine Vergleichseinrichtung zum Vergleichen der vorgegebenen Adresse mit von der Adreßsignal-Erzeugungseinrichtung erzeugten Adressen enthält, um zu beurteilen, ob durch die zentrale Verarbeitungseinheit (CPU) auf die Speichereinrichtung (11) zugegriffen wird oder nicht.
12. Mikrocomputer nach einem der vorstehenden Ansprüche, ferner mit einer Zugriffssteuerungseinrichtung, die auf das Bit des Registers anspricht, um einen Zugriff auf die Speichereinrichtung durch die zentrale Verarbeitungseinheit (CPU) zu ignorieren, wenn sich diese im Benutzermodus befindet und das Bit im genannten Register (RCR) den Kontrollmodus repräsentiert.
13. Mikrocomputer nach Anspruch 12, bei dem die weitere Zugriffssteuerungseinrichtung eine Beurteilungseinrichtung enthält, die mit dem Statusregister (SR) und dem Register (RCR) gekoppelt ist, um zu beurteilen, ob ein Zugriff auf die Speichereinrichtung (11) durch die zentrale Verarbeitungseinheit (CPU) auf Grundlage sowohl des Bits des Statusregisters (SR) als auch des Bits des Registers (RCR) zu verhindern ist.
14. Mikrocomputer nach Anspruch 12, bei dem dieser Ein-Chip-Mikrocomputer ferner eine Adreßdefiniereinrichtung zum Zuordnen einer vorgegebenen Adresse zur Speichereinrichtung aufweist, bei dem die zentrale Verarbeitungseinheit (CPU) ferner eine Adreßsignal-Erzeugungseinrichtung zum Erzeugen von Adreßsignalen aufweist, und bei dem die weitere Zugriffssteuerungseinrichtung ferner eine Vergleichseinrichtung zum Vergleichen der vorgegebenen Adresse mit von der Adreßsignal-Erzeugungseinrichtung erzeugten Adreßsignalen aufweist, um zu beurteilen, ob von der zentralen Verarbeitungseinheit (CPU) auf die Speichereinrichtung (11) zugegriffen wird oder nicht.
15. Mikrocomputer nach einem der vorstehenden Ansprüche, ferner mit einer dritten Zugriffssteuerungseinrichtung, die auf das Bit des Registers (RCR) anspricht, um einen Zugriff auf die Speichereinrichtung (11) durch die zentrale Verarbeitungseinheit (CPU) im Benutzermodus zu ignorieren, wenn das Bit des Registers (RCR) anzeigt, daß die zentrale Verarbeitungseinheit (CPU) im Kontrollmodus auf die Speichereinrichtung (11) zugreifen darf.
16. Mikrocomputer nach Anspruch 15, bei dem die dritte Zugriffssteuerungseinrichtung eine Beurteilungseinrichtung enthält, die mit dem Statusregister (SR) und dem genannten Register verbunden ist, um zu beurteilen, ob ein Zugriff auf die Speichereinrichtung (11) durch die zentrale Verarbeitungseinheit (CPU) zu ignorieren ist oder nicht, was auf Grundlage sowohl des Bits des Statusregisters (SR) als auch des Bits des genannten Registers (RCR) erfolgt.
17. Mikrocomputer nach Anspruch 16, bei dem dieser Mikrocomputer ferner eine Adreßdefiniereinrichtung zum Zuordnen einer vorgegebenen Adresse zur Speichereinrichtung (11) enthält, bei dem die zentrale Verarbeitungseinheit (CPU) ferner eine Adreßsignal-Erzeugungseinrichtung zum Erzeugen von Adreß-



signalen enthält, und bei dem die dritte Zugriffssteuerungseinrichtung ferner eine Vergleichseinrichtung zum Vergleichen der vorgegebenen Adresse mit von der Adreßsignal-Erzeugungseinrichtung erzeugten Adreßsignalen enthält, um zu beurteilen, ob von der zentralen Verarbeitungseinheit (CPU) auf diese Speichereinrichtung (11) zugegriffen wird oder nicht.

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Revendications

1. Micro-ordinateur formé sur une seule microplaquette à semiconducteurs, comprenant une unité centrale de traitement (CPU), qui peut fonctionner soit dans un mode superviseur, qui est autorisé pour l'exécution de toutes les instructions du micro-ordinateur, ou dans un mode utilisateur, qui est limité en ce qui concerne les instructions qu'il est autorisé à exécuter, et qui inclut un registre d'état (SR) comportant un bit (s/u) pour indiquer le mode dans lequel l'unité centrale de traitement fonctionne, le micro-ordinateur possédant également des moyens de mémoire (11) pour mémoriser des données;
 15 caractérisé en ce que :
 le micro-ordinateur comporte un registre (RCR) possédant un bit (ALV) servant à indiquer si une unité centrale de traitement peut ou non accéder aux moyens de mémoire dans le mode utilisateur, le bit pouvant être positionné uniquement lorsque l'unité centrale de traitement fonctionne dans le mode superviseur;
 20 l'accès de l'unité centrale de traitement (CPU) aux moyens de mémoire (11) est limité lorsque le bit (s/u) du registre d'état indique que l'unité centrale de traitement (CPU) fonctionne dans le mode utilisateur, et que le bit du registre indique que l'unité centrale de traitement (CPU) est limitée dans son utilisation des moyens de mémoire (11) dans le mode utilisateur; et
 l'unité centrale de traitement (CPU) est agencée de manière à accéder aux moyens de mémoire (11) indépendamment du bit de registre, lorsque le bit (s/u) du registre d'état (SR) indique que l'unité centrale de traitement (CPU) fonctionne dans le mode superviseur.
2. Micro-ordinateur selon la revendication 1, comprenant en outre un registre d'adresses (16) pour affecter un espace d'adresses aux moyens de mémoire (11).
3. Micro-ordinateur selon la revendication 2, comprenant en outre :
 30 des moyens comparateurs (17) pour comparer une adresse du registre d'adresses (16) et une adresse située dans le bus de transmission d'adresses du micro-ordinateur; et
 des moyens de sortie servant à délivrer un signal résultant de la comparaison.
4. Micro-ordinateur selon l'une quelconque des revendications précédentes, dans lequel lesdits moyens de mémoire (11) sont une mémoire RAM.
5. Micro-ordinateur selon la revendication 4, dans lequel ladite mémoire RAM est une mémoire constituant un groupe de registres généraux de ladite unité centrale de traitement.
6. Micro-ordinateur selon la revendication 4 ou 5, comprenant en outre un registre de commande dans ladite unité centrale de traitement (CPU) pour commander une utilisation de blocs de registres dans ladite mémoire RAM, ledit registre possédant un bit pour spécifier un niveau d'accès de ladite mémoire RAM.
7. Micro-ordinateur selon l'une quelconque des revendications 4 à 6, comprenant en outre un registre d'adresses de base de réseau, le registre d'adresses de base de réseau commandant la position d'emplacements d'une mémoire RAM dans les moyens de mémoire (11), la position d'emplacements permettant soit l'accès à la mémoire RAM uniquement lorsque l'unité centrale de traitement (CPU) est dans le mode superviseur, soit l'accès à la mémoire RAM lorsque l'unité centrale de traitement (CPU) est dans le mode superviseur ou dans le mode utilisateur.
8. Micro-ordinateur selon l'une quelconque des revendications précédentes, comprenant des moyens d'omission (8,13) pour ignorer l'accès de l'unité centrale de traitement aux moyens de mémoire (11) lorsque le bit (s/u) du registre d'état (SR) indique que l'unité centrale de traitement (CPU) fonctionne dans le mode utilisateur et que le bit (ALV) du registre (RCR) indique que l'utilisation des moyens de mémoire (11) par l'unité centrale de traitement (CPU) est limitée, lorsqu'elle se trouve dans le mode utilisateur.
9. Micro-ordinateur selon l'une quelconque des revendications précédentes, comprenant en outre des

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moyens de commande d'accès (8,13) répondant au bit dudit registre (RCR) pour une commande prioritaire de ladite limitation de l'accès auxdits moyens de mémoire (11) par ladite unité centrale de traitement dans ledit mode utilisateur si le bit dudit registre (RCR) représente une autorisation de ladite unité de traitement dans ledit mode superviseur à accéder auxdits moyens de mémoire.

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10. Micro-ordinateur selon la revendication 9, dans lequel lesdits moyens de commande d'accès (8,13) comprennent des moyens d'évaluation couplés audit registre d'état (SR) et audit registre (RCR) pour évaluer si l'accès desdits moyens de mémoire par ladite unité centrale de traitement doit être commandé de façon prioritaire sur la base à la fois du bit dudit registre d'état et du bit dudit registre (RCR).
- 10 11. Micro-ordinateur selon la revendication 10, dans lequel ledit micro-ordinateur monopuce comporte en outre des moyens de définition d'adresses pour affecter une adresse prédéterminée auxdits moyens de mémoire, et dans lequel ladite unité centrale de traitement (CPU) comporte en outre des moyens de production de signaux d'adresses pour produire des signaux d'adresses, et dans lequel lesdits moyens de commande d'accès (8,13) comprennent en outre des moyens comparateurs pour comparer ladite adresse prédéterminée à des signaux d'adresses produits par lesdits moyens de production de signaux d'adresses pour évaluer si ladite unité centrale de traitement (CPU) accède ou non auxdits moyens de mémoire (11).
- 15 12. Micro-ordinateur selon l'une quelconque des revendications précédentes, comportant en outre des moyens de commande d'accès répondant au bit dudit registre pour ignorer un accès auxdits moyens de mémoire par ladite unité centrale de traitement (CPU), lorsqu'elle est dans ledit mode utilisateur, lorsque le bit dudit registre (RCR) représente ledit mode superviseur.
- 20 13. Micro-ordinateur selon la revendication 12, dans lequel lesdits autres moyens de commande d'accès incluent des moyens d'évaluation couplés audit registre d'état (SR) et audit registre (RCR) pour évaluer si l'accès auxdits moyens de mémoire (11) par ladite unité centrale de traitement (CPU) doit être bloqué sur la base à la fois du bit dudit registre d'état (SR) et du bit dudit registre (RCR).
- 25 14. Micro-ordinateur selon la revendication 12, dans lequel ledit micro-ordinateur monopuce comprend en outre des moyens de définition d'adresses pour affecter une adresse prédéterminée auxdits moyens de mémoire, et dans lequel ladite unité centrale de traitement (CPU) comporte en outre des moyens de production de signaux d'adresses pour produire des signaux d'adresses, et dans lequel lesdits autres moyens de commande d'accès comprennent en outre des moyens comparateurs pour comparer ladite adresse prédéterminée à des signaux d'adresses produits par lesdits moyens de production de signaux d'adresses pour évaluer si ladite unité centrale de traitement (CPU) accède ou non auxdits moyens de mémoire (11).
- 30 15. Micro-ordinateur selon l'une quelconque des revendications précédentes, comprenant en outre de troisièmes moyens de commande d'accès répondant au bit dudit registre (RCR) pour ignorer l'accès auxdits moyens de mémoire (11) par ladite unité centrale de traitement (CPU) dans ledit mode utilisateur, si le bit dudit registre (RCR) représente une autorisation d'accès de ladite unité centrale de traitement (CPU) dans ledit mode superviseur auxdits moyens de mémoire (11).
- 35 16. Micro-ordinateur selon la revendication 15, dans lequel lesdits troisièmes moyens de commande d'accès incluent des moyens d'évaluation couplés audit registre d'état (SR) et audit registre pour évaluer si l'accès auxdits moyens de mémoire (11) par ladite unité centrale de traitement (CPU) doit être ou non ignoré sur la base à la fois du bit dudit registre d'état (SR) et du bit dudit registre (RCR).
- 40 17. Micro-ordinateur selon la revendication 16, dans lequel ledit micro-ordinateur comprend en outre des moyens de définition d'adresses pour affecter une adresse prédéterminée auxdits moyens de mémoire (11), et dans lequel ladite unité centrale de traitement (CPU) comporte en outre des moyens de production de signaux d'adresses pour produire des signaux d'adresses, et dans lequel lesdits troisièmes moyens de commande d'accès comprennent en outre des moyens comparateurs pour comparer ladite adresse prédéterminée à des signaux d'adresses produits par lesdits moyens de production de signaux d'adresses pour évaluer si ladite unité centrale de traitement (CPU) accède ou non auxdits moyens de mémoire (11).
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