

18. The package assembly of claim 10, wherein the bridge comprises at least one passive signal line coupled to one of the plurality of first contact points and one of the plurality of second contact points.
19. A method of forming a package assembly comprising:
coupling a first die to a package substrate, the package substrate comprising a bridge substrate comprising active device circuitry; and
coupling a second die to the package substrate,
wherein coupling the first die and the second die to the package substrate comprises coupling the first die and the second die to the active circuitry.
20. The method of claim 19, wherein the active device circuitry comprises a repeater.
21. The method of claim 19, wherein the first die is a microprocessor and the second die is at least one memory die and the active circuitry comprises a memory controller.
22. The method of claim 19, wherein the first die is a microprocessor and the second die is a microprocessor.
23. The package substrate of claim 1, wherein the bridge comprises at least one of a transistor or a memory element.
24. The package substrate of claim 1, wherein the bridge comprises one or more through silicon vias (TSVs).
25. The package substrate of claim 1, wherein the bridge comprises a DRAM controller.
26. The package substrate of claim 1, wherein the bridge comprises a semiconductor material.

27. The package assembly of claim 9, wherein the bridge comprises at least one of a transistor or a memory element.
28. The package assembly of claim 9, wherein the bridge comprises one or more through silicon vias (TSVs).
29. The package assembly of claim 9, wherein the bridge comprises a DRAM controller.
30. The package assembly of claim 9, wherein the bridge comprises a semiconductor material.
31. The method of claim 19, further comprising:
forming at least one of a transistor or a memory element in the bridge substrate.
32. The method of claim 19, further comprising:
forming one or more through silicon vias (TSVs) in the bridge substrate.
33. The method of claim 19, further comprising:
forming a DRAM controller in the bridge substrate.
34. The method of claim 19, wherein the bridge substrate comprises a semiconductor material.