Claims

1. A method of encapsulating a substrate having at least the following layers: a CMOS device layer a layer of first semiconductor material different to silicon, and a layer of second semiconductor material, the first semiconductor material being a group III-V semiconductor material or a material formed from combining different group III-V semiconductor materials, the layer of first semiconductor material arranged intermediate the CMOS device layer and the layer of second semiconductor material such that adjoining edges of the layer of first semiconductor material, the CMOS device layer and the layer of second semiconductor material define a circumferential edge of the substrate, the method comprising:

(i) removing a portion of the circumferential edge, the portion removed comprising a portion of the CMOS device layer and a portion of the layer of first semiconductor material; and

(ii) depositing a dielectric material on the substrate to replace the portion removed at step (i) for encapsulating at least the CMOS device layer and the layer of first semiconductor material such that the layer of first semiconductor material is unexposed.

2. The method of claim 1, wherein the group III-V semiconductor material includes GaN, InGaP, AlGaAs, InGaAsP, InGaN, AlGaN, GaAs, Ge, or InGaAs.

3. The method of any preceding claims, wherein the second semiconductor material includes silicon, or a CMOS-compatible material.

4. The method of any preceding claims, wherein the CMOS device layer includes silicon-on-insulator based devices.

5. The method of any preceding claims, wherein removing the portion of the circumferential edge includes using reactive-ion etching, or inductively coupled plasma reactive-ion etching for the removal.

6. The method of claim 5, wherein prior to step (i), the method further comprises:

removably attaching a wafer mask on the CMOS device layer, if reactive-ion etching, or inductively coupled plasma reactive-ion etching is used.

7. The method of claim 6, wherein the wafer mask is formed of silicon.

8. The method of any one of claims 1 to 4, wherein removing the portion of the circumferential edge includes using edge trimming for the removal.

9. The method of any preceding claims, wherein depositing the dielectric material on the substrate includes depositing a layer of the dielectric material on a surface of the CMOS device layer which opposes the layer of first semiconductor material, and is substantially parallel to the horizontal axis of the substrate, further includes:

(iii) planarizing the substrate to at least partially remove the layer of the dielectric material deposited on the surface of the CMOS device layer.

10. The method of claim 9, wherein planarizing the substrate includes using chemical mechanical polishing for the planarization.

11. The method of any preceding claims, wherein the dielectric material is selected from the group consisting of aluminium oxide, aluminium nitride, silicon dioxide, silicon nitride, synthetic diamond and boron nitride.

12. The method of any preceding claims, wherein depositing the dielectric material on the substrate includes using plasma-enhanced chemical vapour deposition for the deposition.

13. The method of claim 9, wherein subsequent to step (iii), further comprises:

(iv) depositing the dielectric material on a surface of the layer of second semiconductor material which opposes the layer of first semiconductor material.

14. The method of claim 9 or 13, wherein subsequent to step (iii) or (iv), further comprises:

(v) annealing the substrate to densify the deposited dielectric material.

15. The method of any preceding claims, wherein removing the portion of the circumferential edge includes partially removing a portion of the edge of the layer of second semiconductor material.

16. The method of claim 6, further comprises:

maintaining attachment of the wafer mask on the CMOS device layer during performance of step (ii).

17. The method of claim 16, further comprises:

removing the wafer mask subsequent to step (i) and prior to step (ii); and

depositing a spin-on glass material as the dielectric material on the substrate in step (ii).

18. A substrate comprising at least the following layers:

a CMOS device layer,

a layer of first semiconductor material different to silicon, and

a layer of second semiconductor material, the first semiconductor material being a group III-V semiconductor material or a material formed from combining different group III-V semiconductor materials, the layer of first semiconductor material arranged intermediate the CMOS device layer and the layer of second semiconductor material such that adjoining edges of the layer of first semiconductor material, the CMOS device layer and the layer of second semiconductor material define a circumferential edge of the substrate,

wherein a portion of the circumferential edge has been removed, the portion removed comprising a portion of the CMOS device layer and a portion of the layer of first semiconductor material; and

a dielectric material deposited on the substrate to replace the portion removed and which encapsulates at least the CMOS device layer and the layer of first semiconductor material such that the layer of first semiconductor material is unexposed.

19. The substrate of claim 18, wherein the second semiconductor material includes silicon, or a CMOS-compatible material.

20. The substrate of claim 18 or 19, wherein the CMOS device layer includes silicon-on-insulator based devices.

21. The substrate of any one of claims 18 to 20, wherein the dielectric material includes a layer of dielectric material deposited on a surface of the CMOS device layer which opposes the layer of first semiconductor material, and is substantially parallel to the horizontal axis of the substrate, and wherein the layer of dielectric material is at least partially removed by planarizing the substrate.