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NOISE REDUCTION CIRCUITS

This invention relates to noise reduction circuits.

5 A known noise reduction circuit comprises a compression circuit at a transmitter for signal compression during transmission, and an expansion circuit at a receiver for signal expansion during signal reception, in order to increase the effective dynamic range of a signal transmission path. This same signal compression and expansion approach has also been applied to recording and reproduction systems, in which a signal is compressed at an input to a recording device and is expanded during reproduction. Typically, these compression and expansion systems include circuits that have a  
10 controllable transfer function, in which the transfer function of the circuit is varied depending upon signal level and/or frequency.

In a known noise reduction circuit of this type described in US Patent No. 3 631 365, the compression circuit of the noise reduction circuit includes a main signal path, an auxiliary signal path, and a summing circuit  
15 for summing the signals of the two paths to produce an output signal. The auxiliary signal path is formed of a high-pass filter having a variable cut-off frequency, a control circuit for controlling the variable cut-off frequency, and an amplitude limiting circuit. An output signal from the high-pass filter is fed to the amplitude limiting circuit through an amplifier, and an output  
20 signal from the amplitude limiting circuit is fed to the summing circuit where it is added to the main path signal. The amplitude limiting circuit comprises reverse parallel connected diodes or a similar arrangement of PN junctions and has an inherent threshold level of approximately  $1.2 V_{p-p}$  for silicon PN junctions. Because this PN junction threshold level is large when compared to the signal levels usually encountered in circuits of this kind, an  
25 amplifier must be connected in the preceding stage of the amplitude limiting circuit so that the high-pass filter output signal level can be substantially greater than the threshold level of the amplitude limiting circuit. Therefore, this amplifier is an essential rather than an incidental component and acts not only as a buffer amplifier for the high-pass filter  
30 but also to set the limiter level. Because the auxiliary signal path output signal, which has been amplified by this amplifier, must be added to the

main signal with only a small weighting factor, additional complicated circuitry is required, which further adversely affects signal precision and stability. In addition, reverse bias or drain currents flowing in the PN junctions of the amplitude limiting circuit adversely affect the remaining circuits in the system because of the common impedance of the ground circuit.

According to the invention there is provided a noise reduction circuit comprising a main signal path, an auxiliary signal path which includes an amplitude limiter and has the characteristics of a high-pass filter having a controllable cut-off frequency, and means for summing an output signal of the main signal path and an output signal of the auxiliary signal path to form a circuit output signal, wherein the auxiliary signal path comprises:

- voltage-to-current converter means having first and second differential inputs and differential outputs;
- PN junction means connected to the differential outputs of the voltage-to-current converter means;
- a first common emitter configuration transistor pair having bases connected to the PN junction means;
- capacitance means connected at one end to the first differential input of the voltage-to-current converter means;
- the capacitance means being connected or connectable at its other end to the main signal path and the second differential input being connected to ground, or the capacitance means being connected at its other end to ground and the second differential input being connected to the main signal path;
- feedback means connecting a collector circuit of the first common emitter transistor pair to the first differential input of the voltage-to-current converter means; and
- a second common emitter configuration transistor pair having bases connected to the PN junction means, whereby said output signal of the auxiliary signal path is derived from a collector circuit of the second common emitter configuration transistor pair.

The invention also provides a noise reduction circuit comprising a main signal path and an auxiliary signal path that includes an amplitude limiter and has a transfer characteristic of a filter with a cut-off frequency variable in response to an output signal of the auxiliary path, the auxiliary path comprising:

a voltage-to-current converter having first and second differential inputs and differential outputs;

PN junction means connected to the differential outputs of the voltage-to-current converter;

5 capacitance means connected at one end to the first differential input of the voltage-to-current converter;

the capacitance means being connected or connectable at its other end to the main signal path and the second differential input being connected to ground, or the capacitance means being connected at its other end to ground  
10 and the second differential input being connected to the main signal path;

a first pair of common emitter configuration transistors having base circuits connected to the PN junction means, an output of the first pair of common emitter configuration transistors being connected to the first differential input of the voltage-to-current converter; and

15 a second pair of common emitter configuration transistors having base circuits connected to the PN junction means, an output of the second pair of common emitter transistors forming the output signal of said auxiliary path.

Further, the invention provides a noise reduction circuit comprising a main signal path and an auxiliary signal path that includes an amplitude  
20 limiter and has a transfer characteristic of a high-pass filter with a cut-off frequency that is variable in response to an output signal of the auxiliary path output signal, the auxiliary path comprising:

voltage-to-current converter means having first and second differential inputs and differential outputs;

25 PN junction means connected to the differential outputs of the voltage-to-current converter means;

capacitance means connected at one end to the first differential input of the voltage-to-current converter;

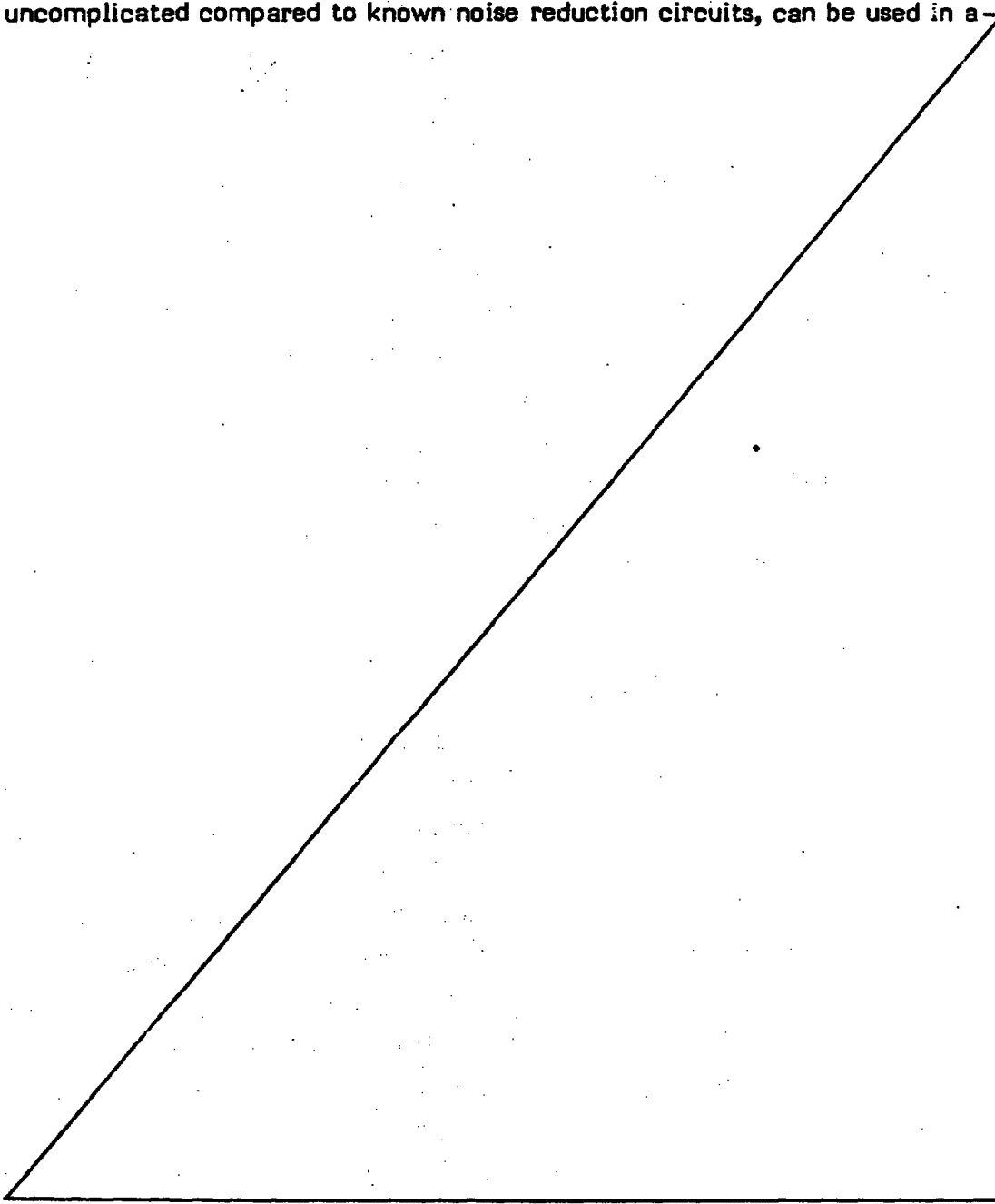
the capacitance means being connected or connectable at its other end to the main signal path and the second differential input being connected to ground, or the capacitance means being connected at its other end to ground  
30 and the second differential input being connected to the main signal path;

a first pair of transistors connected in common emitter configuration and having base circuits connected to the PN junction means, an output of the first pair of common emitter transistors being connected to the first  
35 differential input terminal of the voltage-to-current converter means;

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5 a second pair of transistors connected in common emitter configuration and having base circuits connected to the PN junction means, an output of the second pair of transistors forming an output of the auxiliary signal path; and signal summing means having inputs connected to the main signal path and to the output of the auxiliary signal path for producing a circuit output signal having reduced noise.

Noise reduction circuits embodying the invention can be relatively uncomplicated compared to known noise reduction circuits, can be used in a



signal transmission system that is simple and of high precision and which lends itself to fabrication as an integrated circuit, can be used in a signal transmission system in which the threshold level of the amplitude limiter can be adjusted as necessary without requiring dedicated amplifiers, and can enable adverse effects caused by reverse bias or drain current flowing through the amplitude limiting circuit to be reduced.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which the same references identify the corresponding elements and parts in the several figures, and in which:

Figure 1 is a schematic diagram showing the basic arrangement of a compression circuit of a known noise reduction circuit;

Figure 2 is a plot of the transfer characteristic of the circuit of Figure 1;

Figures 3A and 3B are waveform diagrams of a tone burst signal and the resultant output, respectively, in the circuit of Figure 1;

Figure 4 is a schematic diagram showing the known noise reduction circuit of Figure 1 in more detail;

Figure 5 is a schematic diagram of one embodiment of noise reduction circuit according to the present invention;

Figures 6A and 6B are schematic diagrams of embodiments of voltage-to-current converters for use in the noise reduction circuit of Figure 5;

Figure 7 is a schematic diagram of an embodiment of a current multiplier for use in the circuit of Figure 5;

Figure 8 is a schematic diagram of a filter used in another embodiment of noise reduction circuit according to the present invention;

Figure 9 is a schematic diagram of still another embodiment of noise reduction circuit according to the present invention;

Figure 10 is a schematic diagram of a further embodiment of noise reduction circuit according to the present invention; and

Figure 11 is a schematic diagram showing a modification of a PN junction pair used in embodiments of the present invention.

Figure 1 shows a typical compression circuit known for use in a conventional noise reduction system. The circuit of Figure 1 comprises a main signal path 3 connected between an input terminal 1 and an output

terminal 2, an auxiliary signal path 4, and a summing unit 5. The auxiliary signal path 4 is made up of a high-pass filter 6 having a variable cut-off frequency, a control circuit 7 for controlling the variable cut-off frequency of the high-pass filter 6, and an amplitude limiter 8.

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Figure 2 shows that the transfer function characteristic A of the main signal path 3 has a flat frequency characteristic of constant unity gain, while the transfer function characteristic B of the auxiliary signal path 4 is determined substantially by the transfer function characteristic of the high-pass filter 6. The cut-off frequency of the high-pass filter 6 varies as a function of the input signal level and, thus, the cut-off frequency is lowest for a zero signal level, as shown by a characteristic curve  $B_1$ , and increases with a corresponding increase in signal level, as shown by a characteristic curve  $B_2$ . The transfer function characteristic C between the input terminal 1 and the output terminal 2 of the entire compression circuit of Figure 1 is a combination of the transfer function characteristics A and B of the signal paths 3 and 4, respectively. Curves  $C_1$  and  $C_2$  in Figure 2 represent these combined characteristics for zero signal level and an increased signal level, corresponding to the curves  $B_1$  and  $B_2$ , respectively. The dynamic range of the input signal is compressed by the operation of the circuit of Figure 1; and can be restored to approximately its original value by using an expansion circuit (not shown) during reproduction or reception of a signal recorded or transmitted, respectively, after compression by the circuit of Figure 1. The expansion circuit should have a transfer function characteristic that is complementary to that of the compression circuit. A noise reduction system or circuit with this operating principle is called a sliding band system, because the transfer function characteristic "slides" along the frequency axis.

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In the operation of the noise reduction circuit of Figure 1, if it is assumed that the amplitude limiting circuit 8 is removed and a tone burst signal, as shown in Figure 3A, is supplied for a time interval  $t_1 - t_2$  between instants  $t_1$  and  $t_2$ , then the resultant output signal has a waveform as shown in Figure 3B. Since there is substantially no signal before the time  $t_1$ , the cut-off frequency of the high-pass filter 6 corresponds to the zero signal level curve  $B_1$  in Figure 2. After the time  $t_1$ , the cut-off frequency of the high-pass filter 6 is shifted upwardly by operation of the control circuit 7. Nevertheless, this shifting of the cut-off frequency cannot occur

instantaneously because of the finite rise time constant of the control circuit 7, and this causes an overshoot of the output waveform, which may exceed the clipping level or maximum allowable level inherent in the transmission channel or the recording medium. In order to avoid this overshoot and subsequent clipping, a limiter level L, which is lower than the  
 5      aforementioned clipping level, is set by the amplitude limiting circuit 8. The effects of this limiting circuit are shown in Figure 3B.

Figure 4 shows a known noise reduction circuit that, while operating basically as a compression circuit, can be switched between compression and  
 10      expansion by operation of a changeover switch 11. The input of the auxiliary signal path 4 is connected to a common terminal or contact c of the changeover switch 11, one changeover terminal or contact a of the switch 11 being connected to the input terminal 1 and another changeover terminal or contact b being connected to the output terminal 2. An operational  
 15      amplifier 17 sums the outputs from the signal paths 3 and 4 and is connected to operate as an inverting amplifier, whereby the output signal from the amplifier 17 is supplied to the signal path 4 through the terminal b and is reversed in polarity with respect to the input signal. When the changeover  
 20      switch 11 is switched to the terminal a, to effect signal compression, the signal compression transfer function C(s) between the input terminal 1 and the output terminal 2 may be expressed as:

$$C(s) = -(1 + T(s)) \quad \dots(1)$$

where T(s) represents the transfer function of the auxiliary signal path 4. The gain of the main signal path 3 and that of the summing amplifier (the operational amplifier 17) are selected to be 1 and -1, respectively. When the switch 11 is actuated to connect the terminals b and c, the auxiliary  
 25      signal path 4 provides a negative feedback signal path and the signal expansion transfer function E(s) between the input terminal 1 and the output terminal 2 may be expressed as:  
 30      the signal expansion transfer function E(s) between the input terminal 1 and the output terminal 2 may be expressed as:

$$E(s) = \frac{1}{1 + T(s)} \quad \dots(2)$$

35      In this manner, the circuit accomplishes signal expansion that is complementary to the above-described operation of signal compression.

Referring to Figure 4, the high-pass filter having a variable cut-off frequency is formed by a capacitor 12 and a current-controlled or voltage-controlled variable resistance circuit 13. The output of the high-pass filter is supplied to the control circuit 7 and to the amplitude limiting circuit 8 through an amplifying circuit formed by an operational amplifier 14. The cut-off frequency control circuit 7 is constituted by a weighting circuit 15 that weights the high-frequency signal component and a level sensor 16 that includes a half-wave or full-wave rectifier and a time constant circuit. The output signal from the control circuit 7 controls the resistance value of the variable resistance circuit 13. The amplitude limiting circuit 8 is formed by a pair of reverse parallel connected PN junctions, such as diodes or the like, and has a limiting level appropriate to the particular elements chosen. For instance, a silicon PN junction has a threshold value of approximately 1.2 V<sub>p-p</sub> as a limiter level. Because this value is large compared with the usual design signal level, conventional practice has been to provide an amplifier, such as the operational amplifier 14, ahead of the amplitude limiting circuit 8, whereby the output level of the high-pass filter is raised so that the limiter level will be at an optimum level relative to the signal level. Because of this signal level relationship, the operational amplifier 14 is an essential circuit element, not only as a buffer amplifier for the high-pass filter, but also to set the above-described limiter level. The output signal from the auxiliary signal path 4, amplified by the operational amplifier 14, must also be multiplied by a small factor before it is added to the main signal. These various operations of raising and lowering the signal level result in lowered precision of the signal, with a correspondingly complicated circuit design. There is also a deficiency in these known circuits in that the reverse bias or drain current flowing in the amplitude limiting circuit 8 affects the remaining portions of the circuit through the impedance of the common ground circuit.

Figure 5 shows an embodiment of noise reduction circuit according to the present invention. The circuit of Figure 5 is in many respects like that of Figure 4 and will be described only in so far as it differs therefrom. In the circuit of Figure 5, the main signal path 3, which is a signal transmission line with unity gain, and the auxiliary signal path 4, which includes a high-pass filtering characteristic with variable cut-off frequency, are connected in parallel with each other between the input terminal 1 and the output

terminal 2. The output from the main signal path 3 and the output from the auxiliary signal path 4 are summed by the operational amplifier 17, and the summed signals are supplied to the output terminal 2. Although not shown, the control circuit for varying the cut-off frequency of the high-pass filter in the auxiliary signal path 4 is typically constructed and arranged so that the auxiliary signal path output is sampled, the signal level of the sampled output detected, and the value of the resistance component of the filter circuit portion of the auxiliary signal path is varied depending upon the detected output level.

While the circuit shown in Figure 5 operates principally to provide signal compression, it can also provide signal expansion by operation of the changeover switch 11, whereby the auxiliary signal path 4 acts as a negative feedback path during signal expansion. In that case, however, because the input and output terminals 1 and 2 are in phase with each other, an inverting amplifier 38 of unity gain is connected between the output terminal 2 and the changeover switch 11.

With regard to the auxiliary signal path 4, one terminal of the capacitor 12, which forms part of the high-pass filter with the variable cut-off frequency, is connected to the common terminal C of the changeover switch 11, and the other terminal of the capacitor 12 is connected to a differential input terminal 22 of a voltage-to-current converter 21, which has a differential input terminal pair 22, 23 and a differential output terminal pair 24, 25. The other differential input terminal 23 of the voltage-to-current converter 21 is connected to ground. The differential output terminals 24 and 25 of the voltage-to-current converter 21 are connected to the ends of a PN junction pair 26 formed from two transistors connected as diodes and having their other or cathode ends connected in common.

Also connected, respectively, to the terminals 24 and 25 of the voltage-to-current converter 21 are the base electrodes of a first pair 27 of transistors that are connected in common emitter configuration. A current inverter or current mirror circuit 28 is connected between the collectors of first common emitter transistor pair 27 and the output current therefrom is fed back to the differential input terminal 22 of the voltage-to-current converter 21. A first current source 29 is connected to the common emitters of the first common emitter transistor pair 27. The current flowing in the current source 29 is controlled by the output of the above-described cut-off

frequency control circuit (not shown), through a control input terminal 30.

Thus, looking into the circuit at the terminal 22, the circuit appears as a variable impedance circuit grounded at one end, the variable impedance being dependent upon the current flowing through the current source 29.

5           The bases of a second common emitter transistor pair 33 are connected, respectively, to the output terminals 24 and 25 of the voltage-to-current converter 21, as also are the bases of a third common emitter transistor pair 34, which provides a high-pass filter output to the amplitude limiting circuit 8. Current mirror circuits 31 and 32 are connected as loads to the second and third common emitter transistor pairs 33 and 34, respectively, and second and third current sources 36 and 37 are connected to the common emitters of the transistor pairs 33 and 34, respectively.

10           The output current from the collector circuit of the second common emitter transistor pair 33 is the auxiliary signal path output fed to the amplitude limiting circuit 8 and on to the inverting input of the operational amplifier 17, which functions as the signal path summing means. This auxiliary signal path output is summed in the amplifier 17 with the main signal path output, and the resultant output signal is fed to the output terminal 2. The output of the third common emitter transistor pair 34 is taken off at a terminal 35 to be supplied to the control input terminal 30 through the above-described control circuit (not shown). Terminals 39, 40 designate positive and negative voltage source connections, respectively.

15           The voltage-to-current converter 21 is of the differential input and output kind and may (for example) be configured as shown in Figure 6A or Figure 6B. In Figure 6A, input voltages  $v_1$  and  $v_2$  are applied to the differential input terminals 22 and 23, respectively, which are connected to the bases of respective ones of two PNP transistors. A resistance  $R_0$  is connected between the emitters of the two PNP transistors, and two equal currents  $I_x$  are supplied from the positive voltage source terminal 39 through constant current sources to the junctions between the respective ends of the resistance  $R_0$  and the respective emitters. Under these conditions, the output currents  $i_1$  and  $i_2$  supplied at collector circuit output terminals 24 and 25, respectively, of the pair of PNP transistors are expressed as:

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$$i_1 = I_x - (v_1 - v_2) / R_0 \quad \dots(3)$$

$$i_2 = I_x + (v_1 - v_2) / R_0 \quad \dots(4)$$

Subtracting equation (4) from (3) yields:

$$i_1 - i_2 = - \frac{2}{R_0} \cdot (v_1 - v_2) \quad \dots(5)$$

Thus, the output current difference  $i_1 - i_2$  is proportional to the input voltage difference  $v_1 - v_2$ .

In the circuit shown in Figure 6A, the base-emitter voltage  $V_{BE}$  of each of the two PNP transistors is affected by the changes in the currents. Therefore, for improved accuracy and linearity, the circuit shown in Figure 6B is preferred. In the circuit of Figure 6B, four PNP transistors are connected in a feedback configuration with differential inputs and differential outputs, so that constant currents  $I_D$  flow through a transistor pair forming a differential input stage and, thus, the voltage difference across the resistance  $R_0$  is maintained at  $v_1 - v_2$ , despite any fluctuation in the currents  $i_1$  and  $i_2$ , which flow through a transistor pair forming a differential output stage.

The combination of the PN junction pair 26, which is connected to the differential output terminals 24 and 25 of the voltage-to-current converter 21, with one of the first, second, or third common emitter transistor pairs 27, 33, and 34, respectively, is known as a multiplier circuit. Thus, in a multiplier circuit shown in Figure 7, formed of the PN junction circuit 26 and the common emitter transistor pair 27, the currents  $i_1$  and  $i_2$  flow through PN junctions formed by transistors 26a and 26b, respectively, of the PN junction pair 26, and a current  $2I_x$  flows through the common emitter output circuit. Currents  $i_3$  and  $i_4$  flow through transistors 27a and 27b, respectively, of the transistor pair 27, and a current  $2I_y$  flows through the common emitter output path. Since the PN junction of the transistor 26a has its anode connected to the base of the transistor 27a, and the PN junction of the transistor 26b has its anode connected to the base of the transistor 27b, the currents  $i_3$  and  $i_4$  can be expressed as:

$$i_3 = i_1 \cdot I_y / I_x \quad \dots(6)$$

$$i_4 = i_2 \cdot I_y / I_x \quad \dots(7)$$

When the inputs of the circuit of Figure 7 are connected to the outputs of the voltage-to-current converter 21, such as that shown in either Figure 6A or Figure 6B, the resulting combined circuit is a transconductance circuit, and the currents  $i_3$  and  $i_4$  may be expressed as:

$$i_3 = I_y - (v_1 - v_2) \cdot I_y/I_x \cdot R_0 \quad \dots(8)$$

$$i_4 = I_y + (v_1 - v_2) \cdot I_y/I_x \cdot R_0 \quad \dots(9)$$

By connecting this common emitter transistor pair to a current mirror circuit, the output current  $i_o$  is expressed as the difference between  $i_3$  and  $i_4$  and, thus:

$$\begin{aligned} i_o &= i_3 - i_4 \\ &= 2(v_1 - v_2) \cdot I_y/I_x \cdot R_0 \quad \dots(10) \end{aligned}$$

The current mirror circuits 28, 31, and 32 are connected to the common emitter transistor pairs 27, 33, and 34 of Figure 5, respectively. The output current of the voltage-to-current converter 21 is fed back to the input terminal 22 of the voltage-to-current converter 21, and the output current  $i_g$  of the third common emitter transistor pair 34 is used to derive the control current, as described hereinabove.

With the output signal of the first common emitter transistor pair 27 being fed back to the input terminal 22 of the voltage-to-current converter 21, the impedance viewed from the terminal 22 is equivalent to a resistance that is connected to ground at the other end. The resistance value  $r$  thereof is expressed as:

$$r = \frac{R_0}{2} \cdot \frac{I_x}{I_c} \quad \dots(11)$$

The current  $I_c$  in equation (11) is equivalent to the current  $I_y$  discussed above, since the current  $2I_c$  flows in the first current source 29 connected to the common emitter path of the first transistor pair 27. Assuming that the input and output of the high-pass filter constituted by the resistance  $r$  and capacitor 12 are designated as  $V_i$  and  $V_o$ , respectively, and

are a function of a complex angular frequency, then:

$$V_s = V_i \cdot \frac{Cr}{1 + sCr} \quad \dots(12)$$

Based on equation (12), it can be seen that the circuit displays a primary high-pass characteristic having a pole at  $1/Cr$ , the frequency for this pole being controlled by a current  $I_c$  that is varied by the control signal from the control terminal 30.

If the currents flowing in the second and third current sources 36 and 37, connected respectively to the common emitter paths of the second and third common emitter transistor pairs 33 and 34, are designated  $I_A$  and  $I_B$ , respectively, the functions of complex variables  $I_s$  and  $I_g$  may be written as:

$$I_g = V_s \cdot \frac{2}{R_o} \cdot \frac{I_B}{I_x} \quad \dots(14)$$

It should be noted that the output current  $I_g$  from the second common emitter transistor pair 33 is supplied as an auxiliary signal path output to the inverting input terminal of the operational amplifier 17 through the amplitude limiting circuit 8, with the operational amplifier 17 acting as a signal summing element. A series circuit of two resistors  $R_1$  and  $R_2$  is connected in parallel with the amplitude limiting circuit 8, which comprises two reverse parallel connected diodes, and a junction formed by connecting the circuit 8 and the resistor  $R_1$  is connected to the output of the operational amplifier 17, while the voltage dividing point at the junction of the two resistors  $R_1$  and  $R_2$  is connected to the inverting input terminal of operational amplifier 17, and the junction of the resistor  $R_2$  and circuit 8 is connected to the output of the second common emitter transistor pair 33. For details of the amplitude limiting circuit and the operational amplifier, reference should be made to our copending UK Patent Application No 8236737 (Publication No. GB 2 113 955 A). Since the resistor  $R_1$  provides an auxiliary output signal path, the limiter level of the amplitude limiting circuit 8 (equal to approximately  $1.2 V_{p-p}$  in the case of reverse parallel connected silicon diodes) is multiplied by  $(R_1/R_1 + R_2)$ . Thus, it can be seen that, assuming  $R_2 = 2R_1$ , the amplitude limiting level is lowered to approximately  $0.4 V_{p-p}$ .

In the noise reduction circuit described above, since the auxiliary output signal path is obtained as a current source output, summing the main path and auxiliary path signals together and limiting the amplitude to an optimum level may be effected by the single operational amplifier, thus eliminating the requirement for a buffer operational amplifier (the amplifier 14 of Figure 4) and simplifying the circuit, while increasing circuit accuracy. The operational amplifier 17, because of its straightforward connection as a signal summation element, operates as a perfect voltage follower with respect to the main signal. The operational amplifier 17 and its associated feedback circuitry is low in reverse bias drain current characteristics, while being relatively free from the effects of non-linearity in the resistance of the diffused area in an integrated circuit implementation. Moreover, the circuit gain is accurate and is not dependent on the precision of the resistance values. The reverse bias or drain current flowing through the amplitude limiting circuit 8 does not flow into the grounding circuit, as in known circuits and, thus, it is relatively free from the effects of the common ground circuit impedance.

Figure 8 shows a form of the high-pass filter that can be used to form a portion of another embodiment of the present invention. The high-pass filter of Figure 8 is made up of two capacitors 41 and 42, two resistances 43 and 44, and a feedback circuit, which is formed by the above-described voltage-to-current converter 21 and a multiplier having an equivalent resistance  $r$ . The circuit of Figure 8 has a high-pass filter characteristic with a transfer function having two poles and a zero point. The circuit of Figure 8 is similar in all other respects to the high-pass filter shown in Figure 5.

Figure 9 shows another embodiment of noise reduction circuit according to the present invention that differs from the embodiment described above as regards switching between the compression and expansion modes and in the construction of the high-pass filter. The switching between compression and expansion is effected by changing the connection between an operational amplifier 51 and the main circuit portion that provides the compression capability. When the changeover switch 11 is set to connect the terminals a and c, the operational amplifier 51 acts as a unity gain amplifier or voltage follower, so that the input signal fed to the input terminal 1 is supplied in an unmodified form by the operational

amplifier 51 to an input terminal 52 of the main compression circuit, and the compressed output signal is produced at an output terminal 53. When the switch 11 is set to connect the terminals b and c, the compression circuit is connected as an input to the operational amplifier 51, and the circuit portion between the input terminal 1 and the output terminal 53 then performs signal expansion, which is complementary to the signal compression described hereinabove.

Referring now to the high-pass filter circuit in the embodiment of Figure 9, the equivalent resistance  $r$  formed by the voltage-to-current converter 21, PN junction pair 26, and the first common emitter transistor pair 27 is not connected directly to ground, as in the embodiment of Figure 5, but is floating and is connected to ground only through the capacitor 12. The other end of the capacitor 12 is connected to the differential input 22 of the voltage-to-current converter 21, the other differential input 23 is connected to the main signal path 3, and the output of the first common emitter transistor pair 27 is also connected to the differential input terminal 22 in a feedback circuit configuration. The remaining circuit elements in the embodiment of Figure 9 are similar to those of the embodiment shown in Figure 5.

The embodiment of Figure 9 affords improved performance over the embodiment of Figure 5. For example, in the embodiment of Figure 5 switching between the compression and expansion modes can be accomplished easily by a single changeover switch 11 only when the gain of the main signal path 3 is unity, because the switching arrangement is otherwise complicated. In the embodiment of Figure 9 there is no such constraint and the switching between compression and expansion modes can be realized easily, even when the main signal path 3 has a nonlinear frequency characteristic. Moreover, the inverting amplifier 38 of the embodiment of Figure 5 is eliminated in the embodiment of Figure 9, further simplifying the circuit construction.

Turning now to the circuit elements forming the high-pass filter in the embodiment of Figure 9, only one connection pin is required for connection of the ungrounded terminal of the capacitor 12, so that the number of connection pins required for an integrated circuit implementation is reduced with respect to the embodiment of Figure 5. In addition, it is not necessary for the preceding stage of the voltage-to-current converter 21 to

have a low impedance, because of the high input impedance of the voltage-to-current converter 21 when viewed from the opposite input terminal 23.

Figure 10 shows certain portions only of another embodiment of noise reduction circuit according to the present invention. Since the remaining circuit components are similar to the corresponding parts of the embodiments discussed in detail hereinabove, they are not shown in Figure 10. The embodiment of Figure 10 provides for disengagement of the noise reduction mode of operation and for switching of the limiter level of the amplitude limiting circuit. Thus, in Figure 10, two common emitter transistor pairs 61 and 62 are provided in place of the single common emitter transistor pair 33 of the preceding embodiments. The common emitter transistor pairs 61 and 62 are connected to current inverting or current mirror circuits 63 and 64, respectively. The output currents of the common emitter transistor pairs 61 and 62 are supplied to inputs of first and second amplitude limiting circuits 65 and 66, respectively. A switch 67 is connected between the common emitters of the common emitter transistor pair 34 and the third current source 37. The emitter circuits of the common emitter transistor pairs 61 and 62 are connected to changeover terminals c and e, respectively, of a triple-pole changeover switch 68. A common terminal f of the switch 68 is connected to the second current source 36, and the remaining switch terminal d is open. The resistors  $R_1$  and  $R_2$  are connected in series and the combination is arranged in parallel with a first amplitude limiting circuit 65, and another resistor  $R_3$  is connected to the resistors  $R_1$  and  $R_2$  with the series combination of all three resistors being connected in parallel with the second amplitude limiting circuit 66. One end of the resistor  $R_1$  is connected to the output of the operational amplifier 17, and the inverting input of the operational amplifier 17 is connected to the voltage dividing point at the junction between the resistors  $R_1$  and  $R_2$ . The output current of the common emitter transistor pair 61 is supplied to the junction of the resistors  $R_2$  and  $R_3$  and the amplitude limiting circuit 65, while the output current of the common emitter transistor pair 62 is supplied to the junction between one end of the resistor  $R_3$  and the amplitude limiting circuit 66.

In the embodiment of Figure 10, with the switch 67 open and the changeover switch 68 set to the terminal d (also open), the common emitter transistor pairs 34, 61 and 62 are turned off, thereby disengaging the noise

reduction mode of operation and all signal flow is through the main signal path. With the switch 67 open and the switch 68 actuated to connect either the terminals c and f or the terminals e and f, the noise reduction mode is engaged and the limiting level is set to a higher or lower value, depending on whether the switch 68 is actuated to contact the terminal c or e, respectively. In this manner, engaging or disengaging the noise reduction mode or switching the limiter level is easily achieved.

Figure 11 shows a modification of the PN junction pair 26 employed in the embodiments described above. The arrangement of Figure 11 comprises NPN transistors 71 and 72, the collectors of which are connected to the output terminals 24 and 25, respectively, of the voltage-to-current converter 21. The transistors 71 and 72 act as current inverting or current mirror circuits in cooperation, respectively, with transistors 73 and 74 connected in diode configuration. The bases of the transistors 71 and 72 are connected, respectively, to the emitters of transistors 75 and 76, which are connected in emitter follower configuration, and which are also connected to output terminals 77 and 78. The output terminals 77 and 78 correspond to connections to the bases of the common emitter transistor pairs 27, 33 and 34 described above. The bases of the transistors 75 and 76 of the PN junction circuit of Figure 11 are connected to the collectors of the transistors 71 and 72 respectively, of the PN junction pair 26.

In the circuit arrangement of Figure 11, the transistors 75 and 76, which are connected as emitter followers, are equivalent in operation to the PN junction pair discussed above in connection with Figure 7, because the transistors provide a feedback path through which the output currents  $i_1$  and  $i_2$  of the voltage-to-current converter 21 are counterbalanced with the collector currents of the transistors 71 and 72. In the circuit of Figure 11, the effects on circuit performance of the increased base current supplied to the common emitter transistor pairs connected to the output terminals 77 and 78 are negligible, because such base currents are supplied through the transistors 75 and 76, which are connected in emitter follower configuration. The transistors 73 and 74, which are connected as diodes, and which act to control the bias current of transistors 73 and 74, may be replaced by resistors of appropriate value.

In the noise reduction circuits shown in the drawings and described hereinabove, the auxiliary signal path current is taken as a current source

output and, thus, the summing of the auxiliary signal and the main signal and limiting the signal amplitude can be achieved by a single operational amplifier, without requiring a buffer amplifier as in the heretofore known noise reduction circuits. In an integrated circuit implementation, since the signal summing device acts as a perfect voltage follower with respect to the main signal, it is not affected by any non-linear resistance of the diffused area in the integrated circuit structure and it is also low in reverse bias drain current characteristics. Moreover, the circuit has a high gain so that it is not affected by variations in resistance values. The effects of the common ground impedance are minimized because the drain current flowing in the amplitude limiting circuit does not flow into the common ground circuit. In addition, switching of the noise reduction mode and the limiter level can be carried into effect very easily.

CLAIMS

1. A noise reduction circuit comprising a main signal path, an auxiliary signal path which includes an amplitude limiter and has the characteristics of a high-pass filter having a controllable cut-off frequency, and means for summing an output signal of the main signal path and an output signal of the auxiliary signal path to form a circuit output signal, wherein the auxiliary signal path comprises:

voltage-to-current converter means having first and second differential inputs and differential outputs;

PN junction means connected to the differential outputs of the voltage-to-current converter means;

a first common emitter configuration transistor pair having bases connected to the PN junction means;

capacitance means connected at one end to the first differential input of the voltage-to-current converter means;

the capacitance means being connected or connectable at its other end to the main signal path and the second differential input being connected to ground, or the capacitance means being connected at its other end to ground and the second differential input being connected to the main signal path;

feedback means connecting a collector circuit of the first common emitter transistor pair to the first differential input of the voltage-to-current converter means; and

a second common emitter configuration transistor pair having bases connected to the PN junction means, whereby said output signal of the auxiliary signal path is derived from a collector circuit of the second common emitter configuration transistor pair.

2. A noise reduction circuit according to claim 1, wherein the second differential input of the voltage-to-current converter means is connected to ground, and means is provided for selectively connecting the capacitance means to the main signal path.

3. A noise reduction circuit according to claim 1, in which the capacitance means is connected between the first differential input of the voltage-to-current converter means and ground, and the main signal path is



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connected to a second differential input of the voltage-to-current converter means.

5 4. A noise reduction circuit according to claim 1, wherein a feedback resistance means is connected between an output of the summing means and an inverting input of the summing means, an output of the second common emitter transistor pair is connected to be fed to the inverting input of the summing means, and the main signal path is connected to a non-inverting input of said summing means.

10 5. A noise reduction circuit according to claim 1, wherein the PN junction means is formed by a pair of transistors each having a base and a collector thereof connected together, emitters of the transistors of the PN junction means being connected in common.

15 6. A noise reduction circuit according to claim 1, wherein the PN junction means is formed by first and second pairs of transistors, each said pair has emitters connected in common, collectors of each of the first and second pairs of transistors are connected to the differential outputs of the voltage-to-current converter means and to base electrodes of fifth and sixth transistors, and bases of each of the first and second pairs of transistors are connected to emitters of the fifth and sixth transistors.

20 7. A noise reduction circuit according to claim 1, wherein a control circuit is provided for controlling the cut-off frequency of the high-pass filter and current control means is responsive to said control circuit for controlling the emitter current of said first common emitter transistor pair.

25 8. A noise reduction circuit comprising a main signal path and an auxiliary signal path that includes an amplitude limiter and has a transfer characteristic of a filter with a cut-off frequency variable in response to an output signal of the auxiliary path, the auxiliary path comprising:  
a voltage-to-current converter having first and second differential inputs and differential outputs;  
30 PN junction means connected to the differential outputs of the voltage-to-current converter;

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capacitance means connected at one end to the first differential input of the voltage-to-current converter;

the capacitance means being connected or connectable at its other end to the main signal path and the second differential input being connected to ground, or the capacitance means being connected at its other end to ground and the second differential input being connected to the main signal path;

a first pair of common emitter configuration transistors having base circuits connected to the PN junction means, an output of the first pair of common emitter configuration transistors being connected to the first differential input of the voltage-to-current converter; and

a second pair of common emitter configuration transistors having base circuits connected to the PN junction means, an output of the second pair of common emitter transistors forming the output signal of said auxiliary path.

9. A noise reduction circuit according to claim 8, wherein means is provided to produce a control signal responsive to the output signal of the auxiliary signal path to vary the cut-off frequency, and which includes means for controlling the current flowing in the common emitter circuit of the first pair of common emitter configuration transistors in response to said control signal.

10. A noise reduction circuit according to claim 8, comprising switch means connected to an input of the main signal path and to the capacitance means for selectively connecting the first differential input of the voltage-to-current converter through the capacitance means to the input of the main signal path.

11. A noise reduction circuit according to claim 10, comprising signal inverter means connected to receive a sum of output signals of the main signal path and the auxiliary signal path for producing an inverted feedback signal to be fed to said switch means, whereby said inverted feedback signal can be selectively connected to the capacitance means.

12. A noise reduction circuit according to claim 8, comprising a current mirror circuit connected across collector circuits of the first pair of common emitter configuration transistors.



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13. A noise reduction circuit according to claim 8, wherein the PN junction means is formed by a pair of common emitter configuration transistors each having its base circuit connected to its collector circuit, the emitter circuits of said transistors forming the PN junction means being connected together.

14. A noise reduction circuit according to claim 13, wherein the pair of common emitter configuration transistors forming the PN junction means comprises first and second pairs of transistors, each said pair of transistors has emitter electrodes connected in common, collector electrodes of each of the first and second pairs of transistors are connected to the outputs of the voltage-to-current converter and to bases of fifth and sixth transistors, and bases of each of the first and second pairs of transistors are connected to emitters of the fifth and sixth transistors.

15. A noise reduction circuit according to claim 8, wherein the capacitance means is connected between the first differential input of the voltage-to-current converter and ground, and the second differential input of the voltage-to-current converter is connected to said main signal path.

16. A noise reduction circuit according to claim 15, comprising means connected to sum output signals of the main and auxiliary signal paths, operational amplifier means having the main signal path connected to a non-inverting input thereof, and switch means connected to receive the summed output signals of the main signal path and the auxiliary signal path, the switch means also being connected to an output of the operational amplifier means and to an inverting input of the operational amplifier means for selectively connecting the inverting input either to receive the summed signals or to the output of the operational amplifier means.

17. A noise reduction circuit comprising a main signal path and an auxiliary signal path that includes an amplitude limiter and has a transfer characteristic of a high-pass filter with a cut-off frequency that is variable in response to an output signal of the auxiliary path output signal, the auxiliary path comprising:  
voltage-to-current converter means having first and second differential inputs and differential outputs;



PN junction means connected to the differential outputs of the voltage-to-current converter means;  
capacitance means connected at one end to the first differential input of the voltage-to-current converter;  
5 the capacitance means being connected or connectable at its other end to the main signal path and the second differential input being connected to ground, or the capacitance means being connected at its other end to ground and the second differential input being connected to the main signal path;  
a first pair of transistors connected in common emitter configuration and  
10 having base circuits connected to the PN junction means, an output of the first pair of common emitter transistors being connected to the first differential input terminal of the voltage-to-current converter means;  
a second pair of transistors connected in common emitter configuration and having base circuits connected to the PN junction means, an output of the  
15 second pair of transistors forming an output of the auxiliary signal path; and  
signal summing means having inputs connected to the main signal path and to the output of the auxiliary signal path for producing a circuit output signal having reduced noise.

18. A noise reduction circuit according to claim 17, comprising means  
20 responsive to the output signal of the auxiliary signal path for providing a control signal, and means for varying the cut-off frequency of the high-pass filter, including means for controlling the current flowing in the common emitter circuit of the first pair of transistors in response to said control signal.

25 19. A noise reduction circuit according to claim 17, comprising switch means connected to the main signal path and to the capacitance means for selectively connecting the first differential input of the voltage-to-current converter means through the capacitance means to the main signal path.

30 20. A noise reduction circuit according to claim 19, comprising signal inverter means connected to receive said circuit output signal and connected to the auxiliary signal path for producing an inverted feedback signal to be fed to said switch means, whereby the capacitance means can be selectively connected to the main signal path or to receive the inverted feedback signal.



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21. A noise reduction circuit according to claim 17, wherein the PN junction means is formed by a third pair of transistors each having its base circuit connected to its collector circuit, the emitters circuits of the third pair of transistors being connected together.

5 22. A noise reduction circuit according to claim 17, wherein the PN junction means comprises fourth and fifth pairs of transistors, each of the fourth and fifth pairs has emitters connected in common, the collectors of each of the fourth and fifth pairs of transistors are connected to the output of the voltage-to-current converter means and to bases of a sixth pair of  
10 transistors, and bases of each of the fourth and fifth pairs of transistors are connected to emitters of the sixth pair of transistors.

23. A noise reduction circuit according to claim 17, wherein the capacitance means is connected between the first differential input of the voltage-to-current converter means and ground, and the second differential  
15 input of the voltage-to-current converter is connected to the main signal path.

24. A noise reduction circuit according to claim 17, comprising operational amplifier means having said main signal path connected to a non-inverting input thereof, and switch means connected to receive said  
20 circuit output signal and connected to an output of said operational amplifier means and to an inverting input of the operational amplifier means for selectively connecting the inverted input either to receive the circuit output signal or to the output of the operational amplifier means.

25. A noise reduction circuit substantially as hereinbefore described with  
25 reference to any one of Figures 5 to 11 of the accompanying drawings.

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