

The invention is a television device with separate processing of luminance signal and colour signals according to the preamble of the claim 1.

In such devices usually the luminance signal has a higher band width - approximately 5 - 8 MHz - than the colour signals - approximately 1 MHz. This results in the luminance signal having a lower transit time within the circuit than the colour signals. For picture reproduction however, the correct temporal synchronization of luminance signal and colour signals must be guaranteed again. Therefore, it is necessary to provide for a compensation of transit time within the path of the luminance signal. For this, an additional transit time line with a transit time in the range of 300 - 500 ns is required. This problem occurs, for example, in television devices, video recorders, camcorders, cameras, standard converters, and picture memories.

Television devices of the type described have a steadily increasing band width of the luminance signal, particularly for HDTV systems with increased picture frequency or line frequency. In addition, the colour signals are processed in separate stages with a band width reduced in relation to the luminance signal. This increased difference in the band width of the luminance signal and the colour signals leads, considering the necessary transit time compensation, to delay devices with increased band width and increased delay time so that the outlay for this transit time compensation rises.

Basis for the invention is the object to reduce the circuitry outlay for the adaptation of the transit time of the luminance signal to the higher transit time of the colour signals.

This task is solved by the invention given in the claim 1. Advantageous further developments of the invention are given in the subclaims.

The invention is based on the following consideration. For the required adaptation of the transit time it is not strictly necessary to delay the luminance signal. The transit time compensation can also be achieved by speeding up the colour signals by an amount corresponding to the transit time difference to be compensated. An acceleration, i.e. an advance in time, of a signal initially appears to be impossible, however. The digital memories used anyway, however, render it possible to read out the colour signals in a manner accelerated by a defined time as against the luminance signal. Such an acceleration of the colour signals is equivalent to the delay of the luminance signal required as such. The memories which are used anyway for other purposes are thus utilized in an advantageous way for the required transit time compensation. The prior required discrete transit time element in the path of the luminance signal in the form of a transit time line, a coil, or a CCD circuit is now no longer necessary. By using CCD lines the invention can also be applied in all prior devices operating in a purely analog manner.

The advantage of the omission of the delay stage in the path of the luminance signal is particularly important with a luminance signal with an increased band width of 8 - 10 MHz for high definition systems and with strong differences in the band width of the luminance signal and the colour signals leading to high differences in transit time.

Subsequently, the invention is described by means of the drawing for a system with digitized luminance signals and colour signals. It shows in:

Fig.1 a block circuit diagram for the processing of luminance signal and colour signals,

Fig.2 a pulse diagram for illustrating the mode of operation of Fig.1, and

Fig.3 a complete circuit for the block circuit diagram of Fig.1.

In Fig.1 the luminance signal Y is fed, via the analog-to-digital converter 1, to the digital memory M1 which, via the digital-to-analog converter 2, supplies the luminance signal Y in another time scale. The colour difference signals B-Y is fed, via the analog-to-digital converter 3, to the digital memory M2 which, via the digital-to-analog converter 4 supplies the colour difference signal B-Y in a changed time scale. Accordingly, the colour difference signal B-Y, via the analog-to-digital converter 5, reaches the digital memory M3 which, via the digital-to-analog converter 6 supplies the correspondingly modified colour difference signal R-Y. The memories M1, M2, M3 are controlled by the logic 7 which, *inter alia*, contains sync pulse separation stages for the control of the shown memories and converters.

The memories M2, M3 are read out by the logic 7 during the vertical blanking period at an increased clock rate.

Hereby, the colour difference signals B-Y and R-Y at the outputs of the converters 4, 6 are accelerated as against the luminance signal Y at the output of the digital-to-analog converter 2. This acceleration corresponds to the transit time difference appearing as such between Y on the one hand and B-Y and R-Y on the other hand. This transit time difference is therefore compensated so that the signals Y, B-Y and R-Y at the output correlate in time. A separate transit time element in the path of Y is not required.

The circuit according to Fig.1 represents a picture memory which carries out an up-conversion between a system with a picture frequency of 50 Hz and a line frequency of 16 kHz by doubling the clock pulse to a system with a picture frequency of 100 Hz and a line frequency of 32 kHz whereby all output signals are doubled in frequency. The memories M1, M2, M3 are 1 Mbit video

memories which are organized as FIFOs. The information is written into the memories M1, M2, M3 always during a field (20 ms) at a clock pulse frequency of 12.5 MHz. For the reading out a quartz clock pulse is applied having twice the frequency, i.e. 25 MHz.

In Fig.2 the indications mean

- BO the reset signal for the memories M1, M2, M3,
- B1 the clock pulse for the memory M1 for Y,
- B2 the normal clock pulse for the memories M2, M3 for the colour difference signals. Hereby, B2 is the signal B1 divided in its frequency by 2,
- B3 the switching signal for the clock pulse acceleration for the colour signals which is generated after execution of the reset signal, and
- B4 the clock pulse for the memories M2, M3 for the colour difference signals. The temporary interleave of the higher frequency clock pulses B4s during the 'high time' of B3 can be seen.

Upon the reading out the memories M2, M3 are reset at the beginning of the vertical sync pulse which is derived from the reproduced signal Y through the pulse separation. Following this reset impulse the clock pulse B4s shown which is doubled in its frequency is applied to the memories M2, M3 for a short period of time.

Fig.3 shows the complete circuit. The flip-flop HC112 is switched into its active state $Q = H$ by means of the negative edge of BO. At the same time the programmable counter HC161 at its pin 9 is pre-set to a value selected by means of the switches S1 through S4. With every clock pulse at the pin 2 the counter state is decremented until on 0 an overflow impulse appears at the pin 15. This impulse flips the flip-flop HC112 over to the inactive state $Q = L$. By means of the output signals of the flip-flop HC112 the component HC125/II is directly triggered which operates as multiplexer and selects one of the two

clock pulses.



Patent Claims

1. Television device with separate processing of luminance signal (Y) and colour signals (B-Y, R-Y) in which the signals are written into memories (M) and read out and a relative delay of the luminance signal as against the colour signals occur for the purpose of transit time compensation, characterized in that the relative delay of the luminance signal (Y) occurs in that the colour signals (R-Y, B-Y) are read out from the memories (M2, M3) at an increased speed during a time period which is not visible in the picture.
2. Television device according to claim 1, characterized in that the reading out at increased speed occurs during the line and/or vertical blanking interval.
3. Television device according to claim 1, characterized in that an impulse is derived from the vertical sync pulse which temporarily increases the reading out clock pulse (B4) for the colour signals (B-Y, R-Y) (B4s in Fig.2).
4. Television device according to claim 1, characterized in that the read out clock pulse (B4) for the memories (M2, M3) for the colour signals (R-Y, B-Y) is temporarily doubled (Fig.2).