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PACKAGE MARKING

The present invention relates to apparatus and a method for marking a semiconductor chip device with some form of identification mark.

Generally semiconductor chip devices (for example chip scale packages (CSP) or SRAM packages) are encapsulated in some form of plastic package which may have a "device type" or "date code" marking on it. A typical marking method uses a laser beam to mark the chip device. Due to improvements in semiconductor chip device technology which have resulted in semiconductor chip devices becoming smaller, maintaining positional accuracy for any marking done on such a semiconductor chip device has become critical. This is because accurate marking is necessary in order to achieve a cosmetically pleasing appearance and to maintain the quality of the chip device marked.

Some prior art arrangements are shown in the accompanying Figures 1A-1D. Figure 1A shows one method which has previously been used to precisely mark a CSP device. A number of chip devices 10, which are typically cubic in shape, are loaded into a tray 11 which is divided into an array of compartments 12 which are larger than the chip devices. Each compartment may hold only one chip device and the chip devices are loaded into the compartments by a robotic handler (not shown). The reason each tray compartment is bigger than the chip device is to prevent physical damage to the device during picking and placing the devices into the tray 11. A laser 13 is situated close to the tray and the laser head fires a laser beam which can be directed to mark each of the chip devices.

Due to the fact that the tray compartments are larger than the device dimensions, each chip device will be randomly positioned within each compartment. Due to the randomly positioned devices the laser mark 15, produced on each device 10 will vary from device to device as shown in Figure 1B.

A known improved method of marking the chip devices is shown in Figure 1C. In this method the tray 11, supporting a number of chip devices 10 each located in a respective compartment 12 of the tray, is tilted through an angle θ. As a result each device moves under gravity to abut with two adjacent edges 16, 17 of the tray compartment which form a corner 18 of the compartment in which the device is contained. The tray is then carefully returned to the upright resting position as shown in Figure 1A. The laser 13 is then operated to fire a laser beam to mark each device. Because the chip devices have each been aligned with a respective corner of each compartment the marks produced by the laser beam will tend to mark the devices without having the marking drift described hereinabove and as shown in Figure 1B.

However a small proportion (for example 5%) of the chip devices will still be inaccurately marked due to the fact that all the devices may not be accurately aligned in a desired location. One reason for this is that during tilting of the tray some chip devices will not budge due to insufficient tray tilt or a rough tray compartment which prevents the device moving to abut with the corner 18 of the compartment. Alternatively due to excessive tilt or vibration during tilting some chip devices will jump partially outside the tray compartment causing misalignment with the compartment edges 16,17.

A further known improvement overcomes this problem. As shown in Figure 1D a camera 19 is provided, near to the laser head 13, which looks at the actual physical position of each chip device in turn before the device is marked by the laser beam. Although this process of marking eliminates the problem of variation in the laser mark put on each device the output rate of number of devices marked in a given time is substantially reduced (perhaps by some 50%) due to the fact that the camera must inspect each device in each tray compartment in turn one after another. This greatly increases the inspection time.

It is therefore an object of the present invention to provide a

method and apparatus for accurately marking semiconductor chip devices which provides a high yield of correctly marked devices whilst the output of number of devices per unit time remains high.

According to the present invention there is provided marking apparatus for marking a plurality of semiconductor chip devices which apparatus comprises a support device for holding simultaneously a plurality of chip devices in a required spatial arrangement, an optical inspection device to view simultaneously a plurality of chip devices on said support device within a predetermined field of view and provide an output indicating positions at which chip devices have been located within said field of view, comparator means to compare said output with predetermined data indicating desired locations for each chip device within said field of view, and a marking device operable in response to a control signal from said comparator means to mark selectively those chip devices within the field of view which have positions corresponding to said desired locations.

Preferably said comparator means has a grid generator to generate a grid pattern including desired locations in which a chip device may be selected for marking.

Conveniently said grid pattern is arranged to cover said predetermined field of view of the optical inspection device.

Advantageously said support device comprises a tray having an array of locating compartments each arranged to receive one chip device, each compartment being oversized in relation to the respective chip device size.

According to the present invention there is also provided a method for marking a plurality of semiconductor chip devices which comprises the steps of loading said chip devices onto a support device in a required spatial arrangement, operating an optical inspection device to view simultaneously a plurality of

the chip devices within a predetermined field of view, generating an output from the inspection device indicating positions at which chip devices have been located within said field of view, comparing said output with predetermined data indicating desired locations for each chip device within said field of view, selecting those chip devices within the field of view which have locations corresponding to said desired locations, and operating a marking device to mark the selected chip device.

Preferably said comparator compares said output with said predetermined data for each chip device within said field of view simultaneously.

Conveniently said step of operating the optical inspection device comprises the step of locating the inspection device in a first position, simultaneously viewing a plurality of said plurality of chip devices within a predetermined field of view and locating said inspection device in a second remote position while marking is effected.

Advantageously said loading into a support device comprises loading a respective one of said chip devices into a rectangular locating compartment of a support device providing an array of compartments whilst said support device is in a first position, tilting the support device to a second position in which each chip device is urged towards a desired location abutting a predetermined corner of the respective compartment, and returning said support device to said first position without substantially altering the location of each chip device prior to effecting the optical inspection.

Preferably said predetermined data comprises generating a grid pattern indicating an array of desired locations in which a chip device may be selected for marking.

Conveniently the grid size is selectable to vary the tolerance of desired locations for chip devices to be marked.

An embodiment of the present invention will now be described hereinbelow by way of example only with reference to the accompanying drawings in which:

Figure 1A illustrates part of an apparatus used to mark chip devices as is known in the prior art.

Figure 1B illustrates an example of how chip devices may be inaccurately marked using prior art techniques.

Figure 1C illustrates a step in an improved method of marking chip devices in accordance with the prior art.

Figure 1D illustrates a further apparatus used in the prior art.

Figure 2 illustrates an apparatus used in accordance with the present invention.

Figure 3 illustrates a tilting step in accordance with the present invention.

Figure 4 illustrates a view of chip devices in accordance with the present invention.

Figure 5 illustrates a grid pattern in accordance with the present invention.

In the drawings like reference numerals refer to like parts.

Figure 2 shows how a number of semiconductor chip devices 20, which are substantially cubic in shape, may be loaded into a tray 21. The tray is rectangular and is divided into twelve equally sized rectangular compartments 22. Each compartment 22 is large enough to receive only one chip device 20. The dimensions of the compartments 22 are however oversized in relation to the chip devices 20 to ensure that when each device is loaded into its respective compartment by a handler (not shown) the device is not

damaged. In this way twelve devices may be supported in the tray each device being located in a respective one of the compartments 22.

A laser having a laser head 23 is provided near to the tray. The laser may be operated to provide a laser beam which may be directed to hit any one of the chip devices in the tray thereby marking the device.

A camera 24 is arranged near to the tray 21. The camera may be moved from a remote position (shown in broken lines) to a viewing position (shown in full lines). Whilst in the remote position the camera is withdrawn out of the way of the laser beam to enable the laser to mark packages. Whilst in the viewing position the camera is operable to view a portion of the tray as will be described hereinafter. Whilst the camera is in the remote position the laser may be operated.

As the chip devices which are loaded into the compartments of the support tray will be randomly positioned in each compartment the tray is tilted through a small angle θ which is sufficiently large to enable the force of gravity to urge each chip device into a desired location in which it abuts a locating corner of the compartment 22 in which it is contained. This step is shown in Figure 3.

As a result each device 20 tends to align itself with a respective locating corner 25 of the compartment and each device 20 is therefore substantially aligned in the same location in each compartment 22.

The tray 21 may then be carefully returned to the resting position. This step must be carried out sufficiently smoothly and slowly so that no sudden jerks cause the chip devices to move from their aligned location.

The tray 21 is returned to its resting position of Figure 2 after

the alignment step of Figure 3. Although the tilting step aligns substantially all of the chip devices 20 some will not be aligned for the reasons set out above.

After returning the tray 21 to the resting position the camera 24 is extended to move from the remote position to the viewing position as shown in solid lines in Figure 2. In this position the camera may be operated to view a part of the container tray 21. For example in Figure 2 the field of view of the camera covers the top half of the tray which contains six locating compartments 22 each of which holds a chip device 20 and all six are thereby optically inspected simultaneously.

An example of one view 30 so captured by the camera is shown in Figure 4. The view is processed so that details of the support tray 21 are minimised and includes details of the four edges of each rectangular compartment which in this example form a square. Likewise each device 20 is viewed as a square 27 with the position of each square 27 within each of the larger squares formed by the edges 26 of the compartment 22 determining the actual position of the chip device within each locating compartment of the support tray 21.

The view 30 produced by the camera generates an output which is then processed using a microcomputer and suitable software (for example Microsoft C++) by comparing the captured view with a grid pattern 31 as shown in Figure 5.

The grid pattern 31 may be generated by vision software operating the microcomputer and is in the form of a grid which covers the field of view 30 of the camera and has row and column dimensions which are preset according to the size and shape of each compartment 22, the size and shape of each device 20 and the tolerance or accuracy with which it is desired to mark each device with the laser beam.

The grid pattern includes an area 32 in each compartment which,

if the device 20 is positioned within the area, indicates that the device is correctly positioned.

The grid pattern 31 and view 30 captured by the camera 33 are initially superimposed(for example the grid pattern 31 is superimposed over the captured image 30) and aligned by aligning check points 33 on the view 30 with row and column intersections on the grid. In this example the check points 33 are selected as upper left hand corners of each compartment 22.

A comparison is thereafter made to establish whether the square 27 illustrating the position of a chip device 20 falls within the area 32 which indicates a desired location for the chip device. If it does the device is selected as correctly positioned. If the square 27 indicating the actual position of a device 20 does not fall within the desired area 32 (for example as may be seen by the parts 34 of the square shown in Figure 5). The devices are not correctly positioned and that chip device will not be selected to be marked by the laser.

The size of the area 32 (that is the spacing of the row lines and column lines of the grid) for the grid may be variably set to control the tolerance or accuracy which is required for the marks made on the chip devices. For example if it is essential that the marks appear on each chip device in absolutely identical positions the area will be set to be the size of each chip 20. In this way if the device is not exactly positioned the square 27 in the camera image will not fall within the preset area 32 and the device will not be selected for marking.

On the other hand if marking is not so critical the grid squares 32 may be made larger (although smaller than the size of the compartments) allowing the chip devices to be slightly misaligned but still selected to be marked.

In the example shown in Figures 4 and 5 four of the devices fall within the preset areas 32 and could therefore be marked.

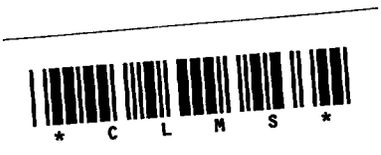
After capturing the view 30 the camera is returned to the withdrawn remote position and details of which chip devices are to be marked will be communicated to the laser. Thereafter the laser will mark the devices 20 which have been selected as being correctly positioned.

The tray 21 will then be moved by a robotic handler (not shown) so that a remaining portion of the tray, which has not been viewed by the camera, will be visible to the camera when it is extended. In the present invention the tray will be moved to allow the lower half of the tray to be visible to the camera. With the present invention there is no chance of marking semiconductor chip devices incorrectly thereby producing a 100% yield. Furthermore the output number of marked devices is substantially increased.

For example taking a tray containing typical SRAM devices and having twelve tray columns and twelve tray rows the prior art method explained with respect to Figure 1D, which inspects only one compartment at a time, will take typically 0.2 seconds to inspect each compartment and therefore 12 x 12 x 0.2 = 28.8 seconds to inspect a tray.

On the other hand the present invention operates with a camera which can inspect more than one locating compartment at a time (for example 3 columns x 3 rows) which will inspect the whole tray in (12 x 12 x 0.2) ÷ 9 = 3.2 seconds which is approximately 90% faster than the prior art method.

The invention is not limited to the details of the example above. For instance, the "chip device" could be a chip scale package (CSP), a ball grid array (BGA) package, a plastic ball grid array (PBGA) package or any other form of semiconductor chip device.



CLAIMS:

1. Marking apparatus for marking a plurality of semiconductor chip devices which apparatus comprises a support device for holding simultaneously a plurality of chip devices in a required spatial arrangement, an optical inspection device to view simultaneously a plurality of chip devices on said support device within a predetermined field of view and provide an output indicating positions at which chip devices have been located within said field of view, comparator means to compare said output with predetermined data indicating desired locations for each chip device within said field of view, and a marking device operable in response to a control signal from said comparator means to mark selectively those chip devices within the field of view which have positions corresponding to said desired locations.

2. Marking apparatus according to claim 1 wherein said comparator means has a grid generator to generate a grid pattern including desired locations in which a chip device may be selected for marking.

3. Marking apparatus according to claim 1 or 2 in which said grid pattern is arranged to cover said predetermined field of view of the optical inspection device.

4. Marking apparatus according to any one of claims 1 to 3 in which said marking device comprises a laser.

5. Marking apparatus according to any one of claims 1 to 4 in which said optical inspection device comprises a camera.

6. Marking apparatus according to any preceding claim in which said support device comprises a tray having an array of locating compartments each arranged to receive one chip device, each compartment being oversized in relation to the respective chip device size.

7. Marking apparatus according to claim 6 in which each compartment is rectangular with a locating corner to which a chip device may abut when in a desired location.

8. Marking apparatus according to claim 6 or 7 in which tilting means are provided to tilt the tray and thereby urge each chip device into a desired location abutting a respective locating corner of the compartment.

9. A method for marking a plurality of semiconductor chip devices which comprises the steps of loading said chip devices onto a support device in a required spatial arrangement, operating an optical inspection device to view simultaneously a plurality of the chip devices within a predetermined field of view, generating an output from the inspection device indicating positions at which chip devices have been located within said field of view, comparing said output with predetermined data indicating desired locations for each chip device within said field of view, selecting those chip devices within the field of view which have locations corresponding to said desired locations, and operating a marking device to mark the selected chip device.

10. A method according to claim 9 wherein said comparator compares said output with said predetermined data for each chip device within said field of view simultaneously.

11. A method according to claim 9 or 10 wherein said step of operating the optical inspection device comprises the step of locating the inspection device in a first position, simultaneously viewing a plurality of said plurality of chip devices within a predetermined field of view and locating said inspection device in a second remote position while marking is effected.

12. A method according to any one of claims 9 to 11 wherein said loading onto a support device comprises loading a respective one

of said chip devices into a rectangular locating compartment of a support device providing an array of compartments whilst said support device is in a first position, tilting the support device to a second position in which each chip device is urged towards a desired location abutting a predetermined corner of the respective compartment, and returning said support device to said first position without substantially altering the location of each chip device prior to effecting the optical inspection.

13. A method according to any one of claims 9 to 12 in which said predetermined data comprises generating a grid pattern indicating an array of desired locations in which a chip device may be selected for marking.

14. A method according to claim 13 in which said grid pattern covers a plurality of desired locations covering the predetermined field of view of the optical inspection device.

15. A method according to claim 13 or claim 14 in which the grid size is selectable to vary the tolerance of desired locations for chip devices to be marked.

16. A method according to any one of the preceding claims 9 to 15 in which the selection of chip devices for marking is effected simultaneously for each location within the said predetermined field of view.

17. Marking apparatus constructed and arranged substantially as herein described with reference to or as shown in Figures 2 to 6.

18. A method for marking semiconductor chip devices as herein described with reference to or as shown in Figures 2 to 6.

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