

ARITHMETIC ENGINE**ABSTRACT OF THE DISCLOSURE**

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An arithmetic engine (11) includes a first dual multiplier accumulator (MAC 12) for receiving input data and for producing first dual MAC output (21) data. A second dual MAC (13) is coupled in parallel to the first dual MAC (12). The second dual
10 MAC (13) receives input data and produces second dual MAC output (19) data. Adder array (14) is coupled to both the first dual MAC (12) and to the second dual MAC (13). The adder array (14) receives the input data, the first dual MAC output data, and the second dual MAC output data and produces arithmetic engine
15 output data. Each dual MAC (12, 13) comprises a multiplier cross point switch (42), multiplier registers (46), a register selector (50), and parallel multipliers (52, 54). Each adder array (14) comprises a cross point switch (84), adder registers (86), a register selector (88), adder (92), and condition code
20 determiner (94).

FIG. 1 accompanies this abstract.