

The invention relates to an arrangement for compressing data words with the help of a scaling-factor calculating circuit.

When remotely transmitting data or when storing, the problem of accommodating a plurality of data channels within a predetermined frame often occurs. If, thereby, the frame is smaller than the extent of the data words of the data channels, then the problem can only be overcome by compressing the data words.

The generation of a compressed code, which only contains the most significant bits in combination with a scaling factor indicating the magnitude of the data word which is to be encoded, is described in EP-A-0 133 697. A shift register, whose clock pulses are periodically suppressed in dependence on the scaling factor, is used for this purpose.

The object of the invention is to develop an arrangement for compressing data words with the help of a scaling factor which makes it possible to have a very rapid data processing with very little expenditure on circuitry - in particular, with a low requirement for storage space.

This object is achieved in an arrangement in accordance with the first part of claim 1 by the features specified in the characterising part.

Due to the splitting-up of the data words of the uncompressed data, the parts of the address words, which are required for the association of the uncompressed data with the aid of a code table, can also be split-up. Thereby, the invention is based on the realisation that a limited address range is sufficient for parts of the data words of the uncompressed data so that the uncompressed data words can also be shortened and address words can be formed therefrom. The dimensioning thereby, is chosen such that the word lengths of the address words are only shortened by the word lengths of the parts of data words which correspond to the uncompressed data. An overlapping range, which ensures the provision of the items of information required for a correct association of the data words for the compressed data, is obtained in this manner. With respect to a matrix which contains a complete code table for the assignment of the compressed data words to the uncompressed data words, the invention enables the storage zone to be reduced by the compression factor. This means, in particular with extensive code tables, that there are considerable advantages as regards the circuit aspects relating to the implementation of the stores as well as in respect of the reliability and the space requirements. The solution thereby makes possible a high data processing speed as is usual for a parallel processing of the data words i.e. a simultaneous transpositioning of all of the bits of a data word.

A preferred embodiment of the arrangement serves for the compression, for the purposes of data reduction, on the basis of NICAM coding such as for D2-MAC for example. With this method of transmission, it is desirable to transmit a plurality of stereo sound channels simultaneously. This is not possible in the linear mode of operation but rather, requires a switch-over into the compressed mode of operation. This differs from the linear mode of operation in that data words are transmitted with a word length of only 10 bits instead of a word length of 14 bits. The compression occurs by means of a scaling factor which does not however offer a linear dependence between the code words. Since the bit having the most significant value is reserved for the polarity for both data words i.e. those for the uncompressed and the compressed data, only the remaining 13 bits of the uncompressed data word, which have to be converted into the 9 bits of the compressed data word, are left over for carrying out the compression. With the uniform splitting-up of the data word for the compressed data, the opportunity is thus offered, in accordance with the teaching of the invention, of undertaking a division into three parts and thus of obtaining compressed data words each of 3 bits. The data word serving as an address word can then be reduced by the difference of the word length of the uncompressed data word i.e. 13 bits, and the word length of the remaining parts of the data words provided for the compressed data, i.e. 6 bits, so that there results a word length for each of the address words of 7 bits. In addition, there is the scaling factor which, for D2-MAC, amounts to 3 bits. In toto therefore, a word length of 7 address words and 3 scaling factors is needed. The reduction in storage space is thus almost the same as the compression factor.

Further developments of the method and of the circuit arrangement are apparent from the further claims, the description and the drawing which illustrates an embodiment of the subject matter of the invention.

In the drawing,

Fig. 1 shows an association table for illustrating the compression of 14 bit data words into 10 bit data words,

Fig. 2 a circuit arrangement for carrying out the compression and

Fig. 3 a code table.

The individual places of the data word provided for the uncompressed data as well as the places of the data word provided for the compressed data, which are associated with each other by means of the scaling factor, are laid out in Fig. 1. Since the

polarity is assigned to the bit having the most significant value and this remains unaltered for the uncompressed and the compressed data word, and thus is not subject to the data processing, this has not been shown in the illustration of the association of the two data words. As can be seen from the drawing, the places *b* have a variation range of 5 places within which they can be assigned to particular places of the uncompressed data word *X*.

A circuit arrangement for compressing data words with the help of a scaling factor is illustrated in Fig. 2. In detail, the circuit comprises an analogue/digital converter 1, a shift register 2 referenced FiFo, an serial/parallel converter 3 referenced S/P, a circuit for calculating a scaling factor 4 and three programmable read stores 5, 6 and 7. The places for the uncompressed data of the data words at the output of the serial/parallel converter 3 are referenced by an *X* and bear an index which indicates the significance of the place. The outputs of the circuit for calculating the scaling factor 4 are referenced *R* and likewise have indices for indicating the significance of the places. The same system is also encountered for the referencing of the address inputs *A* of the programmable read stores 5, 6 and 7 as well as for their data outputs *D*. The lines, on which the compressed data words appear, are referenced *b* whereby the indices likewise indicate the significance of the places.

Of the available address inputs *A0* - *A9* of the programmable read stores 5, 6 and 7, only the first seven places, namely *A0* - *A6*, are connected to the outputs of the second shift register 3. Thereby, the association is effected such that the outputs *X0* - *X6* of the second shift register 3 are connected to the address inputs *A0* - *A6* of the programmable read store 5, the outputs *X3* - *X9* are connected to the address inputs *A0* - *A6* of the programmable read store 6 and the outputs *X6* - *X12* are connected to the address inputs *A0* - *A6* of the programmable read store 7. There is thus a certain overlapping between the data words which are supplied to the address inputs *A0* - *A6* of the programmable read stores 5, 6 and 7. The remaining address inputs *A7* - *A9* of each of the programmable read stores 5, 6 and 7 are connected in parallel and are connected in common to the outputs *R0*, *R1*, *R2* of the circuit arrangement for calculating the scaling factor 4. The outputs *D0* - *D2* of the programmable read stores 5, 6 and 7 provide a nine place compressed data word whereby, the outputs *D0* - *D2* of the programmable read store 5 provide the places *b0* - *b2*, the outputs *D0* - *D2* of the programmable read store 6 provide the places *b3* - *b5* and the outputs *D0* to *D2* of the programmable read store 7 provide the places *b6* - *b8*.

In operation of the circuit arrangement, analogue signals, e.g. stereo sound signals, are converted into digital signals by the

analogue/digital converter 1, and in the case of D2-MAC, into signals having data words of 14 bit word length. Initially, 32 data words are expected in the shift register 2 and these are recalculated in the circuit for calculating the scaling factor.

On the basis of the scaling factor that has been determined, the places of the compressed data word are now associated with corresponding places of the uncompressed data word. It is thus decided for example, whether the place b_0 of the compressed data word is associated with the output X_0 , X_1 , X_2 , X_3 or X_4 . The same applies for the other places $b_1 - b_8$. Since there results a uniform displacement of all of the places, it is possible to equip the programmable read stores 5, 6 and 7 with similar store contents. Thereby, the content of the store corresponds to a code table such as exists in accordance with the D2-MAC specification between the so-called linear operating mode "linear code", and the compressed operating mode "companded code".

This relationship is illustrated in F3, wherein the quadratic field manifests the linear operating mode and the grey background section of the quadratic field manifests the compressed operating mode. The scaling factor for certain data words is indicated to the right of the code table. One can see that the scaling factor is constant in a middle region 8 of smaller dynamic range, is variable for different dynamic stages in the transition regions 9 and is again constant in the regions of highest dynamic range. Thus, the relationship between the compressed and uncompressed data words cannot be represented by linear displacement of the significance of the places in dependence on the dynamic range. Consequently, the table offers the most rapid means for establishing the association between the compressed and the uncompressed data words. A direct solution using a read store would require a storage space which amounts to $2^{16} \times 9$ bits = 589824 bits taking into account the uncompressed data words of 13 bits in addition to the scaling factor of 3 bits and the data words of the compressed data words of 9 bits. In contrast, the solution in accordance with the invention only requires a capacity of $2^{10} \times 3 \times 3$ bits = 9216 bits. This corresponds to a reduction of the otherwise needed storage capacity by the factor 64.



Claims

1. Arrangement for compressing data words with the help of a scaling-factor calculating circuit (4) and associated shift register means (2), characterised in that, the data bits ($X_0 \dots X_{12}$) of the uncompressed data words are applied to address inputs ($A_0 \dots A_6$) of permanent stores (5, 6, 7) in which code tables for a respective data word part ($b_0, b_1, b_2; b_3, b_4, b_5; b_6, b_7, b_8$) of the compressed data words are stored, wherein the control of a portion of the address inputs ($A_0 \dots A_6$) is effected by overlapping groups ($X_0 \dots X_6, X_3 \dots X_9, X_6 \dots X_{12}$) of uncompressed data bits and the control of a further portion of the address inputs (A_7, A_8, A_9) is effected by the bits (R_0, R_1, R_2) of a common scaling factor which is generated in the scaling-factor calculating circuit (4) and wherein the number of overlapping data bits corresponds to the difference between the length of the uncompressed and of the compressed data word.

2. Arrangement in accordance with Claim 1, characterised in that, the compression serves for data reduction on the basis of NICAM codings such as for D2-MAC for example, and that three permanent storage regions or special permanent stores (5, 6, 7) each having ten address inputs ($A_0 \dots A_9$) and three data outputs ($D_0 \dots D_2$) are provided, that the one portion of the address inputs for the uncompressed data bits comprises seven of these respective address inputs ($A_0 \dots A_6$) and the further portion for the bits of the scaling factor comprises the respective three remaining address inputs ($A_7 \dots A_9$).

3. Arrangement in accordance with Claim 2, characterised in that, the seven address inputs ($A_0 \dots A_6$) for the significant places $2^0 \dots 2^6$ of the first permanent storage region or permanent store (5) are controlled by bits of the significant places $2^0 \dots 2^6$ of the uncompressed data words, the same address inputs ($A_0 \dots A_6$) of the second permanent storage region or permanent store (6) are controlled by bits of the significant places $2^3 \dots 2^9$ of the uncompressed data words and the same address inputs ($A_0 \dots A_6$) of the third permanent storage region or permanent store (7) are controlled by bits of the significant places $2^6 \dots 2^{12}$ of the uncompressed data words.

4. Arrangement in accordance with one or more of the Claims 1 to 3, characterised in that, the most significant bit of the uncompressed data words represents, in particular, the polarity of the data words and remains unaltered during the compression.