according to some embodiments of the present disclosure, corresponding to the pixel detection device 100 in Fig. 1.

[0059] In step 210, a first detection signal is input to a pixel circuit by a system low voltage source in a first stage.

[0060] In some embodiments, please refer to Fig. 2, Fig. 6 and Fig. 7, compared with the pixel detection device in Fig. 1, the pixel detection device in Fig. 7 is a state diagram before a mass transfer technology stage. In short, the pixel detection device 100 in Figure 7 has not yet been installed the light-emitting element LED (i.e. a position P1). In the detection stage I2 before the mass transfer technology stage, the driving signal EM(n) and the detection control signal AT are at the low level VGL. The detection circuit 120 forms a first detection loop AT1 with the system low voltage source VSS and a signal line (e.g. the data line DL). In this stage, the first detection signal is input to the pixel circuit 110 through the system low voltage source VSS.

[0061] It should be noted that the mass transfer technology is that after a epitaxy process of the light-emitting element LED, a film transfer process of the light-emitting element LED must be carried out, to transfer millions of micron-scale light-emitting elements LEDs to each pixel (i.e., the pixel detection device 100) in a pixel array in the display panel. In some embodiments, the light emitting element LED includes a Micro light-emitting diode(μ-LED).

[0062] It is further illustrated that the embodiment in Fig. 2 is a timing diagram of detection signals before the mass transfer technology stage, after the mass transfer technology stage, and before the pixel detection device 100 in Fig. 1 leaves a factory.

WHAT IS CLAIMED IS:

1. A pixel detection device, comprising:

a data line;

a pixel circuit, coupled to a system high voltage source, a system low voltage source and a first reference voltage source; and

a detection circuit, coupled to the data line and the pixel circuit, and configured to receive a driving signal and a detection control signal, wherein the detection circuit forms a first detection loop with the system low voltage source and the data line, so as to detect whether the pixel circuit is abnormal according to the driving signal and the detection control signal in a first stage, wherein the detection circuit forms a second detection loop with the first reference voltage source, the system low voltage source, the pixel circuit, and the data line, so as to detect whether the pixel circuit is abnormal according to the driving signal and the detection control signal in a second stage.

2. The pixel detection device of claim 1, wherein the pixel circuit comprises:

a first node;

a second node;

a third node;

a fourth node; and

a light emitting element, configured to emit light according to a driving current of the pixel circuit, wherein the light emitting element comprises:

a first terminal, coupled to the system high voltage source; and

a second terminal, coupled to the first node.

3. The pixel detection device of claim 2, wherein the detection circuit forms a third detection loop with the system high voltage source, the light emitting element and the data line, so as to detect whether the light emitting element is abnormal according to the driving signal and the detection control signal in a third stage.

4. The pixel detection device of claim 2, wherein the pixel circuit further comprises:

a driving transistor, comprising:

a first terminal, coupled to the first node;

a second terminal, coupled to the second node; and

a control terminal, coupled to the third node, and configured to drive the light emitting element according to a voltage level of the third node, wherein the first node, the second node and the third node are not a same point;

a first transistor, comprising:

a first terminal, coupled to the first reference voltage source, and configured to receive a first reference voltage of the first reference voltage source;

a second terminal, coupled to the first node; and

a control terminal, configured to receive a control signal, wherein the first transistor is conducted in response to the control signal; and

a second transistor, comprising:

a first terminal, coupled to the driving transistor;

a second terminal, coupled to the system low voltage source; and

a control terminal, configured to receive the driving signal, wherein the second transistor is conducted in response to the driving signal.

5. The pixel detection device of claim 4, wherein the pixel circuit further comprises:

a reset circuit, coupled to the third node, the fourth node and a second reference voltage source, and configured to reset the third node to a second reference voltage of the second reference voltage source, so as to reset the first node and the second node through the driving transistor, wherein the reset circuit comprises:

a third transistor, comprising:

a first terminal, coupled to the third node;

a second terminal, coupled to the second reference voltage source; and

a control terminal, configured to receive a reset signal, wherein the third transistor is configured to reset the third node in response to the reset signal; and

a fourth transistor, comprising:

a first terminal, coupled to the fourth node;

a second terminal, coupled to the second reference voltage source; and

a control terminal, configured to receive the reset signal, wherein the fourth transistor is conducted in response to the reset signal.

6. The pixel detection device of claim 5, wherein the pixel circuit further comprises:

a compensation circuit, coupled to the second node, the third node, the fourth node and the reset circuit, and configured to compensate the third node to the first reference voltage of the first reference voltage source, wherein the compensation circuit comprises:

a fifth transistor, comprising:

a first terminal, coupled to the second node;

a second terminal, coupled to the third node; and

a control terminal, configured to receive a compensation signal, wherein the fifth transistor is conducted in response to the compensation signal; and

a sixth transistor, comprising:

a first terminal, coupled to the fourth node;

a second terminal, coupled to the second reference voltage source; and

a control terminal, configured to receive the compensation signal, wherein the sixth transistor is conducted in response to the compensation signal.

7. The pixel detection device of claim 6, wherein the pixel circuit further comprises:

a writing circuit, coupled to the fourth node and the data line, and configured to receive a data voltage of the data line for writing into the third node and the fourth node, wherein the writing circuit comprises:

a seventh transistor, comprising:

a first terminal, coupled to the fourth node;

a second terminal, coupled to the data line; and

a control terminal, configured to receive a writing signal, wherein the seventh transistor is conducted in response to the writing signal.

8. The pixel detection device of claim 2, wherein the detection circuit comprises:

a fifth node;

a first detection transistor, comprising:

a first terminal, coupled to the fifth node;

a second terminal, coupled to the first node of the pixel circuit; and

a control terminal, configured to receive the driving signal, wherein the first detection transistor is conducted in response to the driving signal; and

a second detection transistor, comprising:

a first terminal, coupled to the data line;

a second terminal, coupled to the first terminal of the first detection transistor; and

a control terminal, configured to receive the detection control signal, wherein the second detection transistor is conducted in response to the detection control signal.

9. A pixel detection device, comprising:

a signal line;

a pixel circuit, coupled to a system high voltage source, a system low voltage source and a first reference voltage source; and

a detection circuit, coupled to the signal line, the pixel circuit and the first reference voltage source, and configured to receive a first driving signal and a detection control signal, wherein the detection circuit forms a first detection loop with the first reference voltage source, the pixel circuit and the signal line, so as to detect whether the pixel circuit is abnormal according to the first driving signal and the detection control signal in a first stage, wherein the detection circuit forms a second detection loop with the system low voltage source, the pixel circuit and the signal line, so as to detect whether the pixel circuit is abnormal according to the first driving signal and the detection control signal in a second stage.

10. The pixel detection device of claim 9, wherein the pixel circuit comprises:

a first node;

a second node;

a third node;

a fourth node; and

a light emitting element, configured to emit light according to a driving current of the pixel circuit, wherein the light emitting element comprises:

a first terminal, coupled to the system high voltage source; and

a second terminal, coupled to the first node.

11. The pixel detection device of claim 10, wherein the detection circuit forms a third detection loop with the system high voltage source, the light emitting element and the signal line, so as to detect whether the light emitting

element is abnormal according to the first driving signal and the detection control signal in a third stage.

12. The pixel detection device of claim 9, wherein the signal line is configured to receive a first detection signal of the first detection loop, so as to detect whether the pixel circuit is abnormal according to the first driving signal and the detection control signal in the first stage, and is configured to receive a second detection signal of the second detection loop, so as to detect whether the pixel circuit is abnormal according to the first driving signal and the detection control signal.

13. The pixel detection device of claim 10, wherein the pixel circuit further comprises:

a driving transistor, comprising:

a first terminal, coupled the first node;

a second terminal, coupled to the second node; and

a control terminal, coupled to the third node, and configured to drive the light emitting element according to a voltage level of the third node, wherein the first node, the second node and the third node are not a same point;

a first transistor, comprising:

a first terminal, coupled to the first reference voltage source, and configured to receive a first reference voltage of the first reference voltage source;

a second terminal, coupled to the first node; and

a control terminal, configured to receive a control signal, wherein the first transistor is conducted in response to the control signal; and

a second transistor, comprising:

a first terminal, coupled to the driving transistor;

a second terminal, coupled to the system low voltage source; and

a control terminal, configured to receive a second driving signal, wherein the second transistor is conducted in response to the second driving signal.

14. The pixel detection device of claim 13, wherein the pixel circuit further comprises:

a reset circuit, coupled to the third node and a second reference voltage source, and configured to reset the third node to a second reference voltage of the second reference voltage source, so as to reset the first node and the second node through the driving transistor, wherein the reset circuit comprises:

a third transistor, comprising:

a first terminal, coupled to the third node;

a second terminal, coupled to the second reference voltage source; and

a control terminal, configured to receive a reset signal, wherein the third transistor is configured to reset the third node in response to the reset signal; and

a fourth transistor, comprising:

a first terminal, coupled to the fourth node;

a second terminal, coupled to the second reference voltage source; and

a control terminal, configured to receive the reset signal, wherein the fourth transistor is conducted in response to the reset signal.

15. The pixel detection device of claim 14, wherein the pixel circuit further comprises:

a compensation circuit, coupled to the second node, the third node and the reset circuit, and configured to a receive a compensation signal, so as to compensate the third node according to the compensation signal, wherein the compensation circuit comprises:

a fifth transistor, comprising:

a first terminal, coupled to the second node;

a second terminal, coupled to the third node; and

a control terminal, configured to receive the compensation signal, wherein the fifth transistor is conducted in response to the compensation signal; and

a sixth transistor, comprising:

a first terminal, coupled to the fourth node;

a second terminal, coupled to the second reference voltage source; and

a control terminal, configured to receive the compensation signal, wherein the sixth transistor is conducted in response to the compensation signal.

16. The pixel detection device of claim 15, wherein the pixel circuit further comprises:

a writing circuit, coupled to the fourth node and a data line, and configured to receive a data voltage of the data line for writing into the third node and the fourth node, wherein the writing circuit comprises:

a seventh transistor, comprising:

a first terminal, coupled to the fourth node;

a second terminal, coupled to the data line; and

a control terminal, configured to receive a writing signal, wherein the seventh transistor is conducted in response to the writing signal.

17. The pixel detection device of claim 16, wherein the signal line is different from the data line.

18. The pixel detection device of claim 10, wherein the detection circuit comprises:

a first detection transistor, comprising:

a first terminal, coupled to the signal line;

a second terminal, coupled to the second node; and

a control terminal, configured to receive the first driving signal, wherein the first detection transistor is conducted in response to the first driving signal; and

a second detection transistor, comprising:

a first terminal, coupled to the first reference voltage source;

a second terminal, coupled to the first node; and

a control terminal, configured to receive the detection control signal, wherein the second detection transistor is conducted in response to the detection control signal.

19. A pixel detection method, adapted to a pixel detection device, wherein the pixel detection device comprises a signal line, a pixel circuit and a detection circuit, wherein the pixel circuit is coupled to a system high voltage source, a system low voltage source and a first reference voltage source, wherein the detection circuit is coupled to the signal line and the pixel circuit, wherein the pixel detection method comprises:

inputting a first detection signal to the pixel circuit by the system low voltage source in a first stage;

receiving the first detection signal by the detection circuit and the signal line in the first stage, so as to determine whether the pixel circuit is abnormal according to the first detection signal;

inputting a second detection signal to the pixel circuit by the first reference voltage source in a second stage; and

receiving the second detection signal by the detection circuit and the signal line in the second stage, so as to determine whether the pixel circuit is abnormal according to the second detection signal.

20. The pixel detection method of claim 19, wherein the pixel circuit comprises a light emitting element, the light emitting element is coupled between the system high voltage source and the system low voltage source, wherein the pixel detection method further comprises:

inputting a third detection signal to the light emitting element of the pixel circuit by the system high voltage source in a third stage; and

receiving the third detection signal by the detection circuit and the signal line in the third stage, so as to determine whether the light emitting element is abnormal according to the third detection signal.