EPITAXIAL DEPOSITION METHOD AND EPITAXIAL WAFER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to Chinese Patent Application No. 202411447580.9, filed in China on October 16, 2024, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] Embodiments of the present application relate to the field of semiconductor manufacturing technology, and more particularly, to an epitaxial deposition method and epitaxial wafer.

BACKGROUND

[0003] Epitaxial deposition technology is a technique that enables to deposit an epitaxial layer on a polished wafer. The deposited epitaxial layer has a different conductivity, resistivity, and structural characteristics than the polished wafer, which can fulfill the production requirements of a variety of different semiconductor devices and greatly improve both the flexibility and performance of semiconductor device design.

[0004] With the rapid development of semiconductor technology, the requirements for the quality of epitaxial wafers are becoming increasingly stringent, especially the requirements for the minority carrier lifetime (MCLT) level of epitaxial wafers. It is known that the MCLT level of the epitaxial wafer is closely related to the content of bulk metal impurities. If the content of metal impurities in the reactor chamber is too high during the epitaxial deposition process, the resulting epitaxial wafer may contain excessive metal impurities, which in turn affects the MCLT level of the epitaxial wafer.

SUMMARY

[0005] In view of the above, embodiments of the present application aim to provide an epitaxial deposition method and an epitaxial wafer, which can obtain an epitaxial wafer with an MCLT greater than or equal to 2200μs.

[0006] The technical solution of embodiments of the present application is implemented as follows:

[0007] In a first aspect, an embodiment of the present application provides an epitaxial deposition method, wherein the epitaxial deposition method comprises:

[0008] performing a minority carrier lifetime test on a first epitaxial wafer to obtain minority carrier lifetime of the first epitaxial wafer;

[0009] determining a first gas flow rate of slit carrier gas introduced into a reactor chamber in a case that the minority carrier lifetime of the first epitaxial wafer is less than a predetermined first threshold;

[0010] manufacturing a second epitaxial wafer based on the slit carrier gas with the first gas flow rate; wherein minority carrier lifetime of the second epitaxial wafer is greater than or equal to 2200μs.

[0011] In some examples, the first gas flow rate of the slit carrier gas is 20slm to 35slm.

[0012] In some examples, the epitaxial deposition method further comprises:

[0013] obtaining a first characteristic value characterizing resistivity uniformity of an epitaxial layer of the second epitaxial wafer based on resistivities at different locations on the epitaxial layer of the second epitaxial wafer;

[0014] in a case that the first characteristic value is greater than a predetermined second threshold, adjusting a first power ratio and a second power ratio during an epitaxial deposition process according to a resistivity at a center location and a resistivity at an edge location on the epitaxial layer of the second epitaxial wafer; wherein, the first power ratio is a ratio of a power of a heating component at a center location above the reactor chamber to a sum of powers of heating components at locations above the reactor chamber other than the center location above the reactor chamber; the second power ratio is a ratio of a power of a heating component at a center

location below the reactor chamber to a sum of powers of heating components at locations below the reactor chamber other than the center location below the reactor chamber;

[0015] acquiring an epitaxial wafer obtained through remanufacturing according to the adjusted first power ratio and the adjusted second power ratio.

[0016] In some examples, an adjustment range of the first power ratio is 66% to 82%, and an adjustment range of the second power ratio is 16% to 20%.

[0017] In some examples, in a case that the first power ratio and the second power ratio increase or decrease, and the first power ratio is adjusted by a first adjustment magnitude and the second power ratio is adjusted by a second adjustment magnitude, a ratio of the first adjustment magnitude to the second adjustment magnitude is in a range of 3:1 to 5:1.

[0018] In some examples, the in a case that the first characteristic value is greater than a predetermined second threshold, adjusting a first power ratio and a second power ratio during an epitaxial deposition process according to a resistivity at a center location and a resistivity at an edge location on the epitaxial layer of the second epitaxial wafer comprises:

[0019] in a case that the first characteristic value is greater than the second threshold,

[0020] increasing the first power ratio and the second power ratio in a case that the resistivity at the center location is greater than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer; or

[0021] decreasing the first power ratio and the second power ratio in a case that the resistivity at the center location is less than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer.

[0022] In some examples, the epitaxial deposition method further comprises:

[0023] after acquiring the epitaxial wafer obtained through remanufacturing, determining a second gas flow rate of the slit carrier gas introduced into the reactor chamber in a case that the first characteristic value of the epitaxial layer of the epitaxial

wafer obtained through remanufacturing is greater than the second threshold; wherein the second gas flow rate is less than the first gas flow rate, and the second gas flow rate is 20slm to 35slm;

[0024] acquiring an epitaxial wafer obtained through additional remanufacturing based on the slit carrier gas with the second gas flow rate; wherein, the first characteristic value of the epitaxial wafer obtained through additional remanufacturing is less than the second threshold.

[0025] In some examples, the epitaxial deposition method further comprises:

[0026] detecting a thickness of an epitaxial layer of the second epitaxial wafer to obtain a second characteristic value characterizing thickness uniformity of the epitaxial layer of the second epitaxial wafer;

[0027] adjusting a gas flow ratio during an epitaxial deposition process in a case that the second characteristic value is greater than a predetermined third threshold; wherein, the gas flow ratio is a ratio of a gas flow rate of a reaction gas at the center location of the reactor chamber to a gas flow rate at a first gas inlet in the reactor chamber.

[0028] In some examples, the adjusting a gas flow ratio during an epitaxial deposition process in a case that the second characteristic value is greater than a predetermined third threshold comprises:

[0029] increasing the gas flow ratio in a case that a thickness at the center location is less than a thickness at the edge location of the epitaxial layer; or

[0030] decreasing the gas flow ratio in a case that the thickness at the center location is greater than the thickness at the edge location of the epitaxial layer.

[0031] In a second aspect, an embodiment of the present application provides an epitaxial wafer, wherein the epitaxial wafer is manufactured by the epitaxial deposition method according to the first aspect, and minority carrier lifetime of the epitaxial wafer is greater than or equal to 2200μs.

[0032] In some examples, a first characteristic value of the epitaxial wafer is less than or equal to 2.7%, and a second characteristic value is less than or equal to 0.65%,

wherein the first characteristic value is used to characterize resistivity uniformity of an epitaxial layer of the epitaxial wafer, and the second characteristic value is used to characterize thickness uniformity of the epitaxial layer of the epitaxial wafer.

[0033] Embodiments of the present application provide an epitaxial deposition method and an epitaxial wafer. In the present application, the gas flow rate of the slit carrier gas is adjusted through the MCLT of the first epitaxial wafer, so that the slit carrier gas with the first gas flow rate is introduced into the reactor chamber, thereby reducing the metal impurity content in the epitaxial layer of the second epitaxial wafer and ultimately improving the MCLT of the second epitaxial wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] FIG. 1 shows a schematic diagram of a reactor chamber used in an epitaxial deposition process provided in an embodiment of this disclosure;

[0035] FIG. 2 shows a schematic flowchart of an epitaxial deposition method provided in an embodiment of this disclosure;

[0036] FIG. 3 shows MCLT corresponding to different first gas flow rates of the slit carrier gas in a case that the slit carrier gas is hydrogen provided in an embodiment of this disclosure;

[0037] FIG. 4 shows first characteristic values corresponding to different first gas flow rates of the slit carrier gas provided in an embodiment of this disclosure;

[0038] FIG. 5 shows a schematic diagram of a method for calculating a first characteristic value provided in an embodiment of this disclosure;

[0039] FIG. 6 shows a schematic diagram of a method for calculating a first characteristic value provided in another embodiment of this disclosure;

[0040] FIG. 7 shows a schematic diagram of a method for calculating a second characteristic value provided in an embodiment of this disclosure;

[0041] FIG. 8 shows a flowchart of an epitaxial deposition method provided in another embodiment of this disclosure.

DETAILED DESCRIPTION

[0042] The technical solutions in this disclosure will now be clearly and completely described with reference to the accompanying drawings.

[0043] It should be noted that, for clarity, not all features of a particular embodiment are described or shown in the specification and drawings. Furthermore, to avoid unnecessary details obscuring the technical solutions of interest in this disclosure, only the apparatus structures and method steps closely related to the technical solutions of this disclosure are described and shown in the specification and drawings, while other details that are not closely related to the technical content of this disclosure and are known to those skilled in the art are omitted.

[0044] Furthermore, the epitaxial deposition process mentioned in this disclosure may include a loading stage, a heating stage, a baking stage, a vapor deposition stage of polishing wafers, and an unloading stage of epitaxial wafers.

[0045] As mentioned earlier, excessive metal impurities in the reactor chamber may lead to excessively high metal content in the manufactured epitaxial wafers, which in turn affects the MCLT level of the epitaxial wafers. In related technologies, before epitaxial deposition begins, it is necessary to first confirm the content of metal impurities in the reactor chamber. If the content of metal impurities does not meet the requirements, the interior of the reactor chamber needs to be cleaned or even replaced with another reactor chamber. This often results in the need to replace the reactor chamber multiple times, making the entire process operation cycle long.

[0046] As shown in FIG. 1, the reactor chamber 10 used in the epitaxial deposition process typically includes two gas inlets, namely, a first gas inlet 101 and a second gas inlet 102. In FIG. 1, the direction of the first gas inlet 101 is shown as being orthogonal to the direction of the second gas inlet 102. The first gas inlet 101, also commonly referred to as the main gas inlet, is used to supply gas to the main area of the reactor chamber 10, that is, to supply gas mainly to the area above the polished wafer W placed on the base 103. The gas includes hydrogen (i.e., the so-called main hydrogen (Main H2)), reaction gas, and dopant gas, etc. The second gas inlet 102, also commonly

referred to as the auxiliary gas inlet, mainly supplies gas to the area of the reactor chamber 10 located below the base 103. This gas includes hydrogen (i.e., the so-called slit hydrogen (Slit H2)). The gas flow rate of the first gas inlet 101 and the second gas inlet 102 may be controlled, for example, by a valve. It should be noted that, in this disclosure, the introduction of main hydrogen and slit hydrogen into the reactor chamber 10 may continue throughout the entire epitaxial deposition process.

[0047] In some examples, the slit hydrogen may be used as a purge gas, as well as a carrier gas.

[0048] The inventors discover that separately increasing the gas flow rate of the slit hydrogen can clean the reactor chamber, thereby improving the MCLT level of the epitaxial wafer. This is mainly because the slit hydrogen can purge the area below the base 103, thereby inhibiting the diffusion of metal impurities from the area below the base 103 to the area above the base 103, which in turn affects the metal impurity content in the epitaxial wafer.

[0049] Based on this, referring to FIG. 2, an embodiment of this disclosure provides an epitaxial deposition method, which specifically includes following steps:

[0050] S201, performing a minority carrier lifetime test on a first epitaxial wafer to obtain minority carrier lifetime of the first epitaxial wafer;

[0051] S202, determining a first gas flow rate of slit carrier gas introduced into a reactor chamber in a case that the minority carrier lifetime of the first epitaxial wafer is less than a predetermined first threshold;

[0052] S203, manufacturing a second epitaxial wafer based on the slit carrier gas with the first gas flow rate; where minority carrier lifetime of the second epitaxial wafer is greater than or equal to 2200μs.

[0053] First, in step S201, the first epitaxial wafer is subjected to MCLT test to obtain the MCLT of the first epitaxial wafer. Understandably, the MCLT of the first epitaxial wafer may characterize the current content of metal impurities in the reactor chamber.

[0054] In some examples, the MCLT of the first epitaxial wafer may be obtained by the Conductivity Decay Method (CDM), which involves injecting non-equilibrium carriers into the epitaxial layer of the first epitaxial wafer and then measuring the decay of the conductivity of the epitaxial layer of the first epitaxial wafer over time, thereby determining the MCLT of the first epitaxial wafer. Of course, other methods may also be used to obtain the MCLT of the first epitaxial wafer in this disclosure, such as the surface photovoltage method (SPV), which uses light to irradiate the surface of the epitaxial layer of the first epitaxial wafer to generate a photovoltage signal, and then obtains the corresponding MCLT by measuring the decay time of the photovoltage signal.

[0055] In step S202, in a case that the first threshold is predetermined to refer to the critical value of the minority carrier lifetime of the epitaxial wafer, it is determined according to the requirements of the semiconductor device using the epitaxial wafer.

[0056] In some examples, the slit carrier gas may be hydrogen or other gases that may serve a purging function.

[0057] Understandably, in a case that the MCLT of the first epitaxial wafer is less than the first threshold, in order to ensure that the MCLT level of the second epitaxial wafer meets the requirements, the gas flow rate of the slit carrier gas is adjusted so that the slit carrier gas with the first gas flow rate is introduced into the reactor chamber 10, thereby suppressing the diffusion of metal impurities from the area below the base 103 to the area above the base 103, thereby reducing the metal impurity content in the epitaxial layer of the second epitaxial wafer, and improving the MCLT of the second epitaxial wafer.

[0058] For the technical solution shown in FIG. 1, in some possible implementations, the first gas flow rate of the slit carrier gas is 20slm to 35slm.

[0059] In this disclosure, the first gas flow rate of the slit carrier gas is predetermined to 20slm to 35slm, because this can further purge metal impurities in the area below the base 103 from the reactor chamber 10, and prevent metal impurities in the area below the base 103 from diffusing to the area above the base 103. On the one

hand, if the first gas flow rate of the slit carrier gas is too small, it may not be able to completely purge the metal impurities in the area below the base 103 out of the reactor chamber 10. On the other hand, if the first gas flow rate of the slit carrier gas is too large, it may cause the edge flatness of the second epitaxial wafer to deteriorate. This is mainly because the increase in the first gas flow rate of the slit carrier gas may change the gas flow pattern inside the reactor chamber 10, which in turn leads to uneven distribution of the reaction gas on the surface of the polished wafer W, affecting the deposition rate at the edge location of the second epitaxial wafer and thus affecting the edge flatness. Furthermore, the increase in the first gas flow rate of the slit carrier gas may change the heat transfer efficiency inside the reactor chamber 10, resulting in uneven temperature distribution, which in turn leads to inconsistent deposition rates at the center location and edge location of the epitaxial layer, thus affecting the edge flatness.

[0060] Referring to FIG. 3, it shows the MCLT of the second epitaxial wafer in a case that the slit carrier gas is hydrogen and the corresponding first gas flow rates are 5slm, 10slm, 20slm, 30slm and 40slm. As shown in FIG. 3, in a case that the slit carrier gas is hydrogen and the corresponding first gas flow rates are 5slm and 10slm respectively, the MCLT of the second epitaxial wafer is approximately 1800μs and 2100μs, respectively. In a case that the slit carrier gas is hydrogen and the corresponding first gas flow rate is 20slm to 35slm, the MCLT of the second epitaxial wafer is greater than 2200μs. In a case that the slit carrier gas is hydrogen and the corresponding first gas flow rate is 40slm, although the MCLT of the second epitaxial wafer is greater than 2200μs, the edge flatness of the second epitaxial wafer may deteriorate in a case that the first gas flow rate of the slit carrier gas is large during the actual implementation.

[0061] In this disclosure, although the MCLT level of the second epitaxial wafer is improved by introducing the slit carrier gas with the first gas flow rate into the reactor chamber 10, the increase in the gas flow rate of the slit carrier gas may have a negative impact on the resistivity distribution and thickness distribution at different locations on the epitaxial layer of the second epitaxial wafer. Therefore, in this disclosure, after the

MCLT level of the second epitaxial wafer meets the requirements, it is still necessary to detect the resistivity distribution and thickness distribution at different locations on the epitaxial layer. Therefore, for the technical solution shown in FIG. 1, in some possible implementations, the epitaxial deposition method further includes:

[0062] obtaining a first characteristic value characterizing resistivity uniformity of an epitaxial layer of the second epitaxial wafer based on resistivities at different locations on the epitaxial layer of the second epitaxial wafer;

[0063] in a case that the first characteristic value is greater than a predetermined second threshold, adjusting a first power ratio and a second power ratio during an epitaxial deposition process according to a resistivity at a center location and a resistivity at an edge location on the epitaxial layer of the second epitaxial wafer; where, the first power ratio is a ratio of a power of a heating component at a center location above the reactor chamber to the sum of powers of heating components at locations above the reactor chamber other than the center location above the reactor chamber; the second power ratio is a ratio of a power of a heating component at a center location below the reactor chamber to the sum of powers of heating components at locations above the reactor chamber other than the center location below the reactor chamber;

[0064] acquiring an epitaxial wafer obtained through according to the adjusted first power ratio and second power ratio.

[0065] It should be noted that the second threshold refers to the upper limit of the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer. In a case that the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer exceeds the second threshold, it indicates that the resistivity distribution of the epitaxial layer is not uniform. Specifically, the second threshold may be determined based on the actual situation.

[0066] The inventors also discover that, as shown in FIG. 4, in a case that the first gas flow rate of the slit carrier gas is increased, the resistivity uniformity of the epitaxial layer deteriorates, especially the resistivity at the edge location of the epitaxial

layer is significantly lower than that at the center location. This is mainly because introducing the slit carrier gas into the reactor chamber 10 with the first gas flow rate promotes the diffusion of the dopant gas to the edge location of the epitaxial layer. Therefore, after the second epitaxial wafer is manufactured based on the first gas flow rate of the slit carrier gas and the MCLT of the second epitaxial wafer is greater than the second threshold, it is still necessary to detect the resistivity uniformity of the epitaxial layer. It should be noted that the resistivity uniformity of the epitaxial layer in this disclosure refers to the fact that the resistivities at different locations on the epitaxial layer are not significantly different, that is, the difference in resistivities between different locations is within a predetermined range.

[0067] It should be noted that the resistivity uniformity of the epitaxial layer in this disclosure may be obtained by the following method, for example, as shown in FIG. 5, by selecting nine measurement points on the epitaxial layer, one of which is located at the center location of the epitaxial layer, four of which are located at half the radius of the epitaxial layer, and the remaining four of which are located at the edge locations. It should be noted that, in this disclosure, the edge location on the epitaxial layer refers to the location close to the center location along the radial direction of the epitaxial layer and 5mm, 6mm, or 10mm away from the outermost edge of the epitaxial layer. In the specific implementation process, after obtaining the resistivities of the above nine measurement points, the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer may be obtained based on the ratio of the difference between the maximum and minimum resistivity values measured and the sum of the maximum and minimum resistivity values measured. Specifically, the first characteristic value is calculated according to the following formula:

$$a = \frac{R_{max} - R_{min}}{R_{max} + R_{min}} \times 100\%$$

[0068] Where a represents the first characteristic value; R_{max} represents the maximum resistivity value; and R_{min} represents the minimum resistivity value.

[0069] Of course, in the specific implementation process, as shown in FIG. 6, five measurement points may be selected on the epitaxial layer. One of these five measurement points is located at the center location of the epitaxial layer, and the other four measurement points are located at the edge locations of the epitaxial layer. Then, based on the ratio of the difference between the maximum and minimum resistivity values measured and the sum of the maximum and minimum resistivity values measured, the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer can be obtained.

[0070] In the specific implementation process, after obtaining the first characteristic value, in a case that the first characteristic value is greater than a predetermined second threshold, it indicates that the resistivities at different locations on the epitaxial layer of the second epitaxial wafer are not uniform. Therefore, it is necessary to adjust a first power ratio and a second power ratio during an epitaxial deposition process. It should be noted that the first power ratio is a ratio of a power of a heating component at a center location above the reactor chamber to the sum of powers of heating components at different locations above the reactor chamber; the second power ratio is a ratio of a power of a heating component at a center location below the reactor chamber to the sum of powers of heating components at different locations below the reactor chamber. For example, the first power ratio of 72% means that a ratio of a power of a heating component at a center location above the reactor chamber to the sum of powers of heating components at different locations above the reactor chamber is 72%. The first power ratio of 17.5% means that a ratio of a power of a heating component at a center location below the reactor chamber to the sum of powers of heating components at different locations below the reactor chamber is 17.5%.

[0071] Understandably, during the epitaxial deposition process, multiple heating components are arranged above and below the reactor chamber to provide a high-temperature environment for the epitaxial deposition process. Therefore, in this disclosure, in a case that the resistivities at different locations on the epitaxial layer of

the second epitaxial wafer are not uniform, the resistivity of the epitaxial layer is adjusted by adjusting the powers of the heating components located above and below the reactor chamber.

[0072] In some examples of the above implementation methods, an adjustment range of the first power ratio is 66% to 82%, and an adjustment range of the second power ratio is 16% to 20%.

[0073] By controlling the adjustment range of the first power ratio and the second power ratio, the diffusion of dopants during the epitaxial deposition process can be controlled, which helps to achieve a more uniform doping distribution and improve the resistivity uniformity.

[0074] Optionally, in a case that the first power ratio and the second power ratio increase or decrease synchronously, and the first power ratio is adjusted by a first adjustment magnitude and the second power ratio is adjusted by a second adjustment magnitude, a ratio of the first adjustment magnitude to the second adjustment magnitude is in a range of 3:1 to 5:1.

[0075] Specifically, in a case that the resistivities are uneven at different locations on the epitaxial layer of the second epitaxial wafer, the first power ratio is 74% and the second power ratio is 18%. In a case that the first power ratio and the second power ratio are increased synchronously according to the actual situation, and the ratio of the first adjustment magnitude of the first power ratio to the second adjustment magnitude of the second power ratio is 4:1, the adjusted first power ratio is 76% and the adjusted second power ratio is 18.5%. In this disclosure, the first power ratio and the second power ratio are increased or decreased synchronously, which can avoid excessive temperature difference between the upper and lower parts of the reactor chamber during the adjustment process, so as to prevent defects such as slip and dislocation in the epitaxial layer.

[0076] Optionally, the in a case that the first characteristic value is greater than a predetermined second threshold, adjusting a first power ratio and a second power ratio during an epitaxial deposition process according to a resistivity at a center location and

a resistivity at an edge location on the epitaxial layer of the second epitaxial wafer includes:

[0077] in a case that the first characteristic value is greater than the second threshold,

[0078] increasing the first power ratio and the second power ratio in a case that the resistivity at the center location is greater than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer; or

[0079] decreasing the first power ratio and the second power ratio in a case that the resistivity at the center location is less than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer.

[0080] Understandably, in a case that the resistivity at the center location is greater than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer, it indicates that the doping concentration of the dopant at the center location of the epitaxial layer is lower than that at the edge location. Therefore, in the specific implementation process, increasing the first power ratio and the second power ratio can improve the temperature distribution at the center location of the epitaxial layer, thereby increasing the deposition rate at the center location and increasing the doping concentration of the dopant. Conversely, in a case that the resistivity at the center location is less than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer, it indicates that the doping concentration of the dopant at the center location of the epitaxial layer is greater than that at the edge location. Therefore, in the specific implementation process, the first power ratio and the second power ratio are decreased.

[0081] In some examples of the above-described implementation methods, the epitaxial deposition method further includes:

[0082] After acquiring the epitaxial wafer obtained through remanufacturing, determining a second gas flow rate of the slit carrier gas introduced into the reactor chamber in a case that the first characteristic value of the epitaxial layer of the epitaxial wafer obtained through remanufacturing is greater than the second threshold; where the

second gas flow rate is less than the first gas flow rate, and the second gas flow rate is 10slm to 35slm;

[0083] acquiring an epitaxial wafer obtained through additional remanufacturing based on the slit carrier gas with the second gas flow rate; where, the first characteristic value of the epitaxial wafer obtained through additional remanufacturing is less than the second threshold.

[0084] It should be noted that if the resistivities at different locations on the epitaxial layer of the epitaxial wafer obtained through remanufacturing are still uneven after adjusting the first power ratio and the second power ratio, it is necessary to reduce the gas flow rate of the slit carrier gas introduced into the reactor chamber 10, introduce the slit carrier gas into the reactor chamber at the second gas flow rate, and additionally remanufacture the second epitaxial wafer. Understandably, after the epitaxial wafer obtained through additional remanufacturing, it is still necessary to reconfirm the resistivity uniformity at different locations on the epitaxial layer of the epitaxial wafer obtained through additional remanufacturing in a case that the MCLT of the second epitaxial wafer is greater than or equal to 2000μs.

[0085] In some possible implementations, the epitaxial deposition method further includes:

[0086] detecting a thickness of an epitaxial layer of the second epitaxial wafer to obtain a second characteristic value characterizing thickness uniformity of the epitaxial layer of the second epitaxial wafer;

[0087] adjusting a gas flow ratio during an epitaxial deposition process in a case that the second characteristic value is greater than a predetermined third threshold; where, the gas flow ratio is a ratio of a gas flow rate of a reaction gas at the center location of the reactor chamber to a gas flow rate at a first gas inlet in the reactor chamber.

[0088] In some examples, the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer may be obtained by the following method. For example, as shown in FIG. 7, multiple measurement

points are selected on any diameter of the epitaxial layer. To ensure the accuracy of the measurement results, for example, 31 measurement points may be selected. Then, based on the ratio of the difference between the maximum and minimum thickness values measured and the sum of the maximum and minimum thickness values measured, the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer may be obtained. Specifically, the second characteristic value is calculated according to the following formula:

$$b = \frac{T_{max} - T_{min}}{T_{max} + T_{min}} \times 100\%$$

[0089] Where b represents the second characteristic value; T_{max} represents the maximum thickness value; and T_{min} represents the minimum thickness value.

[0090] Of course, in some examples, as shown in FIG. 5, nine measurement points may be selected on the epitaxial layer. One of these nine measurement points is located at the center location of the epitaxial layer, four measurement points are located at half the radius, and the remaining four measurement points are located at the edge locations. Then, based on the ratio of the difference between the maximum and minimum thickness values measured and the sum of the maximum and minimum thickness values measured, the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer may be obtained. Alternatively, as shown in FIG. 6, five measurement points are selected on the epitaxial layer. One of these five measurement points is located at the center location of the epitaxial layer, and the other four measurement points are located at the edge locations. Then, based on the ratio of the difference between the maximum and minimum thickness values measured and the sum of the maximum and minimum thickness values measured, the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer may be obtained.

[0091] It should be noted that the third threshold refers to the upper limit of the second characteristic value characterizing the thickness uniformity of the epitaxial layer

of the second epitaxial wafer. In a case that the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer is greater than the third threshold, it indicates that the thickness distribution of the second epitaxial wafer is not uniform or that the flatness does not meet the requirements. Therefore, it is necessary to adjust the thickness distribution of the epitaxial layer by adjusting the gas flow ratio during the epitaxial deposition process. Specifically, the third threshold may be determined based on the actual situation.

[0092] In this disclosure, the gas flow ratio refers to the ratio of the gas flow rate of the reaction gas at the center location of the epitaxial layer to the gas flow rate of the reaction gas entering the first gas inlet 101 of the reactor chamber. For example, a gas flow ratio of 45% means that the gas flow rate of the reaction gas at the center location of the epitaxial layer accounts for 45% of the gas flow rate entering the first gas inlet 101 of the reactor chamber, which means that 65% of the gas flow rate of the reaction gas diffuses to edge locations of the epitaxial layer.

[0093] Specifically, in some examples, the adjusting a gas flow ratio during an epitaxial deposition process in a case that the second characteristic value is greater than a predetermined third threshold includes:

[0094] increasing the gas flow ratio in a case that a thickness at the center location is less than a thickness at the edge location of the epitaxial layer; or

[0095] decreasing the gas flow ratio in a case that the thickness at the center location is greater than the thickness at the edge location of the epitaxial layer.

[0096] Understandably, in a case that the thickness at the center location of the epitaxial layer is less than that at the edge location, increasing the gas flow ratio can increase the gas flow rate of the reaction gas at the center location, thereby increasing the deposition rate of the epitaxial layer at the center location and making it closer to the deposition rate of the epitaxial layer at the edge location, thus reducing the difference in thickness distribution. Conversely, in a case that the thickness at the center location of the epitaxial layer is greater than that at the edge location, decreasing the gas flow ratio can decrease the deposition rate of the epitaxial layer at the center location

and reduce the difference in thickness distribution between the center location and the edge location of the epitaxial layer.

[0097] Referring to FIG. 8, which illustrates in detail the process flow steps of an epitaxial deposition method provided in this disclosure, as follows:

[0098] In step S801, the first flow rate of the slit carrier gas introduced into the reactor chamber is determined based on the MCLT level of the first epitaxial wafer.

[0099] In step S802, the second epitaxial wafer is manufactured based on the slit carrier gas with the first flow rate; where the MCLT of the second epitaxial wafer is greater than or equal to 2000μs. In a case that the MCLT of the second epitaxial wafer is less than the first threshold, step S803 is performed.

[0100] In step S803, the resistivity uniformity of the epitaxial layer of the second epitaxial wafer is confirmed. In a case that the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer is greater than the second threshold, step S804 is performed. In a case that the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer is less than the second threshold, step S805 is performed.

[0101] In step S804, the resistivity uniformity of the epitaxial layer of the second epitaxial wafer is controlled by adjusting the first power ratio and the second power ratio. If adjusting the first power ratio and the second power ratio may make the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer less than the second threshold, then step S805 is performed. If adjusting the first power ratio and the second power ratio may not make the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer less than the second threshold, then the second flow rate of the slit carrier gas introduced into the reactor chamber is re-determined, and step S802 is repeated until the first characteristic value characterizing the resistivity uniformity of the epitaxial layer of the second epitaxial wafer is less than the second threshold.

[0102] In step S805, after the MCLT and resistivity uniformity of the epitaxial layer of the second epitaxial wafer meet the requirements, the thickness uniformity of

the epitaxial layer of the second epitaxial wafer is confirmed. In a case that the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer is greater than the predetermined third threshold, step S806 is performed. In a case that the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer is less than the predetermined third threshold, step S807 is performed.

[0103] In step S806, the thickness uniformity of the epitaxial layer of the second epitaxial wafer is controlled by adjusting the gas flow ratio during the epitaxial deposition process. In a case that the second characteristic value characterizing the thickness uniformity of the epitaxial layer of the second epitaxial wafer is less than the predetermined third threshold by adjusting the gas flow ratio during the epitaxial deposition process, step S807 is performed.

[0104] In step S807, in a case that the MCLT of the second epitaxial wafer, the resistivity uniformity of the epitaxial layer, and the thickness uniformity of the epitaxial layer all meet the requirements, the production and manufacturing of the second epitaxial wafer begins.

[0105] In addition, this disclosure also provides an epitaxial wafer, which is manufactured by the epitaxial deposition method according to the aforementioned technical solution, and minority carrier lifetime of the epitaxial wafer is greater than or equal to 2000μs.

[0106] In some examples, a first characteristic value of the epitaxial wafer is less than or equal to 2.7%, and a second characteristic value is less than or equal to 0.65%, where the first characteristic value is used to characterize resistivity uniformity of an epitaxial layer of the epitaxial wafer, and the second characteristic value is used to characterize thickness uniformity of the epitaxial layer of the epitaxial wafer.

[0107] In this disclosure, the terms “first”, “second”, etc., are used merely for descriptive purposes and should not be considered restrictive. Furthermore, although this disclosure has been described with reference to exemplary embodiments, it should be understood that the present application is not limited to the specific embodiments

described and shown herein. Various changes may be made to the exemplary embodiments by those skilled in the art without departing from the scope defined by the claims of the present application.

[0108] It should be noted that the technical solutions described in the embodiments of this disclosure can be combined arbitrarily without conflict.

[0109] The above description is merely a specific embodiment of the present application, but the scope of protection of the present application is not limited thereto. Any changes or substitutions that can be easily conceived by those skilled in the art within the scope of the technology disclosed in the present application should be included within the scope of protection of the present application. Therefore, the scope of protection of the present application should be determined by the scope of protection of the claims.

What is claimed is:

1. An epitaxial deposition method, wherein the epitaxial deposition method comprises:

performing a minority carrier lifetime test on a first epitaxial wafer to obtain minority carrier lifetime of the first epitaxial wafer;

determining a first gas flow rate of slit carrier gas introduced into a reactor chamber in a case that the minority carrier lifetime of the first epitaxial wafer is less than a predetermined first threshold;

manufacturing a second epitaxial wafer based on the slit carrier gas with the first gas flow rate; wherein minority carrier lifetime of the second epitaxial wafer is greater than or equal to 2200μs.

2. The epitaxial deposition method according to claim 1, wherein the first gas flow rate of the slit carrier gas is 20slm to 35slm.

3. The epitaxial deposition method according to claim 1, wherein the epitaxial deposition method further comprises:

obtaining a first characteristic value characterizing resistivity uniformity of an epitaxial layer of the second epitaxial wafer based on resistivities at different locations on the epitaxial layer of the second epitaxial wafer;

in a case that the first characteristic value is greater than a predetermined second threshold, adjusting a first power ratio and a second power ratio during an epitaxial deposition process according to a resistivity at a center location and a resistivity at an edge location on the epitaxial layer of the second epitaxial wafer; wherein, the first power ratio refers to a ratio of a power of a heating component at a center location above the reactor chamber to a sum of powers of heating components at locations above the reactor chamber other than the center location above the reactor chamber; the second power ratio is a ratio of a power of a heating component at a center location below the reactor chamber to a sum of powers of heating components at locations below the reactor chamber other than the center location below the reactor chamber;

acquiring an epitaxial wafer obtained through remanufacturing the second epitaxial wafer according to the adjusted first power ratio and the adjusted second power ratio.

4. The epitaxial deposition method according to claim 3, wherein an adjustment range of the first power ratio is 66% to 82%, and an adjustment range of the second power ratio is 16% to 20%.

5. The epitaxial deposition method according to claim 4, wherein in a case that the first power ratio and the second power ratio increase or decrease synchronously, and the first power ratio is adjusted by a first adjustment magnitude and the second power ratio is adjusted by a second adjustment magnitude, a ratio of the first adjustment magnitude to the second adjustment magnitude is in a range of 3:1 to 5:1.

6. The epitaxial deposition method according to any one of claims 3 to 5, wherein the in a case that the first characteristic value is greater than a predetermined second threshold, adjusting a first power ratio and a second power ratio during an epitaxial deposition process according to a resistivity at a center location and a resistivity at an edge location on the epitaxial layer of the second epitaxial wafer comprises:

in a case that the first characteristic value is greater than the second threshold,

increasing the first power ratio and the second power ratio in a case that the resistivity at the center location is greater than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer; or

decreasing the first power ratio and the second power ratio in a case that the resistivity at the center location is less than the resistivity at the edge location of the epitaxial layer of the second epitaxial wafer.

7. The epitaxial deposition method according to claim 3, wherein the epitaxial deposition method further comprises:

after acquiring the epitaxial wafer obtained through remanufacturing, determining a second gas flow rate of the slit carrier gas introduced into the reactor chamber in a case that the first characteristic value of the epitaxial layer of the epitaxial

wafer obtained through remanufacturing is greater than the second threshold; wherein the second gas flow rate is less than the first gas flow rate, and the second gas flow rate is 20slm to 35slm;

acquiring an epitaxial wafer obtained through additional remanufacturing based on the slit carrier gas with the second gas flow rate; wherein, the first characteristic value of the epitaxial wafer obtained through additional remanufacturing is less than the second threshold.

8. The epitaxial deposition method according to claim 1, wherein the epitaxial deposition method further comprises:

detecting a thickness of an epitaxial layer of the second epitaxial wafer to obtain a second characteristic value characterizing thickness uniformity of the epitaxial layer of the second epitaxial wafer;

adjusting a gas flow ratio during an epitaxial deposition process in a case that the second characteristic value is greater than a predetermined third threshold; wherein, the gas flow ratio is a ratio of a gas flow rate of a reaction gas at the center location of the reactor chamber to a gas flow rate at a first gas inlet in the reactor chamber.

9. The epitaxial deposition method according to claim 8, wherein the adjusting a gas flow ratio during an epitaxial deposition process in a case that the second characteristic value is greater than a predetermined third threshold comprises:

increasing the gas flow ratio in a case that a thickness at the center location is less than a thickness at the edge location of the epitaxial layer; or

decreasing the gas flow ratio in a case that the thickness at the center location is greater than the thickness at the edge location of the epitaxial layer.

10. An epitaxial wafer, wherein the epitaxial wafer is manufactured by the epitaxial deposition method according to any one of claims 1 to 9, and minority carrier lifetime of the epitaxial wafer is greater than or equal to 2200μs.

11. The epitaxial wafer according to claim 10, wherein a first characteristic value of the epitaxial wafer is less than or equal to 2.7%, and a second characteristic value is less than or equal to 0.65%, wherein the first characteristic value is used to

characterize resistivity uniformity of an epitaxial layer of the epitaxial wafer, and the second characteristic value is used to characterize thickness uniformity of the epitaxial layer of the epitaxial wafer.