

METHODS AND SYSTEMS FOR ULTRA WIDEBAND (UWB) RECEIVERS

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application claims the benefit of priority from United States Provisional Patent Application 62/819,834 entitled “Methods and Systems for Ultra Wideband (UWB) Receivers” filed March 18, 2019; the entire contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

[002] This invention relates to ultra-wideband wireless communication systems and more particularly ultra-wideband receivers for such ultra-wideband wireless communication systems.

BACKGROUND OF THE INVENTION

[003] Ultra-Wideband (UWB) technology is a wireless technology for the transmission of large amounts of digital data as modulated coded impulses over a very wide frequency spectrum with very low power over a short distance. Such pulse based transmission being an alternative to transmitting using a sinusoidal wave which is then turned on or off, to represent the digital states, as employed within today’s wireless communication standards and systems such as IEEE 802.11 (Wi-Fi), IEEE 802.15 wireless personal area networks (PANs), IEEE 802.16 (WiMAX), Universal Mobile Telecommunications System (UMTS), Global System for Mobile Communications (GSM), General Packet Radio Service (GPRS), and those accessing the Industrial, Scientific and Medical (ISM) bands, and International Mobile Telecommunications-2000 (IMT-2000).

[004] UWB systems are well-suited to short-distance applications in a variety of environments, such as depicted in Figure 1 including peripheral and device interconnections, as exemplified by first residential environment 110, sensor networks, as exemplified by second residential environment 120, control and communications, as exemplified by industrial environment 130, medical systems, as exemplified by medical imaging 150, and personal area networks (PAN), as exemplified by PAN 140. Due to low emission levels permitted by regulatory agencies such UWB systems tend to be short-range indoor applications but it would be evident that a variety of other applications may be considered where such regulatory restrictions are relaxed and / or not present

addressing military and civilian requirements for communications between individuals, electronic devices, control centers, and electronic systems for example.

[005] Accordingly, it would be beneficial for UWB transmitters, UWB receivers and UWB transceivers to accommodate and adapt to what are commonly referred to as inaccuracies, errors, or issues within the implemented electronics, hardware, firmware, and software.

[006] Accordingly, it would be beneficial for receivers to accommodate offsets in absolute frequency between their frequency source and that within the transmitter.

[007] It would be further beneficial for the UWB radios to employ modulation coding schemes that are more efficient with respect to power, data bits per pulse transmitted, and enabled operation at higher output power whilst complying with regulatory emission requirements.

[008] It would be further beneficial for the UWB receivers to accommodate drift within their own electronics arising from phase locked loop and/or from relative clock frequency offsets of the remote transmitter and local receiver.

[009] It would be further beneficial for UWB devices to support a ranging function over a range and with an accuracy that are not limited by the low frequency master clock employed within these devices to enable their operation with ultra-low power consumption.

[0010] Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to mitigate limitations within the prior art relating to ultra-wideband wireless communication systems and more particularly ultra-wideband receivers for such ultra-wideband wireless communication systems.

[0012] In accordance with an embodiment of the invention there is provided a UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and
the signal processing circuit comprising:

an RF front end circuit comprising:

- a first amplifier coupled to the antenna;
- a first filter coupled to the output of the first amplifier; and
- a mixer coupled to the output of the first filter and receiving a clock signal;
- first and second intermediate frequency processing circuits each coupled to one of an in phase output port and a quadrature output port of the mixer;
- a summation circuit coupled to the outputs of the first squaring circuits within the first and second intermediate frequency processing circuits; and
- a third intermediate frequency processing circuit coupled to the output of the summation circuit.

[0013] In accordance with an embodiment of the invention there is provided a UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and
the signal processing circuit comprising:

an RF front end circuit comprising:

- a first amplifier coupled to the antenna;
- a first filter coupled to the output of the first amplifier; and
- a mixer coupled to the output of the first filter and receiving a clock signal;
- a first intermediate frequency processing circuit coupled to an in phase output port of the mixer;
- a second intermediate frequency processing circuits coupled to the quadrature output port of the mixer;
- a third intermediate frequency processing circuit coupled to the output of first intermediate frequency processing circuit; and
- a fourth intermediate frequency processing circuit coupled to the output of the second intermediate frequency processing circuit.

[0014] In accordance with an embodiment of the invention there is provided a method of encoding data for transmission comprising merging at least a first pulse N-bit symbol with a second pulse N-bit symbol to generate an R-pulse 2N-bit Encoded Bundle Pulse Modulation (EDPM) symbol, wherein R and N are positive integers greater than or equal to 2.

[0015] In accordance with an embodiment of the invention there is provided a method of encoding data for transmission comprising:

receiving a M bits of data to be transmitted;

establishing an M-bit encoding scheme for transmission of the M bits of data;

generating a pulse bundle for transmission in dependence upon the M bits of data; and

transmitting the pulse bundle into a time slot of 2^M time slots.

[0016] In accordance with an embodiment of the invention there is provided a method of encoding data for transmission comprising:

receiving digital data to be transmitted;

encoding the digital data to be transmitted;

determining whether a number of a first symbol or a set of first symbols within the encoded data exceeds a predetermined threshold;

upon determining that the number of the first symbol or a set of first symbols within the encoded data exceeds a predetermined threshold inverting the encoded data to generate data for transmission;

upon determining that the number of the first symbol or a set of first symbols within the encoded data does not exceed a predetermined threshold using the encoded data to generate the data for transmission;

providing a first portion of a data packet for transmission defining whether the encoded data has been inverted or not;

providing the data for transmission as a second portion of the data packet for transmission.

[0017] In accordance with an embodiment of the invention there is provided a clock controller comprising:

a first input port for receiving a symbol clock;

a second input port for receiving a delayed version of the symbol clock;

a third input port for receiving a remove clock pulse signal from a controller forming part of a wireless device also comprising the clock controller;

a fourth input port for receiving an add clock pulse signal from the controller;

a first output port for generating a second symbol signal for the wireless device in dependence upon the symbol clock, the add clock pulse signal and the remove clock pulse signal; and

a second output port for generating a symbol signal in dependence upon at least the add clock pulse signal.

[0018] In accordance with an embodiment of the invention there is provided a clock controller comprising:

providing a first symbol clock to a controller; and

providing the controller, the controller for determining in dependence upon synchronous digital inputs when to insert an extra clock pulse into a second symbol clock generated by the controller from the first symbol clock and when to remove or suppress a clock pulse from the second symbol clock.

[0019] In accordance with an embodiment of the invention there is provided a method comprising:

providing a wireless receiver receiving first data to be decoded;

establishing a first integration window of a plurality of integration windows for an energy based detector forming part of the wireless receiver which processes the received first data from which second data is decoded;

processing the analog-to-digital converter (ADC) code values of the N last '0's within the received first data for the first integration window and the ADC code values of the N last '1's within the received first data for the first integration window to generate a first coarse metric of received signal-to-noise ratio;

establishing a second coarse metric of received signal-to-noise ratio for a second integration window of the plurality of integration windows, the second integration window of the plurality of integration windows being an integration window prior to the first integration window of the plurality of integration windows;

establishing a third coarse metric of received signal-to-noise ratio for a third integration window of the plurality of integration windows, the third integration window of the plurality of integration windows being a subsequent integration window to the first integration window of the plurality of integration windows;

determining in dependence upon the first coarse metric of received signal-to-noise ratio, the second coarse metric of received signal-to-noise ratio, and the third coarse metric of received signal-to-noise ratio whether to digitally select a different a current integration window for the energy based detector from the first integration window of the plurality of integration

windows to either the second integration window of the plurality of integration windows or third integration window of the plurality of integration windows.

[0020] In accordance with an embodiment of the invention there is provided a method comprising:

establishing a first phase relating to a first wireless signal received from a first node at a second node;

establishing a second phase of a second wireless signal received by the first node from the second node;

establishing a result in dependence upon an average of the first phase and an average of the second phase;

establishing a phase relating to a time of flight of wireless signals propagating between the first node and second node;

correcting the phase relating to the time of flight for a first delay within a first receiver forming part of the second node and a second delay within a second receiver forming part of the first node;

establishing a distance in dependence upon the phase relating to the time of flight and an integer number of clock cycles of delay relating to the time between a predetermined point in the transmission of the first wireless signal and a predetermined point in the receipt of the second wireless signal.

[0021] Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

[0023] Figure 1 depicts applications of UWB transmitters, receivers, and systems according to embodiments of the invention;

[0024] Figure 2 depicts a block diagram of a UWB transmitter according to an embodiment of the invention;

[0025] Figure 3A depicts a block diagram of a UWB transmitter according to an embodiment of the invention supporting biphasic phase scrambling;

[0026] Figure 3B depicts a block diagram of a UWB transmitter according to an embodiment of the invention employing dynamically configurable and programmable pulse sequences;

[0027] Figure 3C depicts schematically a multi-pulse symbol UWB protocol according to an embodiment of the invention;

[0028] Figure 4 depicts a block diagram of a UWB receiver according to an embodiment of the invention;

[0029] Figure 5 depicts a receiver circuit schematic for a UWB receiver / transceiver according to an embodiment of the invention;

[0030] Figure 6 depicts a circuit schematic for a UWB transceiver according to an embodiment of the invention;

[0031] Figure 7A depicts a circuit schematic of a UWB receiver according to an embodiment of the invention;

[0032] Figure 7B depicts a circuit schematic of a UWB receiver according to an embodiment of the invention;

[0033] Figure 8 depicts an example of 4-bit double PPM encoding scheme according to an embodiment of the invention;

[0034] Figure 9 depicts a comparison of prior art encoding schemes and new encoding schemes according to embodiments of the invention;

[0035] Figure 10 depicts an example of a 5-bit double PPM encoding scheme according to an embodiment of the invention;

[0036] Figure 11 depicts a schematic circuit of a clock pulse controller according to an embodiment of the invention;

[0037] Figure 12 depicts the tolerance to clock drift for UWB receivers with and without digital phase tracking according to an embodiment of the invention;

[0038] Figure 13 depicts schematically a data exchange of symbol / pattern information (integration window energy distribution) to communicate the received signal phase according to an embodiment of the invention;

[0039] Figure 14 depicts energy detection according to an embodiment of the invention employing 2 accumulators per integration window as depicted in Figure 14 where Accumulator #1 does not show a significant correlation whilst Accumulator #2 does show a significant correlation for a specific ranging pulse pattern indicating a phase delay of the ranging signal;

[0040] Figure 15 depicts averaging with respect to range determination according to an embodiment of the invention using a common centroid strategy across the time dimension for improved accuracy, especially against linear clock drift;

[0041] Figures 16 and 17 depict a two-step ranging process according to an embodiment of the invention where a ranging signal is transmitted and after a known number of bits the transmitter changes the transmission pattern to transmit only the center pulse where an N-path filter is temporarily disabled so that the integration windows are shrunk around the estimated signal phase; and

[0042] Figure 18 depicts a schematic with respect to receiver and transmitter side processing with accumulators upon a preamble pattern according to an embodiment of the invention.

DETAILED DESCRIPTION

[0043] The present invention is directed to ultra-wideband wireless communication systems and more particularly ultra-wideband receivers for such ultra-wideband wireless communication systems.

[0044] The ensuing description provides exemplary embodiment(s) only, and is not intended to limit the scope, applicability or configuration of the disclosure. Rather, the ensuing description of the exemplary embodiment(s) will provide those skilled in the art with an enabling description for implementing an exemplary embodiment. It being understood that various changes may be made in the function and arrangement of elements without departing from the spirit and scope as set forth in the appended claims.

[0045] 0. IMPULSE RADIO ULTRA WIDEBAND SYSTEM

[0046] As discussed *supra* UWB offers many potential advantages such as high data rate, low-cost implementation, and low transmit power, ranging, multipath immunity, and low interference. The Federal Communications Commission (FCC) regulations for UWB reserved the unlicensed frequency band between 3.1GHz and 10.6GHz for indoor UWB wireless communication system wherein the low regulated transmitted power allows such UWB systems to coexist with other licensed and unlicensed narrowband systems. Therefore, the limited resources of spectrum can be used more efficiently. On the other hand, with its ultra-wide bandwidth, an UWB system has a capacity much higher than the current narrowband systems for short range applications. Two possible techniques for implementing UWB communications are Impulse Radio (IR) UWB and multi-carrier or multi-band (MB) UWB. IR-UWB exploits the transmission of ultra-short (of the order of nanosecond) pulses, although in some instances in order to increase the processing gain more than one pulse represents a symbol. In contrast MB-UWB systems use orthogonal frequency division multiplexing (OFDM) techniques to transmit the information on each of the sub-bands. Whilst OFDM has several good properties, including high spectral efficiency, robustness to RF and multi-path interferences. However, it has several drawbacks such as up and down conversion, requiring mixers and their associated high power consumption, and is very sensitive to inaccuracies in frequency, clock, and phase. Similarly, nonlinear amplification destroys the orthogonality of OFDM. Accordingly, MB-UWB is not suitable for low-power and low cost applications.

[0047] In contrast IR-UWB offers several advantages, including unlicensed usage of several gigahertz of spectrum, offers great flexibility of spectrum usage, and adaptive transceiver designs can be used for optimizing system performance as a function of the data rate, operation range, available power, demanded quality of service, and user preference. Further, multi-Gb/s data-rate transmission over very short range is possible and due to the ultra-short pulses within IR-UWB it is very robust against multipath interference, and more multipath components can be resolved at the receiver in some implementations, resulting in higher performance. Further, the ultra-short pulses support sub-centimeter ranging whilst the lack of up and down conversion allows for reduced implementation costs and lower power transceiver implementations. Beneficially, ultra-short pulses and low power transmissions make IR-UWB communications hard to eavesdrop upon.

[0048] An IR-UWB transmitter as described below in respect of embodiments of the invention in with reference to Figures 2 and 3 respectively exploits an on-demand oscillator following a pulse generator in order to up-convert the pulses from the pulse generated whilst avoiding the requirement of a separate mixer. Implementable in standard CMOS logic both the pulse generator and the on-demand oscillator are digitally tunable in order to provide control over the pulse bandwidth and center frequency. Further, by exploiting a digitally controlled ring oscillator for the on-demand oscillator the IR-UWB transmitter is designed to allow very quick frequency adjustments on the order of the pulse repetition rate (PRR). Beneficially this technique provides the same advantages as MB-OFDM in respect of spectrum configurability, achieved by sequentially changing the transmitted spectrum using a frequency hopping scheme, whilst maintaining the benefits of IR-UWB. Further, by providing advanced duty cycling with fast power up time combined with On-Off Shift Keying (OOK) modulation the IR-UWB according to embodiments of the invention allows significant reductions in power consumption by exploiting the low duty cycle of a UWB symbol and the fact that only half the symbols require sending energy.

[0049] In addition to defining the operating frequency range for UWB systems the different regulatory bodies all specify and enforce a specific power spectral density (PSD) mask for UWB communications. A PSD mask as may be employed in respect of embodiments of the invention is the FCC mask for which mask data are summarized in Table 1 below for the 3100MHz-10600MHz (3.1GHz-10.6GHz) range.

Frequency Range	Indoor EIRP Limit (dBm/MHz)	Outdoor EIRP Limit (dBm/MHz)
<960	-49.2	-49.2
960-1610MHz	-75.3	-75.3
1610-1990MHz	-53.3	-63.3
1990-3100MHz	-51.3	-61.3
3100-10600MHz	-41.3	-41.3
>10600MHz	-51.3	-61.3

Table 1: FCC Masks for Indoor – Outdoor for Different Frequency Bands

[0050] Accordingly, it would be evident that the upper limit of -41.3 dB/MHz across the 3.1GHz-10.6GHz frequency range is the same limit imposed on unintentional radiation for a given frequency in order not to interfere with other radios. Basically, for a given frequency, the UWB radio operates under the allowed noise level which creates the relationship presented in Equation (1) between E_p , the transmitted energy per pulse, the maximum spectral power S , the bandwidth B , the bit rate R_b and the number of pulses per bits N_{ppb} .

$$E_p \cdot N_{ppb} \cdot R_b \leq S \cdot B \quad (1)$$

[0051] The IEEE has published a few standards for a physical layer (PHY) for UWB radio in Personal Area Networks (IEEE 802.15.4a-2007), Body Area Networks (IEEE 802.15.4a-2007) and Radio-Frequency Identification (IEEE 802.15.4f-2012). These standards use mostly relatively large pulses resulting in relatively narrow bandwidth which is up-converted to a specific center frequency in order to fill predetermined channels. The data is encoded using pulse-position-modulation (PPM) and bi-phasic shift keying (BPSK) is used to encode redundancy data. Every bit consists of one or more pulses scrambled in phase depending on the target data rate. These standards allow considerable flexibility on channel availability and data rates. The standard also defines the preamble, headers for the data packet and ranging protocol.

[0052] These IEEE standards are designed with multiple users in mind and use different channels to transmit the data, thereby putting a heavy constraint on pulse bandwidth and limiting the transmitted energy. Prior art on non-standard transmitter attempts to make better use of the available spectrum by using narrow pulses, which therefore have a larger bandwidth thereby increasing the maximum transmitted energy according to Equation (1). Accordingly, these transmitters are non-standard and were also designed for different data rates, frequencies, pulse width, etc. Additionally, they also used various encoding schemes, most notably PPM, OOK or BPSK.

[0053] Within the work described below the inventors have established improvements with respect to UWB systems, UWB transmitters and energy based UWB receivers which are capable of generating and adapting to a variety of IR-UWB pulses and bit encoding schemes thereby supporting communications from both IR-UWB transmitters compliant to IEEE standards as well as those that are non-standard. These improvements are made with respect to UWB transmitters,

UWB receivers, UWB transceivers and UWB systems such as those described and depicted by the inventors within WO/2019/000075 “Energy Efficient Ultra-Wideband Impulse Radio Systems and Methods” (PCT/CA2018/000,135 filed June 29, 2018); WO 2016/191851 “Systems and Methods for Spectrally Efficient and Energy Efficient Ultra-Wideband Impulse Radios with Scalable Data Rates” (PCT/CA2016/000,161 filed May 31, 2016); and WO/2015/103,692 “Systems and Methods Relating to Ultra Wideband Broadcasting comprising Dynamic Frequency and Bandwidth Hopping” (PCT/CA2015/000,007, filed January 7, 2015).”

[0054] 1. IR-UWB TRANSMITTER CIRCUIT

[0055] Referring to Figure 2 there is depicted schematically an exemplary architecture for an IR-UWB transmitter 200 according to embodiments of the invention which is composed of five main blocks plus the antenna. First a programmable impulse is produced by a pulse generator 230 at clocked intervals when the data signal from AND gate 210 is high based upon control signals presented to the AND gate 210. The pulses from the pulse generator 230 are then up-converted with a programmable multi-loop digitally controlled ring oscillator (DCRO) 240. The output from the DCRO 240 is then coupled to a variable gain amplifier (VGA) 250 in order to compensate for any frequency dependency of the pulse amplitude. Finally, a driver 260 feeds the antenna 270, overcoming typical package parasitics, such as arising from packaging the transceiver within a quad-flat no-leads (QFN) package. In order to further reduce the power consumption of the IR-UWB transmitter (IR-UWB-Tx) 200 according to embodiments of the invention a power cycling controller 220 dynamically switches on or off these functional blocks when the data signal is low.

[0056] Now referring to Figure 3A there is depicted schematically a block diagram 300 of an exemplary IR-UWB transmitter according to embodiments of the invention supporting biphasic phase scrambling. In comparison to the IR-UWB transmitter 200 in Figure 2 for an IR-UWB according to embodiments of the invention without biphasic phase shifting rather than being composed of five main blocks plus the antenna the Biphasic Phase Shifting IR-UWB (BPS-IR-UWB) transmitter comprises 6 main blocks. First a programmable impulse is produced by a pulse generator 330 at clocked intervals when the data signal from AND gate 310 is high based upon control signals presented to the AND gate 310. The pulses from the pulse generator 330 are then up-converted with a programmable multi-loop digitally controlled ring oscillator (DCRO) 340. The output from the DCRO 340 is then coupled to a dual-output amplifier (VGA) 350 both in

order to compensate for any frequency dependency of the pulse amplitude but also to generate dual phase shifted output signals that are coupled to a switch 360 which selects one of the two signals to couple to the output power amplifier (driver) 380 under the action of the switch control signal “S” applied to the switch 360. Note that a similar phase selection scheme could be implemented by affecting the startup conditions of DCRO 340 in order to provide the two phases. This would preclude the need for switch 360 at the cost of an added control startup condition control signal on DCRO 340.

[0057] The output power amplifier 380 feeds the antenna 370, overcoming typical package parasitics, such as arising from packaging the transceiver within a quad-flat no-leads (QFN) package. In order to reduce the power consumption of the BPS-IR-UWB transmitter represented by block diagram 300 according to an embodiment of the invention a power cycling controller 320 dynamically switches on or off these functional blocks when the data signal “PC” is low. Accordingly, a BPS-IR-UWB transmitter according to embodiments of the invention transmits pulses with or without phase shift based upon the control signal “S” applied to switch 360. If this control signal is now fed from a random data generator or a pseudo-random data generator then the resulting pulses coupled to the antenna of the BPS-IR-UWB transmitter will be pseudo-randomly or randomly phase shifted.

[0058] Now referring to Figure 3B there is depicted schematically a block diagram 3000 of an exemplary IR-UWB transmitter according to embodiments of the invention. As depicted a Pulse Pattern block 3010 holds a configuration for the pulses used to represent the current symbol. From the symbol-rate clock (i.e. 20 MHz), multiple phases are generated by a Delay Locked Loop (DLL) 3030. The rising edge of each clock phase represents the start of one pulse in the symbol pulse bundle. A multiplexer 3020 is triggered by the edges of the clock phases and selects the configuration of the current pulse out of the Pulse Pattern block 3010. A pulse generator (Pulser) 3050 generates pulses with a pulse width set by the multiplexer 3020 and enables the Digitally Controlled Oscillator (DCO) 3040 and Power Amplifier (PA) 3060. When enabled, the DCO 3040 generates a Gaussian shaped pulse with frequency set by the multiplexer 3020, which is then amplified by the PA 3060 and radiated by the antenna 3070.

[0059] Accordingly, the Pulse Pattern block 3010 establishes the pulses for a symbol or sequence of symbols. In this manner updating the Pulse Pattern block 3010 adjusts the pulse sequence

employed for each symbol and accordingly the Pulse Pattern block 3010 may be dynamically updated based upon one or more factors including, but not limited to, network environment data, predetermined sequence, date, time, geographic location, signal-to-noise ratio (SNR) of received signals, and regulatory mask.

[0060] Referring to Figure 3C there is depicted schematically a multi-pulse symbol UWB protocol according to an embodiment of the invention. Referring to first image 3100A there is depicted a bit 3160 comprising a series of sub-pulses 3160A to 3160C which are each at frequencies $f_1; f_2; f_3$. Accordingly, the multi-pulse spectrum 3180 of a symbol (bit 3160) is depicted in second image 3100B as obtained conceptually (phase scrambling is omitted for clarity) by summing the individual pulse spectra of the sub-pulses 3160A to 3160C, which increases the bandwidth whilst increasing the total symbol duration, in contrast with single-pulse prior art methods, whilst maintaining the maximum power below the UWB mask 3120. This allows the symbol energy to be maximized while relaxing the timing requirements and level of synchronization required at the receiver. An arbitrary number of pulses with different sets of parameters may be included within a bundle to tailor the pulse spectrum to a given requirement.

[0061] 2. IR-UWB RECEIVER

[0062] Referring to Figure 4 there is depicted schematically the architecture of an IR-UWB receiver 400 according to embodiments of the invention. Accordingly, the signal from an IR-UWB transmitter is received via an antenna 410 and coupled to a low noise amplifier (LNA) 420 followed by first amplifier 430 wherein the resulting signal is squared by squaring circuit 440 in order to evaluate the amount of energy in the signal. The output of the squaring circuit 440 is then amplified with second amplifier 450, integrated with integration circuit 460 and evaluated by a flash ADC 470 to generate the output signals. Also depicted is Power Cycling Controller 480 which, in a similar manner to the power cycling controller 220 of IR-UWB transmitter 200 in Figure 2, dynamically powers up and down the LNA 420, first and second amplifiers 430 and 450 respectively, squaring circuit 440, and flash ADC 470 to further reduce power consumption in dependence of the circuit's requirements.

[0063] Referring to Figure 5 there is depicted a schematic of a receiver 500 according to an embodiment of the invention. The RF signal from the antenna 510 is initially amplified by a Low

Noise Amplifier (LNA) 520 before being passed to a two stage RF amplifier (AMP1) 530. A first squaring mixer (MIX1) 540 multiplies the signal with itself to convert to the Intermediate Frequency (IF). A three-stage Variable Gain Amplifier (VGA) 550 amplifies the signal further and implements a bandpass filter function. The VGA 550 output is then coupled to a second squaring mixer (MIX2) 560 which down-converts the signal to the baseband frequency. A parallel integrator (INT1 and INT2) sums the signal energy, which is digitized by the Analog-to-Digital Converters (ADC1 and ADC2) within a digital processor (not depicted for clarity).

[0064] 3. IR-UWB RECEIVER

[0065] As described within WO/2019/000075 and WO 2016/191851 the inventors have established design parameters of millisecond range start-up time from sleep mode and microsecond range start-up time from idle mode by establishing a custom integrated DC/DC converter and duty cycled transceiver circuitry that enables fast circuit start-up / shut-down for optimal power consumption under low (1 kbps) and moderate data rates (10 Mbps).

[0066] In order to sustain good energy efficiency, the elements of a total UWB transceiver, such as depicted with transceiver 600 in Figure 6 according to embodiments of the invention, has been designed for low static sleep current and fast startup/sleep times. Referring to Figure 6, a battery ($3.0\text{ V} \leq V_{BATT} \leq 3.6\text{ V}$) (not depicted for clarity) powers a low-frequency crystal oscillator 615, sleep counter 620 and bandgap reference 610, all of which are typically always operational although the bandgap reference 610 could be duty cycled within other embodiments of the invention without altering the scope of the claimed invention). Their power consumption limits the minimum power consumption of the system to sub-microwatt level. An integrated buck DC-DC converter 605 is powered by the battery when the system is not in sleep mode, and this provides the supply voltage to the rest of the system with high conversion efficiency. The startup time of the DC-DC converter 605 is on the order of several symbol periods in order to minimize wasted energy. Between sleep periods, the PLL 655 is active to provide the base clock for the system. The receiver 625 and DLL 660 have dedicated power down controls and are only activated during frame transmission / reception. Further, the transmitter is also power cycled through its all-digital architecture which is not depicted as having a separate control. The power consumption of the digital synthesized blocks is low due to the low base clock (e.g. 20 MHz).

[0067] In principle, a power-cycled transceiver achieves linear scaling of power consumption with data rate, thus achieving constant energy efficiency. With a fixed frame size, multiple data rates are obtained by adjusting the length of the sleep period, with the maximum attainable data rate determined by the symbol rate in the frame itself. In order to preserve energy efficiency, the power consumption during sleep must be lower than the average power consumption. For high data rates, powering down the PLL is not required when its consumption does not significantly degrade the overall efficiency. For low data rates, the whole system except the bandgap reference, crystal oscillator, and sleep counter can be shut down during sleep mode. In this case, the millisecond range startup time of the PLL can be insignificant compared to the sleep period, and overall efficiency is also not significantly degraded.

[0068] As depicted the UWB transceiver 600 also comprises a receive / transmit switch 690 coupled to the antenna to selectively couple the transmitter 6000 or receiver 625 to the antenna during transmission and receipt respectively. The UWB transceiver 600 also comprises a spectrum configuration circuit 665 (equivalent to Pulse Pattern 3010 in transmitter 3000 in Figure 3B), PHY Processing circuit 650, Link Controller 645, Buffer and Interface circuit 640, and PHY Formatting circuit 635. The UWB transceiver 600 communicates via Link Controller 645 to the Client 605. As such, Link Controller 645 may communicate using a wired protocol to Client 605, for example.

[0069] 4. Uncertain IF Receiver for UWB Receivers

[0070] Referring to Figure 7A there is depicted a UWB receiver 700A according an embodiment of the invention allowing the UWB receiver 700A to detect pulses received by an antenna 705 which have been transmitted by a transmitter according to an embodiment of the invention. Accordingly, the antenna receives a pulsed UWB signal, which consists of a carrier signal that is pulsed according to a fast envelope, for example with ± 2 ns pulse width. This received signal is coupled initially to a Low Noise Amplifier (LNA) 710 which amplifies the signal wherein the amplified signal is bandpass filtered by first filter 715 to suppress out-of-band interferers. Optionally, other amplifiers can be present at this RF stage prior to mixer 720. First filter 715 may, for example, be a bandpass filter. Optionally, LNA 710 and first filter 715 may be a tunable LNA to perform filtering to a sub-band (or sub-bands) currently in use in order to improve noise performance.

[0071] Next, an in-phase quadrature mixer 720 multiplies the received filtered and amplified signal with a square clock, thus down converting the pulses to an uncertain intermediate frequency, IF1, where the IF1 frequency is the difference between the pulse carrier frequency and the clock frequency. As the UWB receiver 700A is an energy receiver the paths in quadrature are required (90 degrees out of phase) such that the total energy of the pulse is preserved where the in-phase, I, and quadrature signals, Q, are split between the two paths in accordance with the phase difference between RF signal and clock. Even if UWB Receiver 700A was not an energy receiver both paths would be required to avoid the scenario of using a single path, either I or Q, and the received RF signal and clock being out of phase to yield no signal in the single path.

[0072] The IF1 signals within the I and Q arms are processed by first and second signal processing circuits 740 and 750 respectively. Each of these comprises an amplifier 725 such that the mixed and down converted IF1 signals are amplified and these are then filtered by a second filter 730, for example a sharp low pass or bandpass filter, which is established in dependence upon a UWB band. Within embodiments of the invention the UWB may be a full band or a predetermined portion of a wider band. For example, considering the ISM band according to FCC regulations then the full band may be 3.1GHz to 10.6GHz or it may be a predetermined portion thereof. Optionally, within some embodiments of the invention the transmitter may cycle through a plurality of sub-bands of the band according to a sequence, where a sub-band may for example be 500MHz where the cyclic sequence is a defined number of sub-bands, e.g. 4, 8, 16 or another integer number, within the overall band, e.g. the FCC regulated unlicensed frequency band between 3.1GHz and 10.6GHz. Accordingly, the receiver either employs filters having bandwidths covering the full band or a sub-band. When the filter bandwidths are a sub-band then the transmitter may communicate an initial sequence within a synchronization process and update the sequence in the pre-amble to align the receiver to the transmitter. Optionally, the filters may be reconfigurable filters employing N-path techniques or other re-configurable filtering techniques.

[0073] This method according to embodiments of the invention allows for multiple UWB signals within a sequence of defined sub-bands within an overall wider bands such that the receiver is operating upon a small bandwidth rather than the full bandwidth over which the transmitter and receiver can operate. Accordingly, in embodiments of the invention the filters dynamically set or selected according to the band sequence. Alternatively, in other embodiments of the invention

exploiting non-banded transmitters and receivers the second filter 730 may be established to pass the full down converted bandwidth.

[0074] The output of each second filter 730 is then squared by a squaring operation performed by first squarer 735 in order to extract the instantaneous power on that path. The outputs from the first and second signal processing circuits 740 and 750 respectively are summed into the total instantaneous power by summation circuit 745. The output of the summation circuit 745 is then coupled to an amplification stage 755. This amplified signal is then filtered by third filter 760, squared by a squaring operation performed by second squarer 765 and then integrated with integrator 770. The amplification stage 755, third filter 760, second squarer 765 and integrator 770 forming a third signal processing circuit 780.

[0075] The signal from summation circuit 745 follows the envelope of the pulse signal with the RF carrier removed. Accordingly, without knowing the exact pulse carrier frequency, it is still possible to receive the signal whilst applying sharp filtering. The amplification within each of the first and second signal processing circuits 740 and 750 together with that of the third signal processing circuit 780 may be fixed gain amplifiers or variable gain amplifiers. In embodiments of the invention where variable gain is employed then this can be employed to amplify the signal to full strength which in conjunction with the bandpass filtering allows removal of narrowband interfering signals.

[0076] Now referring to Figure 7B there is depicted a UWB receiver 700B according an embodiment of the invention. Wireless signals received at the antenna 705 are coupled initially to a Low Noise Amplifier 710 which amplifies the signal wherein the amplified signal is bandpass filtered by first filter 715 to suppress out-of-band interferers. Optionally, other amplifiers can be present at this RF stage prior to mixer 720. First filter 715 may, for example, be a bandpass filter.

[0077] Next, an in-phase quadrature mixer 720 multiplies the received filtered and amplified signal with a square clock, thus down converting the pulses to an uncertain intermediate frequency, IF1, where the IF1 frequency is the difference between the pulse carrier frequency and the clock frequency. As with UWB receiver 700A the I and Q outputs from the mixer 720 are coupled to first and second signal processing circuits 740 and 750 respectively but rather than being summed the outputs of the first and second signal processing circuits 740 and 750 respectively are coupled to the third and fourth signal processing circuits 7100 and 7200 respectively. The I O/P and Q O/P

outputs from the third and fourth signal processing circuits 7100 and 7200 respectively may then be coupled directly to one or more digital processing circuits prior to being summed to generate the total power and perform the decision making. Optionally, these outputs may be summed and then converted to digital signals.

[0078] 5. Encoded Bundle Pulse Modulation (EBPM) Coding Schemes

[0079] Measures of merit for a wireless link exploiting wireless radios according to embodiments of the invention are channel bandwidth efficiency (which is tightly correlated to energy efficiency), spectral efficiency and link robustness. Channel bandwidth efficiency is achieved by minimizing the number of symbol periods required to exchange a given amount of information which also translates into a faster and lower latency link. Optimizing spectral efficiency allows for the transmission of more information for a given amount of electromagnetic radiation for which there are regulatory limits globally and there is always a compromise between data rate and link margin (robustness) for the wireless radio because of these regulatory limits. The less pulses ('1's after encoding) per bit of information there are (with the worst possible pattern of data), the better the spectral efficiency. Link robustness is effectively determined by the signal-to-noise ratio (SNR), resiliency to interferences and correlates with the Hamming distance between each symbol of the modulation coding scheme.

[0080] On/Off Keying (OOK) is a prior art modulation format exploiting a direct translation of bit of information to a pulse bundle (1 = pulses, 0 = no pulses). The inventors have also established what they refer to as "Invertible" OOK or I-OOK which exploits the fact that the regulatory limits on spectral emissions apply on the data pattern that causes the maximum possible amount of emitted wireless radiation. For regular OOK, that pattern is "11111..." which causes one pulse to be emitted per bit of information. However, for all patterns of data for which there is more "1"s than "0"s, then if the pattern is entirely bit-flipped the amount of emitted wireless radiation is reduced. Now, with the addition of a single bit in addition to the data bits then the receiver knows whether the pattern was flipped or not by the transmitter. In this manner the I-OOK encoding scheme has twice the spectral efficiency for no degradation in link robustness and almost no loss in bandwidth and energy efficiency, with the exception of an extra header field.

[0081] It would be evident that whilst the discussion above and below in respect of binary data comprising "1"s and "0"s the method is applicable to other systems wherein the decision is made

as to whether a symbol or a set of symbols requiring increased wireless emission relative to another symbol or set of symbols exceeds a threshold wherein once that threshold is exceeded then the data to be transmitted is inverted.

[0082] Pulse Position Modulation (PPM) is a form of signal modulation in which M message bits are encoded by transmitting a single pulse in one of 2^M possible time shifts. Accordingly, 1-bit PPM is a simple differential encoding of bits into a pair of time slots (symbol periods) where the energy integrated in one time slot is subtracted relative to the other. Whilst this means double the energy and bandwidth is employed the Hamming distance per bit is also doubled. It is called PPM because it works in a very similar way to one (the position of the pulse bundle dictates the bit of information) except it is entirely managed digitally. Extending this to a 2-bit PPM encoding scheme uses two bits of information to define the position of one pulse bundle between four time slots (symbol periods). This encoding scheme offers twice the spectral efficiency and the same bandwidth efficiency for a marginal loss in link robustness in practice over 1-bit PPM. This can be extended to 4-bit PPM wherein one pulse (bundle) is located somewhere within 16 possible pulse positions.

[0083] 2-bit PPM distributes only one set of pulses over 4 symbol clock periods to encode 2-bits of information in 4 pulse positions. For example, data bits “11 01” become “0010 0100” where 2 sets of pulses are employed for 4 bits but requires 8 clock cycles to perform. Accordingly, in four clock cycles there are only 4 possible combinations instead of 16 with OOK. The result is double the energy consumption of OOK, double the channel bandwidth occupied, and double the latency. This becomes exponentially worse as the number of bits per symbol increases.

[0084] The inventors have established what they refer to as Encoded Bundle Pulse Modulation (EBPM) to alleviate the energy and bandwidth burden of 2-bit PPM for the same spectral efficiency. By positioning two sets of pulses within each bundle window instead of one set of pulses the inventors can greatly increase the number of possible combinations such that more bits can be represented. With two separate 2-bit windows then patterns like “1010 0000” are invalid. However, with the novel encoding scheme of the inventors with double pulses merged such windows lead to more combinations. This can be generalized as given by Equation (1) where n is the effective number of bits per symbol, p is the number of pulse positions, and b_0 and b_1 are the respective number of empty (0) and occupied (1) pulse positions.

$$n = \log_2 \frac{p!}{b_0! \times b_1!} \quad (1)$$

[0085] According, considering 2-bit PPM then as given by Equation (2) the ratio of the number of bits per symbol over the number of pulse positions, a bit-per-pulse ratio of 2 is $2/4 = 0.5$. For 2-pulse 4-bit EBPM (referred to as 4-bit Double EBPM by the inventors) for the same number of pulses and pulse positions we get more than 4 bits of information. The inventors have also considered whether the 2 pulse 4-bit PPM symbol can fit into 6 pulse positions rather than 8.

$$n = \log_2 \frac{p!}{b_0! \times b_1!} = \log_2 \frac{4!}{2! \times 1!} = 2 \quad (2)$$

$$n = \log_2 \frac{p!}{b_0! \times b_1!} = \log_2 \frac{8!}{6! \times 2!} = 4.807 \quad (3)$$

[0086] Referring to Figure 8 there is depicted an example of a 4-bit Double EBPM encoding scheme according to an embodiment of the invention with a minimum Hamming distance of 2.

[0087] Now referring to Figure 9 there is depicted a comparison of prior art encoding schemes, these being OOK, 1-bit PPM, 2-bit PPM and 4-bit PPM, with the new encoding schemes according to embodiments of the invention, namely 4-bit Double EBPM and Invertible OOK. The assumptions for energy/bit were that the transmitter energy cost is independent of packet data. The link robustness is qualitatively estimated based upon Hamming distance, number of bits affected, etc. As noted above, Invertible OOK requires some simple packet pre-processing.

[0088] Referring to Figure 10 there is depicted a 5-bit Double EBPM encoding scheme yielding 1.6nJ/bit using the same analysis parameters as employed in calculating the data in Figure 9 and achieves 2.5 bit/pulse transmission. The encoding scheme presented is not necessarily an optimal encoding scheme as some signaling configurations may be more vulnerable to noise-induced bit errors where there are significant number of 0s such as encoded patterns “01000000”, “00100000”, “0001000”, “00001000”, and “10000000.”

[0089] Accordingly, 4-bit Double EBPM supports operating in wireless emission constrained applications. Essentially, with the constraints on the average power imposed by regulatory bodies, there is a maximum number of "pulse bundles" that can be sent every millisecond. Accordingly, 4-bit Double EBPM allows for more data to be sent for the same amount of emitted "pulse bundles" (or energy) compared to OOK and 1-bit PPM. It would be evident to one of skill in the art that the concept can be extended to N as one can increase the order of the PPM to extend the concept.

[0090] 6. PLL Drift and Digital Phase Tracking

[0091] 6A PLL Drift

[0092] Within the receivers described by the inventors in WO/2019/000075 and WO 2016/191851 a single integration window was described as being selected from multiple integration windows, described as 4, which was then “locked”, for example when a synchronization word is detected. By “locked” the inventors means that the selection (or choice) between the multiple integration windows is locked (maintained) when no phase tracking is performed

[0093] However, offsets in the underlying clock applied to the phase locked loop (PLL) result in gradual phase drifting of the receiver system. Accordingly, the optimum integration window can shift, for example during the receipt of long packets or with infrequent synchronization of the receiver to the transmitter. Accordingly, the inventors have established observing adjacent windows during receipt of the packet after synchronization in order to allow the integration window employed to follow this drift.

[0094] With respect to the receiver circuit then the additional elements include:

- accumulators for a running average of ‘1’s and ‘0’s of the current window and the two adjacent ones;
- management logic to keep track of how many ‘1’s and ‘0’s were integrated in the average; and
- a clock pulse controller to manage transitions between the first phase of one clock cycle and a last phase of the same clock cycle.

[0095] The clock pulse controller manages therefore where the transmitter runs slightly faster or slower than the receiver. For example, where the transmitter runs slightly faster than the receiver then the receiver might have to process two symbols/timeslots within one clock period which therefore requires that an additional clock pulse is inserted. In this scenario the first clock pulse takes care of the first ADC value (first integration window) and the second clock pulse the last integration window.

[0096] Optionally, the additional elements may also include decision threshold update logic using outputs from the aforementioned accumulators.

[0097] Now referring to Figure 11 there is depicted a schematic circuit of a clock pulse controller according to an embodiment of the invention. As depicted the clock pulse controller receives the PLL clock and a tapped delay line copy of the PLL clock having 90° phase offset relative to the PLL clock. However, where there is no duty cycle constraint of the output clock signal then the delay lines does not need to be tapped as “any” delay will do. By “any” the inventors mean that it is much less than half a clock cycle but long enough, e.g. 2-3ns. 90° phase offset is required only to maintain 50% of the clock duty cycle.

[0098] The PLL clock is coupled to first and second D-type flip-flops 1110 and 1120 respectively. The Q output of the second D-type flip-flop 1120 is combined with the PLL clock by OR gate 1150 as well as being coupled back to an inverted input of a first AND gate 1130, the output of which is coupled to the D input of the second D-type flip-flop 1120. The other input of AND gate 1130 being coupled to what the inventors refer to as “skip beat” signal. The output of the first D-type flip-flop 1110 is combined via a second AND gate 1140 together with the 90° phase offset copy of the PLL clock. The outputs of the OR gate 1150 and second AND gate 1140 providing the inputs to an Exclusive NOR 1160 to provide what the inventors refer to as a “modem clock” signal. The output of the second AND gate also provides what the inventors refer to as an “extra beat” signal. The D input of the first D-type flip-flop 1110 is coupled to a signal the inventors refer to as “add extra beat.” Optionally, AND gate 1130 may be omitted but has been included within the embodiment of the invention depicted in Figure 11 to ensure that the wireless radio employing the circuit does not get “stuck” with all of its clock edges suppressed.

[0099] Accordingly, the “modem clock” is the clock signal provided to the rest of the digital circuitry. The “skip beat” signal eliminates a clock edge in the cases where the remote transmitter is too slow. The “add extra beat” signal inserts an extra clock pulse in the cases where the remote transmitter is too fast and forces the receiver to take two symbols within one clock cycle. The “extra beat” signal tells the modem which of the rising edges is produced by the extra pulse (which also defines when to change integration window selection).

[00100] It would be evident that the clock pulse controller is a simple and small logic circuit to address the issues discussed above. Beneficially, it does not impact currently established logic within a wireless modem in the modem significantly to accommodate skipping a beat or processing two symbols at once as the altered clock signal already does it. With respect to the accumulators

for generating the running averages of the current window and the two adjacent ones then there is already a per-window accumulator used in window selection that is unused after window selection is done as it is only used before the synchronization word is received. Accordingly, these accumulators already exist within the logic of the modem for preamble detection and analysis purposes.

[00101] Whilst the embodiment of the invention described in respect of Figures 10 and 11 relates to a clock source within a wireless radio exploiting a PLL clock it would be evident that the concept is applicable to any symbol clock employed to provide the outlined functionality.

[00102] *6B. Digital Phase Tracking*

[00103] Within the receivers described by the inventors in WO/2019/000075 and WO 2016/191851 the receiver is synchronized to the transmitter during an initial “configuration” phase. However, it would be beneficial to track subsequent clock drift between the transmitter and receiver provided. The assumption is that the drift is slow and predictable enough. Accordingly, the phase tracking methodology established by the inventors allows the receiver to decide when to switch between integration windows and change the bit decision threshold to keep receiving the drifting signal during a packet reception. Figure 12 depicts the tolerance to clock drift for both the standard receiver, not implementing a method of digital phase tracking according to an embodiment of the invention, and a receiver implementing a method of digital phase tracking according to an embodiment of the invention. This method can also relax timing requirements for the system, enabling lower power and lower cost timing circuitry to be used (e.g. low cost 32kHz quartz crystal).

[00104] Figure 12 depicts allowable clock drift in parts per million (ppm) for a UWB receiver when receiving packets with 528 bits of payload. Each dotted line is the dropped (or missing) packet rate for a fixed channel attenuation as a function of the frequency offset between a transmitter and a receiver's symbol clock expressed in parts-per-million when phase tracking is disabled, meaning the receiver picks the same integration window for all symbols of the same packet at the beginning, assumes the signal will stay aligned with this window and pays no attention to adjacent integration windows. Continuous lines are the same conditions with phase tracking enabled where we can see that the region of tolerance to clock drifting roughly quadruples below the 10 % packet error rate mark.

[00105] The digital phase tracking exploits a phase tracking algorithm which tracks signal drifts by subtracting the analog-to-digital converter (ADC) code values of the 16 last '0's (vacant pulse slots) from the ADC code values of the 16 last '1's for a given integration window. The algorithm does this for the currently chosen integration window from which the packet is decoded as well as for its two adjacent integration windows. This produces the latest averaged difference between the energy levels of '1's and '0's (a coarse metric of SNR) for the current integration window together with the window leading and the window lagging. For embodiments of the receiver such as described in WO/2019/000075 and WO 2016/191851 and the clock rates etc. described within these then the leading window is leading by approximately 12 ns and the one lagging behind lags by approximately 12 ns. The algorithm by comparing these SNR figures can establish that the current integration window it is using to decode the packet is no longer optimal and decide to continue decoding the incoming packet from another integration window. If the device transmitting the packet has a local symbol clock running slightly slower than the receiver's clock for which the packet is destined to, the more the receiver keeps decoding the packet from the same integration window, the more will the received signal be strong through the integration window lagging the one currently used by the receiver. The same happens to the integration window leading the one being used by the decoder if the transmitter's clock runs faster.

[00106] It would be evident that within the embodiments of the invention that the integration windows whilst being described as “lagging” or “leading” with respect to other integration windows may or may not overlap portions of other integration windows. Optionally, within another embodiment of the invention the phase tracking algorithm may ignore the ADC code values of the 16 last '0's (vacant pulse slots).

[00107] In order to account for the need to skip a symbol clock or to add one respectively, a clock controller allows the receiver to jump from the last integration window to the first or from the first to the last. In the former case which can happen when the transmitter's clock runs slower, the clock controller will suppress one clock pulse of the symbol clock to pause the receiver's modem for one symbol period to keep it synchronized within one symbol clock cycle with the transmitter. In the latter case, an extra clock pulse is inserted to make the receiver's modem process two symbols within one symbol clock cycle so that the receiver catches up to the transmitter. It would be evident that the controller to achieve this is similar to the one described above in respect of Figure 11 and

PLL drift except that now the signals “add extra beat” and “skip beat” are now generated by the digital decision circuitry implementing the digital phase tracking algorithm which uses the ADC values from the 16 last '0's (vacant pulse slots) and 16 last '1's for the current integration window and the integration windows leading and lagging.

[00108] Accordingly, it would be evident that the digital phase tracking may be implemented with:

- digital accumulators for summing ADC values of last 16 ‘1’s and last 16 ‘0’s of the current window and the two adjacent ones;
- management logic to manage storing ADC values to the digital accumulators and counting received ‘1’s and ‘0’s to stop adding until both accumulated 16 counts and then reset;
- decision threshold update logic using outputs from the aforementioned accumulators; and
- the clock pulse controller to manage changes in phase selection between the first and last phase.

[00109] Whilst the embodiments of the invention have been described with respect to 16 “1”s and 16 “0”s it would be evident to one of skill in the art that the number of bits for which ADC values are digitally accumulated may vary within other embodiments of the invention. Optionally, the number of bits accumulated may be dynamically set by a receiver controller in dependence upon one or more factors including, but not limited to, packet size, established rate of clock drift from shifting integration windows, and a measure of the overall signal SNR.

[00110] 7. RTT Ranging Algorithm

[00111] Amongst the beneficial features and/or applications of UWB devices would be an ultra-low power RF ranging device. Within WO 2016/191851 the inventors have presented a couple of ranging concepts based upon time of flight information established by a first device in dependence upon a signal sent to a second device from which an echo back signal received, known as Round-Trip Time (RTT) ranging.

[00112] With this idea, it is possible to implement coarse ranging capability with ultra-low power UWB devices such as described by the inventors previously which are optimized for digital

communication. Traditional Round-Trip Time (RTT) ranging devices operate by time-accurate echoing from one node (device) of the ranging signal exchange. Within this one node (device) sends the ranging signal that the other node must echo as soon as it receives it and especially with as predictable and accurate as the echoing delay can be and the first node use the delay between the instant it sends the ranging signal and the instant it receives the echo to compute what is the distance between the two communicating nodes. Thus, the echo delay has to be very accurately fixed and usually, the echoing node runs on a fast sampling clock to allow it to have a finer time granularity to decide when to send back the echo. With this finer granularity, the echoing delay varies less which allows the first node who sent the incidental signal to get a more accurate measure of the distance between it and the echoing node. The slower the sampling clock, the more inaccurate the ranging devices will be.

[00113] As noted in WO/2019/000075 and WO 2016/191851 the UWB devices operate with a base symbol clock of only 20.48 MHz so accurate echoing delay is impossible. To overcome this, the ability to evaluate the time at which a pulse is received with the energy accumulated through the integration windows can be used to reach a coarse but still useful time-of-flight ranging capability. Instead of trying to repeat the signal with a precise echoing delay, the echoing node can measure what is the phase of the incidental signal it receives relative to its symbol clock, the same clock with which it launches the echo, and therefore it knows what its own echoing delay is for any given ranging signal despite not being able to correct it. Accordingly, the echoing node can communicate to its peer what was its echoing delay (through phase information) so that the peer subtracts the delay error to get a much more accurate measure of the distance between the two nodes than a 20 MHz symbol clock would normally enable.

[00114] Considering initially the granularity of a transceiver according to the embodiments of the invention within WO/2019/000075 and WO 2016/191851 then we find the following:

- Symbol/PLL period time = 48.8 ns (14.64 m / 48.03 feet); and
- Receiver's integration window = 12.2 ns (3.66 m / 12 feet); and
- Pulse repetition rate = ~4 ns (1.2 m / 3.94 feet); and
- Phase of pulse = ~0.1 ns (0.03 m / 0.1 feet).

[00115] With respect to control / detectability then we find the following:

- Symbol/PLL period time can be established through timers/counters;
- Receiver's integration window is detectable only;
- Pulse repetition rate is controllable through a transmitter pattern register; and
- Phase of pulse has no control / detection.

[00116] Considering base time resolution then this is ~4 ns on the transmitter side and ~12.2 ns on the receiver side. However, the distribution of energy between integration windows can give improved accuracy rather than just picking the window with the highest energy. The gain in precision is dependent upon:

- ADC resolution (quantization noise);
- averaging (EM noise);
- echoing imprecision; and
- clock drift.

[00117] When considering traditional time of flight ranging techniques then these are based upon a Time of Arrival (ToA) or Round-Trip-Time (RTT) technique. The former ToA technique requires an absolute time reference, for example provided by a global positioning signal from a global positioning system (GPS) which increases complexity as a GPS receiver must be integrated or requires strict synchronization. Due to the design of the inventor's wireless radios then this is not an option with 48.8 ns of master clock plus jitter. With the latter RTT technique a ranging signal is echoed by a remote (slave) transceiver which eliminates the need for an absolute time reference or synchronization but requires that the time delay in the remote transceiver is constant and deterministic as possible.

[00118] Accordingly, to echo a signal within wireless radios according to embodiments of the invention and those previously disclosed by the inventors with low frequency master clocks then it is necessary to compute the relative phase of the signal with the PLL clock (with integration windows) and reply back to the master the ranging signal with pulse positions that match the phase, thereby changing the transmitted pattern to include a value. This raises several issues as the echo alone introduces a delay uncertainty of ± 2 ns which is the transmitter pattern resolution, any bit corruption will mean a phase cannot be reproduced and the use of a delay line to provide intermediate timing generally has poor accuracy.

[00119] 7A. Alternate Ranging Scheme

[00120] The inventors have therefore established an alternative ranging scheme as an alternative to both ToA and RTT exploiting a transmitter pattern at a known setting and calculating the clock phase difference in both directions. Hence, this is based upon the following:

- say Φ_{OFFSET} is the phase offset between clocks of Node A and Node B, which whilst unknown but does not change significantly over a short period of time ($\Phi_{\text{OFFSET}} = \Phi_B - \Phi_A$);
- ranging signals going from Node A to Node B arrive at Node B with phase $\Phi_{AB} = \text{Phase(ToF)} + T_{\text{filters}} - \Phi_{\text{OFFSET}}$;
- ranging signals going from Node B to Node A arrive at Node A with phase $\Phi_{BA} = \text{Phase(ToF)} + T_{\text{filters}} + \Phi_{\text{OFFSET}}$;
- therefore $\text{Phase(ToF)} + T_{\text{filters}} = (\Phi_{AB} + \Phi_{BA}) / 2$; and
- T_{filters} be known to a sufficient degree of precision, this being constant and intrinsic to the system

[00121] This technique exploits the premise that the phase matches delay linearly and accordingly matches the distance. Such a concept is depicted in Figure 13 using the data exchange in symbol / pattern information (integration window energy distribution) to communicate the received signal phase. The delays K0 and K2 are constant and known whilst K1 varies within a single clock cycle because of the synchronization event coming from Node B. Beneficially, this technique does not require accurate echoing, it has no dependency on transmitter pattern resolution or limitation to its ~4 ns resolution, no drawbacks from corrupted pulses, and has no requirement to receive during the first pulses. However, the delay line accuracy affects both the transmitter and receiver whilst PLL cumulative jitter (~4 ns over a 30 μ s period) and crystal clock drift (~0.6 ns over 30 μ s) are factors. Further, the ADC quantization noise is significant especially with 3-bit ADCs such as described within WO/2019/000075 and WO 2016/191851. However, most importantly the technique does not allow distinguishing between clock cycles such that the maximum range would be limited to the speed of light times the duration of a clock cycle (48.828 ns) or 14.64 meters (approximately 50 feet). This is certainly sufficient for a wide range of

applications such as within residential environments, localized environments within other environments such as offices, retail, etc.

[00122] However, in other applications extending the range limit would be beneficial and accordingly the inventors have addressed and considered improvements.

[00123] Improvement #1 – Periodicity: By making the ranging signal out of a synchronization pattern, such as a short synchronization word for example. If we consider the pattern “0110” then this spans $4 \times 48.8 \text{ ns} = \sim 195 \text{ ns} = \sim 58.5 \text{ meters} (\sim 192 \text{ feet})$. Accordingly, if we increase the number of digital accumulators to 8 for averaging then this is sufficient for this pattern. For each integration window, the energy is accumulated using 2 accumulators per window as depicted in Figure 14 which depicts the scenario where Accumulator #1 does not show a significant correlation while Accumulator #2 does show a significant correlation for the particular ranging pulse pattern of “...01100110...” indicating the phase delay of the ranging signal” Accordingly, with 8 accumulators and determining which has the strongest signal and its polarity allows the wireless radio controller to distinguish between 16 consecutive integration windows. Further, the uncertainty can be reduced by using the adjacent windows energy distribution. Beneficially, this improvement produces the additional benefit of cancelling both ADC and integration window offsets.

[00124] Improvement #2 - Delay-line: Digital calibration of the delay line has very limited precision. However, whilst the uncertainty can be improved by providing a DLL and more power this is counter-productive to the goal of low power consumption despite improving both the transmitter pattern dependent processing and receiver integration windows precision. However, only employing the early pulses helps for transmitter timing.

[00125] Improvement #3 – Clock Drift: Within this improvement the assumption is that the clocks of the transmitter and receiver drift linearly relative to each other. Accordingly, as depicted in Figure 15 averaging is employed using a common centroid strategy across time dimension for better accuracy, especially against linear clock drift.

[00126] Improvement #4 – Narrow Integration Windows: Within the receivers described and depicted within WO 2016/191851 an N-path filter is employed within the receiver chain. However, if the N-path filter is disabled then a two-step process with narrow integration windows such as depicted within Figures 16 and 17 may be employed. Considering Figure 16 and the first step then

the process begins by starting to transmit the same ranging signal as discussed previously but then after a known number of bits the transmitter changes the transmission pattern to transmit only the center pulse. Now, with the N-path filter temporarily disabled the integration windows are shrunk around the estimated signal phase whilst adjusting gain as depicted in Figure 17. Accordingly, the resolution is improved. It would be evident that whilst the specific embodiment described employs an N-path filter that the principles apply to the disabling of all IF and baseband filtering within the receiver chain.

[00127] Improvement #5 – Integration Window Sweep: Within exemplary receivers described previously with respect to WO/2019/000075 and WO 2016/191851 a single integration window is probed per PLL clock cycle. However, alternatively the receiver could be configured to sweep across all four (or the number implemented) integration windows observing and averaging one at a time. Exploiting this methodology then if the signal is not visible in the first chosen window it is not problem as it is only the signal pattern phase is all that is needed, and hence first / initial bits can be missed. This Integration Window Sweep being applicable in wireless radios according to embodiments of the invention where only one integration window ADC value is observable at any point in time.

[00128] Accordingly, when a Serial Peripheral Interface (SPI) is employed to transfer data from the receiver for processing then the SPI master is changed at specific instants where typically 16 SPI clock cycles are required per change. It would be beneficial to synchronize the SPI clock to the PLL clock within the receiver / transceiver. Further, if a microcontroller is employed then operation is required real time as it relies upon the exact and constant number of clock cycle operations both for the SPI and for general purpose input / output (GPIO) sample and control of the microcontroller.

[00129] *7B. Periodic Non-Data Signal Based Ranging*

[00130] Within this embodiment of the invention the wireless radios employ a periodic non-data signal which is required by the receiver to capture and average the ranging signal into an energy distribution between phase windows. In order to implement this a set of accumulators are required to store the digitized values of this energy distribution and a fixed (ideally very short) delay between the transmitter and receiver ranging signals. Within a transceiver according to embodiments of the invention where an auto-reply function or feature is enabled then this allows

the transceiver to immediately reply to a transmission with another of its own. Accordingly, the delay between the two is short and deterministic.

[00131] The preamble of each packet as described within WO/2019/000075 and WO 2016/191851 is a periodic signal which allows the receiver to simply capture and average the signal to get an energy distribution indicating the phase of that signal relative to its own clock. Further, wireless radios according to embodiments of the inventors already possess accumulators dedicated to collecting energy per integration window during receipt of the preamble. However, the requirements for these accumulators are insufficient for this requirement and they are also required to properly track the preamble and adjust the gain. Accordingly, additional accumulators are needed in parallel.

[00132] Referring to Figure 18 there is depicted schematically implementation of this embodiment of the invention for the receiver and transmitter side processing with accumulators identified as Phase A to Phase D. These being the ADC output signals within the wireless radio circuit(s), for example within an ASIC, that are input into a wireless modem according to embodiments of the invention. These correspond to integration window energy values for each symbol clock cycle and not to accumulators. Within the scenario depicted in Figure 18 the ADCs are 3-bit ADCs and hence these values range 0 to 7. It would also be evident that Figure 18 is a simplified representation wherein only the “1”s of the preamble are shown, whereas normally there would be ‘0’s between each.

[00133] However, the preamble pattern has a periodicity of only two symbols which yields to some ambiguity within the algorithm applied as one phase value could be the result of two very different distances. By implementing a register or register field within a node receiving the reply, which the inventors refer to as a receiver waited (RX_WAITED) register, then the node is aware of how many clock cycles of delay there have been between the end of the original transmitted packet and the end of the synchronization word of the reply which provides for disambiguation. Whilst the RX_WAITED provides for a very coarse ranging metric the phase information fulfills the need for finer accuracy. Accordingly, adding additional accumulators to provide this phase information is a low impact enhancement to the transceiver design. Optionally, the accumulator values could be made available as read-only register fields in common with those for the other

accumulators. An algorithm providing the required functionality would probably require firmware intervention to exchange all the necessary information.

[00134] Transceivers according to embodiments of the invention would exploit a procedure comprising:

[00135] “Agree” with the node the transceiver wishes to compute the distance to on a timeslot to exchange ranging information;

- Enable an auto-reply function (all settings apply to both sides);
- Set the preamble length to an appropriate value, the longer the preamble length the more averaging is applied but also more clock drift; and
- (Optional) employ minimum possible packet size so as to minimize the delay between the preambles being exchanged as ranging signals (e.g. no PPM, no forward error correction (FEC), a packet size equal to 1, no cyclic redundancy check, etc.).

[00136] After packet exchange for phase information gathering, read RX_WAITED (replying side only) and read phase information (both sides). This allows the nodes to exchange the information read with the other node and to collect all the information for processing all on one side. For flexibility the ranging equation may be implemented in the firmware.

[00137] Based upon potential applications including, for example, embedded sensors requiring very low power and low complexity design as well as other power and cost limited system the receiver has to be configurable digitally using very simple control circuitry. Furthermore, the integration window has to be easily tunable considering the high sensitivity of energy detection receiver to proper integration window synchronization. Different modulation, data rates and burst length will also need to change the shape of the integration duty cycle and all the power management must properly keep in synchronization.

[00138] Specific details are given in the above description to provide a thorough understanding of the embodiments. However, it is understood that the embodiments may be practiced without these specific details. For example, circuits may be shown in block diagrams in order not to obscure the embodiments in unnecessary detail. In other instances, well-known circuits, processes, algorithms, structures, and techniques may be shown without unnecessary detail in order to avoid obscuring the embodiments.

[00139] Implementation of the techniques, blocks, steps and means described above may be done in various ways. For example, these techniques, blocks, steps and means may be implemented in hardware, software, or a combination thereof. For a hardware implementation, the processing units may be implemented within one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), processors, controllers, micro-controllers, microprocessors, other electronic units designed to perform the functions described above and/or a combination thereof.

[00140] The foregoing disclosure of the exemplary embodiments of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many variations and modifications of the embodiments described herein will be apparent to one of ordinary skill in the art in light of the above disclosure. The scope of the invention is to be defined only by the claims appended hereto, and by their equivalents.

[00141] Further, in describing representative embodiments of the present invention, the specification may have presented the method and/or process of the present invention as a particular sequence of steps. However, to the extent that the method or process does not rely on the particular order of steps set forth herein, the method or process should not be limited to the particular sequence of steps described. As one of ordinary skill in the art would appreciate, other sequences of steps may be possible. Therefore, the particular order of the steps set forth in the specification should not be construed as limitations on the claims. In addition, the claims directed to the method and/or process of the present invention should not be limited to the performance of their steps in the order written, and one skilled in the art can readily appreciate that the sequences may be varied and still remain within the spirit and scope of the present invention.

The current application discloses the following concepts:

1. A UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and

the signal processing circuit comprising:

an RF front end circuit comprising:

a first amplifier coupled to the antenna;

a first filter coupled to the output of the first amplifier; and

a mixer coupled to the output of the first filter and receiving a clock signal;

first and second intermediate frequency processing circuits each coupled to one of an in phase output port and a quadrature output port of the mixer;

a summation circuit coupled to the outputs of the first squaring circuits within the first and second intermediate frequency processing circuits; and

a third intermediate frequency processing circuit coupled to the output of the summation circuit.

2. The UWB receiver according to concept 1, wherein

each intermediate frequency processing circuit comprises:

a second amplifier receiving a down converted signal from the mixer;

a second filter coupled to the output of the second amplifier; and

a first squaring circuit for squaring a signal filtered by the second filter.

3. The UWB receiver according to concept 1, wherein

the third intermediate frequency processing circuit comprises:

a third amplifier receiving the output of the summation circuit;

a third filter coupled to the output of the third amplifier;

a second squaring circuit coupled to the third filter; and

an integration circuit coupled to the output of the second squaring circuit.

4. A UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and

the signal processing circuit comprising:

an RF front end circuit comprising:

- a first amplifier coupled to the antenna;
- a first filter coupled to the output of the first amplifier; and
- a mixer coupled to the output of the first filter and receiving a clock signal;
- a first intermediate frequency processing circuit coupled to an in phase output port of the mixer;
- a second intermediate frequency processing circuits coupled to the quadrature output port of the mixer;
- a third intermediate frequency processing circuit coupled to the output of first intermediate frequency processing circuit; and
- a fourth intermediate frequency processing circuit coupled to the output of the second intermediate frequency processing circuit.

5. The UWB receiver according to concept 4, wherein

each of the first and second intermediate frequency processing circuits comprises:

- a second amplifier receiving a down converted signal from the mixer;
- a second filter coupled to the output of the second amplifier; and
- a first squaring circuit for squaring a signal filtered by the second filter.

6. The UWB receiver according to concept 4, wherein

each of the third and fourth intermediate frequency processing circuits comprises:

- a third amplifier receiving the output of the summation circuit;
- a third filter coupled to the output of the third amplifier;
- a second squaring circuit coupled to the third filter; and
- an integration circuit coupled to the output of the second squaring circuit.

7. The UWB receiver according to concept 4, further comprising

- a first analog-to-digital converter (ADC) coupled to the output of the third intermediate frequency processing circuit; and
- a second ADC coupled to the output of the fourth intermediate frequency processing circuit.

8. A method of encoding data for transmission comprising:
merging at least a first pulse N-bit symbol with a second pulse N-bit symbol to generate an R-pulse 2N-bit Encoded Bundle Pulse Modulation (EDPM) symbol, wherein
R and N are positive integers greater than or equal to 2.

9. The method according to concept 8, wherein
at least one of:

the first pulse N-bit symbol and the second pulse N-bit symbol are a pair of a plurality
of pulse N-bit symbols combined to form the R-pulse 2N-bit EDPM symbol;
and
some generated R-pulse 2N-bit EDPM symbols comprise patterns which are invalid for
separate N-bit windows.

10. A method of encoding data for transmission comprising:
receiving a M bits of data to be transmitted;
establishing an M-bit encoding scheme for transmission of the M bits of data;
generating a pulse bundle for transmission in dependence upon the M bits of data; and
transmitting the pulse bundle into a time slot of 2^M time slots.

11. A method of encoding data for transmission comprising:
receiving digital data to be transmitted;
encoding the digital data to be transmitted;
determining whether a number of a first symbol or a set of first symbols within the encoded
data exceeds a predetermined threshold;
upon determining that the number of the first symbol or a set of first symbols within the
encoded data exceeds a predetermined threshold inverting the encoded data to generate
data for transmission;
upon determining that the number of the first symbol or a set of first symbols within the
encoded data does not exceed a predetermined threshold using the encoded data to
generate the data for transmission;
providing a first portion of a data packet for transmission defining whether the encoded data
has been inverted or not;

providing the data for transmission as a second portion of the data packet for transmission.

12. A clock controller comprising:

a first input port for receiving a symbol clock;

a second input port for receiving a delayed version of the symbol clock;

a third input port for receiving a remove clock pulse signal from a controller forming part of a wireless device also comprising the clock controller;

a fourth input port for receiving an add clock pulse signal from the controller;

a first output port for generating a second symbol signal for the wireless device in dependence upon the symbol clock, the add clock pulse signal and the remove clock pulse signal;
and

a second output port for generating a symbol signal in dependence upon at least the add clock pulse signal.

13. A method comprising:

providing a first symbol clock to a controller; and

providing the controller, the controller for determining in dependence upon synchronous digital inputs when to insert an extra clock pulse into a second symbol clock generated by the controller from the first symbol clock and when to remove or suppress a clock pulse from the second symbol clock.

14. A method comprising:

providing a wireless receiver receiving first data to be decoded;

establishing a first integration window of a plurality of integration windows for an energy based detector forming part of the wireless receiver which processes the received first data from which second data is decoded;

processing the analog-to-digital converter (ADC) code values of the N last '0's within the received first data for the first integration window and the ADC code values of the N last '1's within the received first data for the first integration window to generate a first coarse metric of received signal-to-noise ratio;

establishing a second coarse metric of received signal-to-noise ratio for a second integration window of the plurality of integration windows, the second integration window of the

plurality of integration windows being an integration window prior to the first integration window of the plurality of integration windows;
establishing a third coarse metric of received signal-to-noise ratio for a third integration window of the plurality of integration windows, the third integration window of the plurality of integration windows being a subsequent integration window to the first integration window of the plurality of integration windows;
determining in dependence upon the first coarse metric of received signal-to-noise ratio, the second coarse metric of received signal-to-noise ratio, and the third coarse metric of received signal-to-noise ratio whether to digitally select a different a current integration window for the energy based detector from the first integration window of the plurality of integration windows to either the second integration window of the plurality of integration windows or third integration window of the plurality of integration windows.

15. The method according to concept 14, wherein
the second integration window of the plurality of integration windows overlaps a first portion of the first integration window of the plurality of integration windows; and
the third integration window of the plurality of integration windows overlaps a second portion of the first integration window of the plurality of integration windows

16. The method according to concept 14, wherein
processing the ADC code values of the N last '0's and the ADC code values of the N last '1's comprises either:

subtracting the ADC code values of the N last '0's from the ADC code values of the N last '1's; or
ignoring the ADC code values of the N last '0's.

17. A method comprising
establishing a first phase relating to a first wireless signal received from a first node at a second node;
establishing a second phase of a second wireless signal received by the first node from the second node;

establishing a result in dependence upon an average of the first phase and an average of the second phase;
establishing a phase relating to a time of flight of wireless signals propagating between the first node and second node;
correcting the phase relating to the time of flight for a first delay within a first receiver forming part of the second node and a second delay within a second receiver forming part of the first node;
establishing a distance in dependence upon the phase relating to the time of flight and an integer number of clock cycles of delay relating to the time between a predetermined point in the transmission of the first wireless signal and a predetermined point in the receipt of the second wireless signal.

18. The method according to concept 17, wherein
at least one of the first signal and the second signal is a synchronization pattern employed in synchronizing the first node and second node to each other.

19. The method according to concept 17, wherein
determining the phase of the first signal and the second signal is established in dependence upon:

establishing a first estimate of the phase by employing a plurality N integration windows for which there are two accumulators per integration window to yield $2N$ consecutive integration windows; and
refining the first estimate in dependence upon the energy distribution between the integration window with the highest energy and its adjacent windows.

20. The method according to concept 17, further comprising
implementing a wait counter receiver to establish the integer number of clock cycles of delay; the predetermined point in the transmission of the first signal being the end of the first signal;
and
the predetermined point in the receipt of the second signal is the end of the second signal.

CLAIMS

What is claimed is:

1. A wireless receiver comprising:

a digital processor which executes a process.

2. The wireless receiver according to claim 1, further comprising

an energy based detector processing first data received by the wireless receiver from which second data is decoded where the energy based detector employs an integrator circuit providing integration within an integration window of a plurality of integration windows and an analog-to-digital converter (ADC) to convert the output of the integration circuit; wherein

the process executed by the digital processor comprises:

processing the analog-to-digital converter (ADC) code values of N last '0's within the received first data for a first integration window of the plurality of integration windows and the ADC code values of the N last '1's within the received first data for the first integration window plurality of integration windows to generate a first coarse metric of received signal-to-noise ratio;

processing the analog-to-digital converter (ADC) code values of N last '0's within the received first data for a second integration window of the plurality of integration windows and the ADC code values of the N last '1's within the received first data for the second integration window of the plurality of integration windows to establish a second coarse metric of received signal-to-noise ratio for the second integration window of the plurality of integration windows, the second integration window of the plurality of integration windows being an integration window of the plurality of integration windows immediately prior to the first integration window of the plurality of integration windows;

processing the analog-to-digital converter (ADC) code values of N last '0's within the received first data for a third integration window of the plurality of integration windows and the ADC code values of the N last '1's within the received first data for the third integration window of the plurality of integration windows to establish a third coarse metric of received signal-to-noise ratio for the third integration window of the plurality of

integration windows, the third integration window of the plurality of integration windows being an immediately subsequent integration window of the plurality of integration windows to the first integration window of the plurality of integration windows; and

establishing in dependence upon the first coarse metric of received signal-to-noise ratio, the second coarse metric of received signal-to-noise ratio, and the third coarse metric of received signal-to-noise ratio a current integration window for the energy based detector from the first integration window of the plurality of integration windows, the second integration window of the plurality of integration windows and the third integration window of the plurality of integration windows; and

N is a positive integer greater than or equal to 2.

3. The wireless receiver according to claim 2, wherein

the second integration window of the plurality of integration windows overlaps a first portion of the first integration window of the plurality of integration windows and the third integration window of the plurality of integration windows overlaps a second portion of the first integration window of the plurality of integration windows

4. The wireless receiver according to claim 2, wherein

processing the ADC code values of the N last '0's and the ADC code values of the N last '1's comprises either subtracting the ADC code values of the N last '0's from the ADC code values of the N last '1's or ignoring the ADC code values of the N last '0's.

5. The wireless receiver according to claim 2, wherein

the value of N is dynamically set by the digital processor in dependence upon at least one of a packet size of packets comprising the first data, a rate of clock drift established in dependence upon the timing of shifting integration windows within the plurality of integration windows and a measure of an overall signal SNR for the received first data.

6. The wireless receiver according to claim 1, wherein

the process executed by the digital processor establishes distance between a first node comprising the wireless receiver and a second node comprising another wireless receiver;

the process comprises:

establishing a first phase relating to a first wireless signal received from the first node at the second node;

establishing a second phase of a second wireless signal received by the first node from the second node;

establishing a result in dependence upon an average of the first phase and an average of the second phase;

establishing a phase relating to a time of flight of wireless signals propagating between the first node and second node;

correcting the phase relating to the time of flight for a first delay within the another wireless receiver within the second node and a second delay within the wireless receiver forming part of the first node;

establishing the distance in dependence upon the phase relating to the time of flight and an integer number of clock cycles of delay relating to the time between a predetermined point in the transmission of the first wireless signal and a predetermined point in the receipt of the second wireless signal; wherein

at least one of:

at least one of the first signal and the second signal is a synchronization pattern employed in synchronizing the first node and second node to each other; and

determining the phase of the first signal and the second signal is established in dependence upon:

establishing a first estimate of the phase by employing a plurality N integration windows for which there are two accumulators per integration window to yield $2N$ consecutive integration windows; and

refining the first estimate in dependence upon the energy distribution between the integration window with the highest energy and its adjacent windows; and

N is an integer greater than or equal to 2.

7. The wireless receiver according to claim 1, wherein
the process executed by the digital processor establishes a distance between a first node comprising the wireless receiver and a second node comprising another wireless receiver;
the process comprises:
establishing a first phase relating to a first wireless signal received from the first node at the second node;
establishing a second phase of a second wireless signal received by the first node from the second node;
establishing a result in dependence upon an average of the first phase and an average of the second phase;
establishing a phase relating to a time of flight of wireless signals propagating between the first node and second node;
correcting the phase relating to the time of flight for a first delay within the another wireless receiver within the second node and a second delay within the wireless receiver forming part of the first node;
establishing the distance in dependence upon the phase relating to the time of flight and an integer number of clock cycles of delay relating to the time between a predetermined point in the transmission of the first wireless signal and a predetermined point in the receipt of the second wireless signal; and
implementing a wait counter receiver to establish the integer number of clock cycles of delay;
wherein
the predetermined point in the transmission of the first signal is the end of the first signal; and
the predetermined point in the receipt of the second signal is the end of the second signal.

8. The wireless receiver according to claim 1, wherein
the process executed by the digital processor establishes a distance between a first node comprising the wireless receiver and a second node comprising another wireless receiver;
the process comprises:
establishing a first phase relating to a first wireless signal received from a first node at a second node;

establishing a second phase of a second wireless signal received by the first node from the second node;
 establishing a result in dependence upon an average of the first phase and an average of the second phase;
 establishing a phase relating to a time of flight of wireless signals propagating between the first node and second node;
 correcting the phase relating to the time of flight for a first delay within a first receiver forming part of the second node and a second delay within a second receiver forming part of the first node;
 establishing the range in dependence upon the phase relating to the time of flight and an integer number of clock cycles of delay relating to the time between a predetermined point in the transmission of the first wireless signal and a predetermined point in the receipt of the second wireless signal; wherein
 establishing the first phase relating to the first wireless signal received from the first node at the second node is established with a process comprising:
 transmitting a ranging signal from the first node comprising N bits;
 transmitting a pulse from the first node after a delay equivalent to a defined number of bits;
 receiving the ranging signal with a receiver comprising a multipath filter and detecting received energy within a plurality of integration windows, where the receiver forms part of the second node; and
 temporarily disabling the multipath filter after receipt of the ranging signal and increasing a gain of the receiver to detect the pulse whereby a duration of the integration windows employed by the receiver is reduced to provide increased resolution of detecting the pulse and accuracy of the first phase.

9. The wireless receiver according to claim 1, wherein

the process executed by the digital processor establishes a distance between a first node comprising the wireless receiver and a second node comprising another wireless receiver;
 the process comprises:
 establishing a first phase relating to a first wireless signal received from a first node at a second node;

establishing a second phase of a second wireless signal received by the first node from the second node;

establishing a result in dependence upon an average of the first phase and an average of the second phase;

establishing a phase relating to a time of flight of wireless signals propagating between the first node and second node;

correcting the phase relating to the time of flight for a first delay within a first receiver forming part of the second node and a second delay within a second receiver forming part of the first node;

establishing the range in dependence upon the phase relating to the time of flight and an integer number of clock cycles of delay relating to the time between a predetermined point in the transmission of the first wireless signal and a predetermined point in the receipt of the second wireless signal;

establishing an agreement between the first node and second node to a timeslot upon which to exchange ranging information; and

enabling an auto-reply feature upon the second node such that the second wireless signal is automatically provided in response to the first wireless signal.

10. The method according to claim 9, further comprising
setting a preamble length for each of the first wireless signal and the second wireless signal.

11. The method according to claim 9, wherein
the first wireless signal and the second wireless signal are transmitted independent of bits for forward error correction and other bits for one or more cyclic redundancy checks.