

Circuit arrangement for powering a load.

This Sheet Has Been Replaced



The invention relates to a circuit arrangement for powering a load.

US-PS 4,626,763 describes a motor control arrangement for controlling the speed of a motor as a function of a rectangular signal of variable frequency and of chopper pulses. In this arrangement a three-phase motor is energized with rectangular
5 voltages formed by a rectangular wave having a fundamental frequency corresponding to the motor speed and superposed pulses of variable width. These rectangular voltages are derived from a first rectangular signal whose frequency corresponds to six times the frequency or
10 speed of rotation of the motor and from a second signal whose frequency is high relative to the frequency of the first signal. The resulting voltages then have continuously constant values in some of the time intervals between each time two pulses of the first signal and vary as high-frequency rectangular pulses in other ones of these time intervals.

A similar arrangement with corresponding variations as a function of time of the voltages across the phases of a three-phase motor is also disclosed in US-PS 4,602,201.

15 In the circuit arrangements disclosed in said documents the frequency of the first signal determines the speed of the three-phase motors being driven. The frequency of the first signal is therefore varied in accordance with the desired or prevailing speed of the motor. For low speeds this results in low frequencies of the first signal and, consequently, large time intervals between the pulses forming this signal. Likewise, the individual voltages
20 across the motor phases have large time intervals with a constant voltage value. However, it may be desirable to reduce these time intervals, in which the motor operation is not influenced, without the speed being influenced.

From GB-OS 2,142,194 it is known, in order to change the harmonic content of the supply voltages for a three-phase asynchronous motor and, particularly, in
25 order to reduce the negative effects of lower-order harmonics at low speeds, to apply pulse modulations at the beginning and towards the end of each halfcycle of the rectangular supply voltage and, in addition, to apply voltage chopping in the middle of the pulses of the rectangular voltages. This results not only in an overall reduction of the constant-voltage

intervals in the rectangular supply voltages of the three-phase motor but also in a change of the overall voltage waveforms.

However, when a load is powered by means of a circuit arrangement comprising a power inverter the situation may occur that under given operating conditions a constant voltage of given polarity is applied to a terminal of the load beyond a given period of time. If it is then desired to restrict the supply of this constant voltage of given polarity to said time interval a variation of the voltage value will result the voltage waveform to be applied to the load being changed in an undesirable manner. For example, at a low enough speed of a three-phase motor to be powered a voltage variation will occur which deviates to an uncontrolled extent from that at higher speeds. Particularly if the voltage variation for the high speeds has been dimensioned for optimum operating conditions of the motor, for example in order to minimize the content of undesirable harmonic waves or in order to reduce unwanted transient effects, these optimum operating conditions may be disturbed severely at low speeds.

It is an object of the invention to provide a circuit arrangement for powering a load which under all operating conditions prevents a voltage on a terminal of the load from being sustained at a given voltage value beyond a given period of time, without the operation being impaired.

According to the invention this object is achieved by means of a circuit arrangement for powering a load having a number of n terminals via a power inverter comprising a number of n branches, in which one of the terminals of the load is optionally connectable to a first or a second terminal of a voltage source by each of the branches, as a result of which a voltage vector having a number of n components is applied to the load, which components can each assume two values constituted by the voltage values produced by the voltage source on the terminals of this source, which arrangement comprises a control circuit by means of which the n components of the voltage vector can be set to the two possible values in a given time sequence, so that the voltage vector complies with a given function of time in which all n components assume the same value (referred to as null vector) in regularly recurring time intervals, the next null vector, in the case that at least one of the components of the voltage vector assumes exclusively a first one of the two values for a given period of time, being formed with the second one of the two values.

The circuit arrangement in accordance with the invention can be used universally for polyphase loads of a wide variety of kinds. It is particularly suitable for the power supply of variable-speed polyphase drives. The most important requirement is then





that a null vector recurs at regular time intervals. This means that all components of the voltage vector, i.e. all the voltages appearing on the load terminals, assume the same value. In the time intervals in which this condition occurs the load is thus short-circuited with respect to all its terminals. In that case it is irrelevant via which of the supply source terminals this short-circuit is produced. Consequently, it may be produced via the desired supply source terminal, i.e. via the desired one of the two values of the components of the voltage vector. For all the components of the voltage vector it is thus possible to effectively limit the time interval during which it can exclusively assume one of the two values, without the operation of the load being affected thereby. In particular, it does not give rise to any undesired harmonics or transient effects.

A preferred use of the invention is obtained if at least some of the n components of the voltage vector are temporarily pulse-width modulated as a function of time. At least the individual pulses of this function then form regularly recurring time intervals, in which preferably null vectors occur. A particularly suitable field of use is obtained in the case that not all of the n components of the voltage vector are pulse-width modulated, in which case at option some components may be pulse-width modulated predominantly or continuously and other components may be pulse-width modulated to a small extent or not at all but, as an alternative, all the components in succession may be pulse-width modulated alternately in a given sequence in given periods of time but may be constant in the other periods of time. This results in a very broad field of use for the circuit arrangement in accordance with the invention because it is possible to use a variety of different variants for powering the load in accordance with the invention.

In an advantageous case in which the circuit arrangement in accordance with the invention is used, the first terminal of the voltage source essentially carries a high voltage value as the first one of the two values of the components and the second terminal of the voltage source carries ground potential as the second one of the two values of the components. This selection of the voltage values is particularly suitable for an embodiment of the circuit arrangement in accordance with the invention, which is characterized in that each branch of the power inverter includes two semiconductor switches, of which a first one is disposed between the first terminal of the voltage source and the associated terminal of the load and of which a second one is disposed between the associated terminal of the load and the second terminal of the voltage source, there has been provided a driver circuit for each for each semiconductor switch, and the driver circuits of one branch of the power inverter are powered from a common drive supply voltage source, to which the (first) driver circuit



of the first semiconductor switch is connected via a diode and the (second) driver circuit of the second semiconductor switch is connected directly. This arrangement is of very simple construction and is therefore favorable for use in mass products. The invention then makes it possible to obtain an efficient and reliable drive using very cheap means.

5 Embodiments of the invention, given by way of example, are shown in the drawings, in which

Fig. 1 shows the basic circuit diagram of a three-phase motor powered by means of a direct voltage source,

Fig. 2 shows some signal waveforms relating to Fig. 1,

10 Fig. 3 shows an example of an embodiment, and

Fig. 4 shows in detail a power inverter for use with the invention.

In Fig. 1 the reference numeral 1 refers to a voltage source having a first terminal 2 and second terminal 3. In principle, the voltage source carries a direct voltage of a magnitude U_0 between its terminals 2, 3. The second terminal 3 is connected to ground
15 and is therefore at ground potential 0. The first terminal of the voltage source 1 is consequently at a high voltage value U_0 .

Fig. 1 further shows diagrammatically a power inverter 4 and a motor forming a load 5. The load 5 has a number of $n=3$ terminals 51, 52 and 53, each connected to an associated branch 41, 42 or 43 of the power inverter 4. By each of the branches 41, 42
20 and 43 the associated terminal 51, 52 or 53 of the load 5 can be connected optionally to the first terminal 2 or the second terminal 3 of the voltage source 1. In Fig. 1 the branches 41, 42, 43 of the power inverter 4 are therefore each shown diagrammatically as a switch. Voltages U_1 , U_2 and U_3 are applied to the respective terminals 51, 52 and 53 of the load 5 via the branches 41, 42, 43 of the power inverter 4. These voltages U_1 , U_2 , U_3 represent a
25 voltage vector, which in a generalized form comprises a plurality of components, in general terms n components U_1 , U_2 , U_3 , ..., U_n . These components can each assume two different values, formed by the voltage values U_0 and 0 produced by the voltage source 1 on its terminals 2, 3. The switches in the branches 41, 42, 43 - in general up to $4n$ - can be set in such a manner by a control circuit, not shown in Fig. 1, that given voltage vectors can be
30 applied to the load 5 in a given time sequence, i.e. the n components of the voltage vector can be set to their two possible values 0 and U_0 in this given time sequence. Thus, the voltage vector is a given function of time.

Fig. 2 shows a series of diagram of signal waveforms for powering the load 5 in Fig. 1. These signal waveforms can be processed or generated by means of the



above-mentioned control circuit. An example of such a circuit can be found in the US Patents 4,626,763 and 4,602,201 mentioned in the introductory part, which are herewith incorporated by reference. Therefore, the description of the present embodiment does not include a detailed description of the construction and operation of such a control circuit.

5 The control of the motor forming the load 5 is based on a rectangular signal as shown in Fig. 2a) and having a frequency corresponding to six times the revolution frequency (in the simplest case) of the motor. This first signal S1, which defines the revolution frequency of the motor 5, divides one revolution period T of the motor 5 into six equal time intervals, which start at the rising edges of the first signal S1, which edges
10 correspond to the instants t_0 to t_5 ; the instant t_6 corresponds to the end of a revolution period T. In the diagrams shown in Fig. 2 the letter t indicates the time axis.

Fig. 2b) shows the variation in time of a second signal S2, which is also rectangular and whose frequency is high relative to the frequency of the first signal S1. TS2 is a period of the second signal S2 and ATS2 is a pulse duration within this period TS2. The
15 frequency of the second signal S2 is maintained at a constant value independently of the operating condition of the motor 5, i.e. independently of the frequency of the first signal. However, the pulse duration ATS2 of the second signal S2 can be pulse-width modulated, i.e. can be varied between 0 and TS2, as required. This serves to obtain time variations for the voltage vector U1, U2, U3, which is described in detail in the literature cited in the
20 introductory part. For the sake of simplicity Fig. 2 only refers to a signal waveform with a constant ratio, i.e. duty cycle, between the pulse duration ATS2 and the period TS2.

In a manner known per se a pulse-width modulation circuit forms a signal vector having components P1, P2, P3 (in general up to Pn) from the said two signals S1 and S2, which components are shown as a function of time in Figs. 2c), 2d) and 2e). By means
25 of these signals P1, P2, P3 the branches 41, 42 and 43 of the power inverter 4 in Fig. 1 can be controlled in such a manner that the associated branch 41, 42 or 43 of the power inverter 4 connects the respective terminal 51, 52 or 53 of the load 5 connected to it to the first terminal 2 of the voltage source 1 when a high signal level occurs in one of the signals P1, P2 and P3 and to the second terminal 3 in the case of a low level of the signals P1, P2 and
30 P3. Accordingly, the signal vector P1, P2, P3 can produce across the load 5 a voltage vector U1, U2, U3 corresponding to a three-phase system. In the present example the components P1, P2, P3 of the signal vector pulsate only at intervals in accordance with the shape of the second signal S2 but are constant in the other time intervals. For example, the first component P1 of the signal vector and hence the voltage U1 as the first component of the



voltage vector across the load 5 has a constant value in the first time interval between the instants t_0 and t_1 , pulsates in accordance with S_2 in the time interval between T_1 and t_2 , has a constant high value between t_2 and t_3 , has a constant low value between t_3 and t_4 , pulsates again between t_4 and t_5 , and has again a constant low value between t_5 and t_6 . In

- 5 comparison with a continuously pulsating form this signal waveform has the advantage that the number of switching actions per unit of time is smaller, as a result of which smaller switching losses occur in the power inverter branches 41, 42, 43.

The time intervals in which the signals P_1 , ... and, consequently, the voltages U_1 , ... have constant values, which intervals are long in comparison with the period
10 TS_2 of the second signal S_2 , may be extended undesirably in the case of low revolution frequencies of the motor 5. It may then be desirable to change the value of the relevant component of the signal vector or voltage vector at least briefly within these time intervals. The operational or design reasons for this may be manifold; an example of this will be described hereinafter with reference to Fig. 3 and Fig. 4. This example, but also that of Fig.
15 2, is based on the case that at least one of the components of the voltage vector U_1 , ... assumes the high value U_0 beyond a given period of time within a time interval bounded by the instants t_0 to t_6 . In accordance with the object of the invention said component of the voltage vector U_1 , ... should then at least briefly assume the low value 0 at the latest after expiry of this given period of time, without the change of the voltage vector U_1 , ... caused
20 thereby leading to a change of the voltages between the terminals 51, 52, 53 of the load 5. Fig. 2i) shows the difference of the voltages U_2 and U_3 between the second terminal 52 and the third terminal 53 as an example for one of the voltages between the terminals 51, 52, 53 of the motor 5. It is apparent that an interruption of the signal waveform of P_3 in Fig. 2e) in the time interval between t_0 and t_1 will lead to a change of the voltage waveform of Fig. 2i)
25 in this area. However, such a change is undesirable.

In accordance with the invention, after expiry of the given period of time, which is designated ZSP in Fig. 2, the next null vector of the voltage vector U_1 , ... is inverted. This null vector, i.e. a state of the voltage vector U_1 , ... in which all the components U_1 , ... of the voltage vector assume the same value, will always occur in the
30 time interval between the instants t_0 and t_1 if all the components U_1 , ... of the voltage vector assume the high value. As in this time interval the component U_3 also constantly has the high value U_0 the null vector will appear with the high value U_0 in each pulse of the voltage U_2 . After expiry of the given period of time ZSP this appearance will take place in the time interval Z1. By inverting this null vector all the components U_1 , ... of the voltage



vector are changed over to the low value 0 during the time interval Z1. In Figs. 2f), 2g) and 2h) this is shown for the components $U_1, \dots$ of the voltage vector. As is apparent from Fig. 2i) this change-over does not mean a change for the voltages via the terminals 51, 52 and 53 of the load 5.

5 In the time interval between the instants t_1 and t_2 the components U_2 and U_3 of the voltage vector continuously assume the low value 0, while U_1 is switched between the high value U_0 and the low value 0 in accordance with the second signal S_2 . Thus, in this time interval a null vector is formed via the low voltage value 0 on the second terminal 3 of the voltage source 1 in time intervals which recur regularly with a repetition frequency
10 corresponding to the frequency of the second signal S_2 . Since the spacing between these time intervals in which a null vector occurs is smaller than the given period of time Z_{SP} , the null vector is not inverted between the instants t_1 and t_2 .

The same applies to the time intervals between the instants t_3 and t_4 as well as t_5 and t_6 . Conversely, in the time intervals between the instants t_2 and t_3 as well as
15 t_4 and t_5 a constantly high value occurs in the components P_1 and P_2 and P_2 and P_3 , respectively, for a longer time than the given period of time Z_{SP} . As a consequence, the null vector is inverted again in these time intervals, i.e. in the time intervals marked Z_2 and Z_3 in Fig. 2.

The embodiment shown block-schematically in Fig. 3 is a power supply
20 for a polyphase motor using the circuit arrangement in accordance with the invention. Items already described with reference to Figs. 1 and 2 again bear the same reference symbols. A control circuit 6 is connected to a first signal source 8, which supplies the second signal S_2 to the control circuit 6 via the first input 7. The first signal S_1 is applied to the control circuit 6 via a second input 9. In a control stage 10 this first signal is derived from a
25 nominal-value signal, which is representative of the desired speed of the motor 5 and which is applied to the control stage 10 via a nominal-value input 11, and from an actual-value signal, which is obtained from a rotational-position sensor 12 connected to the motor 5 and which is applied to the control stage 10 via an actual-value input 13. The duty cycle of the signal (7) applied to the control circuit (8) will also be varied depending on the desired motor
30 speed (11) in accordance with the motor characteristic. The control circuit 6 is connected to the power inverter 4 via the power inverter control terminals 21, 22, ..., $2n$. Each of the power inverter control terminals 21, 22, ..., $2n$ is associated with one of the branches 41, 42, ..., $4n$ of the power inverter 4, as is shown very schematically for a three-phase motor 5 in Fig. 1 and in detail for a general example in Fig. 4. The power inverter 4 shown in Fig. 4



includes in each of its branches 41, 42, ..., 4n two load transistors 411, 421; 412, 422 ..., 41n, 42n, respectively, having their main current paths arranged in series between the first terminal 2 and the second terminal 3 of the voltage source 1. The load transistors 411, 412 ... form semiconductor switches for the power inverter 4, of which each time the first is

5 arranged between the first terminal 2 of the voltage source 1 and the associated terminal 51, ... of the load 5, and the second one between the terminal 51, ... of the load 5 and the second terminal 3 of the voltage source 1. Each of the load transistors 411, 421, ... has an associated driver circuit 431, 441; 432, 442, ... 43n, 44n whose output is connected to the control terminal of the associated load transistor 411, 421, ... The respective driver circuits

10 431, 441; 432, 442, ... 43n, 44n of each of the branches 41, 42 ... 4n each have their inputs connected to one another via a power inverter 451, 452, ... 45n dimensioned for high reverse voltages, the second driver circuits 441, 442 ... 44n for the second load transistors 421, 422 ... 42n having their inputs connected to the associated power inverter control terminals 21, 22 ... 2n. The first driver circuits 431, 432 ... 43n each have a first one of their

15 supply voltage terminals 461, 462 ... 46n connected to the associated terminal 51, 52 ... 5n of the load 5, i.e. also to the node between the main current paths of the associated load transistors 411, 421; 412, 422 ... 41n, 42n. Likewise, the second driver circuits 441, 442 ... 44n each have their first supply voltage terminal 471, 472 ... 47n connected to the second terminal 3 of the voltage source 1. Each second supply voltage terminal 491, 492, ... 49n is

20 connected to a first terminal 14 of a common driver supply voltage source 15, whose second terminal 16 is coupled to ground potential 0 together with the voltage source 1. Moreover, a diode 31, 32 ... 3n in each branch 41, 42 ... 4n of the power inverter 4 connects the first terminal 14 of the driver supply voltage source 15 to a second supply voltage terminal 481, 482 ... 48n of the first driver circuit 431, 432 ... 43n associated with the respective branch.

25 The first and the second supply voltage terminal of each of the driver circuits 431, 432 ... 43n are connected to one another via a respective supply capacitor 511, 521; 512, 522 ... 51n, 52n. Thus, in the present embodiment not only the driver circuits 431, 441, ... of a branch 41, ... of the power inverter 4 but all the driver circuits receive their power supply from a common driver supply voltage source 15.

30 In a practical version of the power inverter shown in Fig. 4 the driver circuits 431, 441, ... of each of the branches 41, ... may be combined in a common, preferably integrated, device. All the driver circuits 431 require only one driver supply voltage source 15, which supplies a supply voltage U_v . This simplifies the power supply for the power inverter 4 considerably. In principle, the voltage U_v may be smaller than the



voltage value U_0 . In the intervals in which in a branch 41, ... of the power inverter 4 the first load transistor 411, ... conducts and, consequently, the second load transistor 421, ... is cut off, the associated diode 31, ... is also cut off and the first driver circuit 431, ... is isolated from the driver supply voltage source 15. The first driver circuit 431, ... is then
 5 powered by the connected supply capacitor 511, ... If the first load transistor 411, ... now remains continuously conductive beyond the given period of time ZSP and, as a result, the supply capacitor 511, ... is not recharged during this period of time ZSP, the supply voltage for the first driver circuit 431, ... may decrease below a permissible minimum value. It is then necessary to recharge the associated supply capacitor 511, ... For this purpose, the
 10 second load transistor 421, ... of the relevant branch 41, ... of the power inverter 4 must be turned on and the associated first load transistor 411, ... must be turned off. The invention explained with reference to Fig. 2 guarantees this and also ensures that this switching operation has no effect on the load 5.

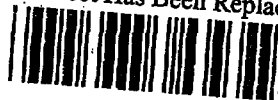
Fig. 4 shows the symbolic equivalent diagram of the second branch 4n of
 15 the power inverter 4 in order to illustrate the relationship with Fig. 1.

Fig. 3 shows an example of an embodiment for a circuit arrangement in accordance with the invention by means of which the signal waveforms shown in Figs. 2f to 2h can be generated and which can be used in conjunction with the power inverter 4 shown in Fig. 4. The control circuit 6 shown in Fig. 3 comprises a pulse-width modulation circuit
 20 17 which, in a manner known from the literature cited in the introductory part, which derives the signal vector $P_1, P_2, \dots, P_n$ shown in Figs. 2c) to 2e) from the signals applied to it via the inputs 7 and 9 of the control circuit 6 and delivers it at signal outputs 171, 172, ..., 17n. Each of the signal outputs 171, ... is connected to a first input 61, 62, ..., 6n of a respective Exclusive-Or gate 71, 72 ... 7n, whose output 81, 82 ... 8n is connected to the power
 25 inverter control terminal 21, 22 ... 2n of the branch 41, 42 ... 4n of the power inverter 4, to which the associated component $P_1, P_2 \dots P_n$ of the signal vector $P_1, \dots, P_n$ is to be applied. The Exclusive-Or gates 71, 72 ... 7n serve as inverters which can be controlled via their second inputs 91, 92 ... 9n. Depending on the signal applied via the second inputs 91, 92 ... 9n the signal vector $P_1, \dots, P_n$ is transferred in inverted or non-inverted form.

30 The signal outputs 171, ... 17n of the pulse-width modulation circuit 17 are also connected to inputs 181, 182 ... 18n of an OR gate 18 and to inputs 191, 192 ... 19n of an AND gate 19. At its output 180 the OR gate 18 produces a signal with information whether at least one of the components $P_1, \dots$ of the signal vector has a high value. The output 180 of the OR gate 18 forms an enable input of a counter 100, to which the second

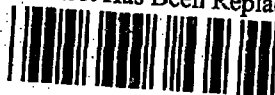
signal S2 from the first input 7 of the control circuit 6 is applied via a clock input 101. The counter 100 counts the pulses of the second signal S2 as long as the enable input (or the output 180 of the OR gate 18) carries a signal indicating that at least one of the components of the signal vector $P_1, \dots, P_n$ has a high value. When a count N is reached, which
5 corresponds to a number of periods TS_2 forming the given period of time ZSP , the counter 100 supplies a signal of logic high level to a further input 20 of the AND gate 19 of the AND gate 19 via a decoder circuit 102. When the next null vector appears, which is formed via the high voltage value U_0 on the first terminal 2 of the voltage source 1, i.e. when all the components $P_1, \dots$ of the signal vector assume a high value, another signal of logic high
10 level appears on the output 190 of the AND gate 19. This is applied to the second inputs 91, ... of the Exclusive-Or gate 71, upon which this gate inverts the applied null vector.

This Sheet Has Been Replaced



CLAIMS:

This Sheet Has Been Replaced



1. A circuit arrangement for powering a load having a number of n terminals via a power inverter comprising a number of n branches, in which one of the terminals of the load is optionally connectable to a first or a second terminal of a voltage source by each of the branches, as a result of which a voltage vector having a number of n components is applied to the load, which components can each assume two values constituted by the voltage values produced by the voltage source on the terminals of this source, which arrangement comprises a control circuit by means of which the n components of the voltage vector can be set to the two possible values in a given time sequence, so that the voltage vector complies with a given function of time in which all n components assume the same value (referred to as null vector) in regularly recurring time intervals, the next null vector, in the case that at least one of the components of the voltage vector assumes exclusively a first one of the two values for a given period of time, being formed with the second one of the two values.
2. A circuit arrangement as claimed in Claim 1, characterized in that at least some of the n components of the voltage vector are temporarily pulse-width modulated as a function of time.
3. A circuit arrangement as claimed in Claim 1 or 2, characterized in that the first terminal of the voltage source essentially carries a high voltage value (U_0) as the first one of the two values of the components and the second terminal of the voltage source carries ground potential (0) as the second one of the two values of the components.
4. A circuit arrangement as claimed in Claim 3, characterized in that each branch of the power inverter includes two semiconductor switches, of which a first one is disposed between the first terminal of the voltage source and the associated terminal of the load and of which a second one is disposed between the associated terminal of the load and the second terminal of the voltage source, there has been provided a driver circuit for each for each semiconductor switch, and the driver circuits of one branch of the power inverter are powered from a common drive supply voltage source, to which the (first) driver circuit of the first semiconductor switch is connected via a diode and the (second) driver circuit of the second semiconductor switch is connected directly.