Method for producing a semiconductor wafer

The invention relates to a method for producing a semiconductor wafer.

In accordance with the prior art, semiconductor wafers are produced in a multiplicity of successive process steps, which can generally be subdivided into the following groups:

a) production of a single crystal composed of semiconductor material (crystal pulling);
b) separation of the semiconductor single crystal into individual wafers ("wafering", "sawing"),
c) mechanical processing of the semiconductor wafers;
d) chemical processing of the semiconductor wafers;
e) chemomechanical processing of the semiconductor wafers;
f) thermal treatment of the semiconductor wafers and/or epitaxial coating of the semiconductor wafers.

In addition there are a multiplicity of secondary steps such as cleaning, measuring and packaging.

A semiconductor single crystal is usually produced by pulling a single crystal from a melt (CZ or "Czochralski" method) or by recrystallizing a rod composed of polycrystalline semiconductor material (FZ or "floating zone" method).

Known separation methods include wire sawing ("multi-wire slicing", MWS) and internal-diameter sawing.

In the case of wire sawing, a multiplicity of semiconductor wafers are sliced from a piece of crystal in one work operation.

The mechanical processing serves for removing sawing undulations, for removing the surface layers that were

damaged in crystalline fashion by the rougher sawing processes or were contaminated by the sawing wire, and primarily for global leveling of the semiconductor wafers. Surface grinding (single-side, double-side) and lapping are known here, and also mechanical edge processing steps.

In the case of single-side grinding, the semiconductor wafer is held on the rear side on a support ("chuck") and leveled on the front side by a cup grinding disk with rotation of support and grinding disk and slow radial advance. Methods and apparatuses for the surface grinding of a semiconductor wafer are known from US-3,905,162 and US-5,400,548 or EP-0955126 for example. In this case, a semiconductor wafer is fixedly held on a wafer holder by one of its surfaces, while its opposite surface is processed by means of a grinding disk, by wafer holder and grinding disk rotating and being pressed against one another. In this case, the semiconductor wafer is fixed on the wafer holder in such a way that its center substantially corresponds to the rotation center of the wafer holder. Moreover, the grinding disk is positioned in such a way that the rotation center of the semiconductor wafer reaches a working region or the edge region formed by teeth of the grinding disk. As a result, the entire surface of the semiconductor wafer can be ground without any movement in the grinding plane.

In the case of simultaneous double-side grinding ("double-disk grinding", DDG), the semiconductor wafer is simultaneously processed on both sides in a manner floating freely between two grinding disks mounted on opposite colinear spindles, and in the process is guided in a manner largely free of constraining forces axially between a water cushion (hydrostatic principle) or air cushion (aerostatic principle) acting on the front and rear sides, and is prevented from floating

away radially loosely by a surrounding thin guide ring or by individual radial spokes.

In the case of lapping, the semiconductor wafers are moved under a specific pressure with supply of a slurry containing abrasive materials between an upper and a lower working disk, which are usually composed of steel and normally provided with channels for better distribution of the lapping agent, whereby semiconductor material is removed.

DE 103 44 602 A1 and DE 10 2006 032 455 A1 disclose methods for the simultaneous grinding at the same time of both sides of a plurality of semiconductor wafers with a movement sequence similar to that of lapping, but characterized by the fact that abrasive is used which is fixedly bonded in working layers ("films", "pads") applied to the working disks. A method of this type is referred to as "fine grinding with lapping kinematics" or "planetary pad grinding" (PPG).

Working layers which are used in the case of PPG and which are adhesively bonded onto the two working disks are described for example in US 6,007,407 A and US 6,599,177 B2. During processing, the semiconductor wafers are inserted into thin guide cages, so-called carriers, which have corresponding openings for receiving semiconductor wafers. The carriers have an outer toothing which engages into a rolling apparatus comprising inner and outer toothed rings and are moved by means of said rolling apparatus in the working gap formed between upper and lower working disks.

The edge of the semiconductor wafer including any existing mechanical markings such as an orientation notch is usually processed as well ("edge rounding", "edge notch grinding"). Conventional grinding steps with profiled grinding disks or belt grinding methods

with continuous or periodic tool advance are used for this purpose.

These edge rounding methods are necessary since the edge in the unprocessed state is particularly fracture-sensitive and the semiconductor wafer can be damaged even by slight pressure and/or temperature loads in the edge region.

The wafer edge that has been ground and treated with an etching medium is usually polished in a later processing step. In this case, the edge of a centrally rotating semiconductor wafer is pressed against a centrally rotating polishing drum with a specific force (contact pressure). US 5,989,105 discloses an edge polishing method of this type wherein the polishing drum is composed of an aluminum alloy and has a polishing pad applied to it. The semiconductor wafer is usually fixed on a flat wafer holder, a so-called chuck. The edge of the semiconductor wafer projects beyond the chuck, such that it is freely accessible for the polishing drum.

The group of chemical processing steps usually comprises wet-chemical cleaning and/or etching steps.

The group of chemomechanical processing steps comprises polishing steps by which, through in part chemical reaction and in part mechanical material removal (abrasion) the surface is smoothed and residual damage of the surface is removed.

While the polishing methods that work on one side ("single-side polishing") generally lead to poorer plane-parallelisms, polishing methods acting on both sides ("double-side polishing") make it possible to produce semiconductor wafers having improved flatness.

After the grinding, cleaning and etching steps, in accordance with the prior art, the surface of the

semiconductor wafers is smoothed by removal polishing. In the case of single-side polishing (SSP), semiconductor wafers are held on the rear side on a support plate by means of cement, by vacuum or by means of adhesion during processing. In the case of double-side polishing (DSP), semiconductor wafers are loosely inserted into a thin toothed disk and polished on the front and rear sides simultaneously in "freely floating" fashion between an upper and a lower polishing plate covered with a polishing pad.

Furthermore, the front sides of the semiconductor wafers are often polished in haze-free fashion, for example by means of a soft polishing pad with the aid of an alkaline polishing sol. This step is often referred to as CMP polishing ("chemomechanical polishing") in the literature. CMP methods are disclosed for example in US 2002-0077039 and in US 2008-0305722.

The prior art likewise discloses the so-called "fixed abrasive polishing" (FAP) technologies, wherein the silicon wafer is polished on a polishing pad which, however, contains an abrasive material bonded in the polishing pad ("fixed-abrasive pad"). A polishing step in which such an FAP polishing pad is used is hereinafter referred to for short as FAP step.

WO 99/55491 A1 describes a two-stage polishing method, comprising a first FAP polishing step and a subsequent second CMP polishing step. In CMP, the polishing pad contains no bonded abrasive material. Here, as in the case of a DSP step, abrasive material is introduced in the form of a slurry between the silicon wafer and the polishing pad. Such a two-stage polishing method is used, in particular, to eliminate scratches left by the FAP step on the polished surface of the substrate.

The German patent application DE 102 007 035 266 A1 describes a method for polishing a substrate composed of silicon material, comprising two polishing steps of the FAP type, which differ in that in one polishing step a polishing agent slurry containing unbonded abrasive material as solid is introduced between the substrate and the polishing pad, while in the second polishing step the polishing agent slurry is replaced by a polishing agent solution that is free of solids.

Semiconductor wafers are often provided with an epitaxial layer, that is to say with a layer grown in monocrystalline fashion and having the same crystal orientation, on which semiconductor components are applied later. Such epitaxially coated semiconductor wafers have certain advantages over semiconductor wafers composed of homogeneous material, for example the prevention of charge reversal in bipolar CMOS circuits followed by the short circuit of the component ("latch-up" problem), lower defect densities (for example reduced number of COPs ("crystal-originated particles") and the absence of an appreciable oxygen content, whereby it is possible to rule out a short-circuit risk owing to oxygen precipitates in component-relevant regions.

What is crucial is how the above-described mechanical and chemomechanical or purely chemical method steps are arranged in a process sequence for producing a semiconductor wafer.

It is known that the polishing steps such as SSP, DSP and CMP, the etching treatments and the epitaxy step lead to a deterioration in the flatness of the semiconductor wafer particularly in the edge region.

Therefore, endeavors have been made in the prior art to minimize the material removal during polishing, in

order also to limit the deterioration in flatness to a minimum.

US 5942445 A proposes slicing (sawing) a semiconductor wafer from the crystal, rounding the edge of the semiconductor wafer, then carrying out a grinding step, which can comprise a double-side grinding and a single-side grinding of front and rear sides of the semiconductor wafer, subjecting the semiconductor wafer to an alkaline wet etch, and finally polishing the semiconductor wafer by means of DSP. The double-side grinding can also be replaced by a lapping step. A plasma etch can also be effected after the wet etch. Finally, the grinding steps and the wet etch can be replaced by a plasma etch.

The semiconductor wafers polished by means of DSP which are obtainable by this method have an unsatisfactory geometry in the edge region owing to the use of wet-chemical treatments and the plasma-assisted chemical etching (PACE). Thus, at best semiconductor wafers having acceptable flatness values are available if an edge exclusion of at least 2 mm is always taken as a basis, cf. ITRS "Roadmap". The nanotopology, in particular, is adversely influenced by etching methods. In order to improve the nanotopology after the etching step, in DSP an increased material removal is necessary, but the latter in turn adversely influences the geometry in the edge region.

In order to be able to provide semiconductor wafers for future technology generations which meet the stringent requirements made of the edge region of a semiconductor wafer, that is to say in order, for example, to make even the outermost edge region of the wafer accessible to the modern lithographic methods (immersion lithography), other approaches are necessary.

The problem area described gave rise to the stated object of the present invention, namely of providing a novel process sequence for producing semiconductor wafers in particular having a diameter of 450 mm.

The object of the invention is achieved by means of a method for producing a semiconductor wafer, comprising in the stated order:

(a) double-side material-removing processing of the semiconductor wafer sliced from a single crystal;

(b) rounding of the edge of the semiconductor wafer;

(c) grinding of front and rear sides of the semiconductor wafer, wherein in each case one side of the semiconductor wafer is fixedly held by means of a wafer holder while the other side is processed by means of a grinding tool;

(d) polishing of at least one side of the semiconductor wafer by means of a polishing pad comprising fixedly bonded abrasives;

(e) treatment of both sides of the semiconductor wafer with an etching medium in conjunction with a material removal of not more than 1 µm per side of the semiconductor wafer;

(f) polishing of a front side of the semiconductor wafer using a polishing pad having fixedly bonded abrasives and simultaneous polishing of a rear side of the semiconductor wafer by means of a polishing pad which contains no abrasives, but in the case of which an abrasive-containing polishing agent is introduced between polishing pad and rear side of the semiconductor wafer;

(g) polishing of the edge of the semiconductor wafer;

(h) polishing of the rear side of the semiconductor wafer by means of a polishing pad comprising fixedly bonded abrasives and simultaneous polishing of the front side of the semiconductor wafer by means of a polishing pad which contains no fixedly bonded abrasives, wherein an abrasive-containing polishing

agent is introduced between polishing pad and front side of the semiconductor wafer.

Firstly, a semiconductor wafer is sliced from a single crystal composed of semiconductor material, grown by means of CZ or FZ. The semiconductor wafer is preferably sliced by means of a wire saw. The slicing of the semiconductor wafer by means of a wire saw is effected in the manner known e.g. from US 4655191, EP 522 542 A1, DE 39 42 671 A1 or EP 433 956 A1.
The grown single crystal composed of semiconductor material is preferably a single crystal composed of silicon. The semiconductor wafer is preferably a monocrystalline silicon wafer.

The essential steps of the method according to the invention and the preferred embodiments thereof are explained below in detail.

Step (a) - Double-side material-removing processing of the semiconductor wafer sliced from a single crystal

In step (a) of the method according to the invention, both sides of the semiconductor wafer are subjected to material-removing processing.

This can be done by means of simultaneous double-side grinding (DDG) or by means of PPG (planetary pad grinding). A lapping step is less preferred in the method according to the invention.

DDG machines according to the prior art, as are described for example in JP2000-280155A and JP2002-307303A have two grinding wheels which lie opposite one another and the rotation axes of which are arranged colinearly. During the grinding operation, a workpiece in wafer form which is positioned between the grinding wheels is processed on both sides simultaneously by the two grinding wheels rotating about their axis, while it

is held in position by a ring-shaped holding and rotation device and at the same time rotated about its own axis. During the grinding operation, the two grinding wheels are advanced in an axial direction until the desired final thickness of the workpiece has been reached.

The holding and rotation device may, for example, comprise friction wheels which engage on the edge of the workpiece. However, it may also be a device which surrounds the workpiece in ring-shaped fashion and engages in a score, groove or notch which is possibly present at the periphery of the workpiece. A device of this type is normally referred to as a "notch finger". In order to process the entire area of the workpiece, the workpiece is guided relative to the grinding wheels in such a way that the abrasive grinding segments of the grinding wheels describe a circular path which runs constantly over the center of the workpiece.

In this case, the workpiece is not generally in a fixed position, but rather is held axially in position by two apparatuses for hydrostatic bearing, referred to as "hydropads", which are fitted on both sides of the workpiece. Apparatuses of this type are described in JP2002-280155A. In accordance with the prior art, those surfaces of the two hydropads which face the workpiece are configured in planar fashion and oriented parallel to one another. Each hydropad comprises a plurality of hydrostatic bearings, between which grooves for discharging the medium used for the hydrostatic bearing (referred to hereinafter as the "hydro-bearing medium") and the grinding coolant are arranged.

In each case one or more measuring sensors are integrated into the hydropads, allowing the distance between the surface of the hydropads and the workpiece surface to be measured during the grinding operation. This distance measurement is usually carried out with

the aid of dynamic pressure tubes as a pneumatic dynamic pressure measurement. The dynamic pressure tubes are designed as simple bores in the edges of the hydrostatic bearings, which form the guide surfaces. To enable the distance between the hydropads and the workpiece to be measured as close as possible to the location of grinding processing, the dynamic pressure tubes are generally arranged close to that edge of the hydropads which is adjacent to the grinding wheels.

PPG is a method for the simultaneous double-side grinding of a plurality of semiconductor wafers, wherein each semiconductor wafer lies in freely movable fashion in a cutout in one of a plurality of carriers that are caused to rotate by means of a rolling apparatus, and is thereby moved on a cycloidal trajectory, wherein the semiconductor wafers are processed in material-removing fashion between two rotating working disks, wherein each working disk comprises a working layer containing bonded abrasive.

The use of a PPG method in step (a) of the method according to the invention is especially preferred.

Preferably, the semiconductor wafer to be processed by PPG already has a rounded edge, but is once again subjected to such edge rounding after the PPG step has been carried out. It has been found that such an edge rounding step divided into two parts affords advantages, especially since the PPG method in the case of semiconductor wafers having rounded edges apparently leads to semiconductor wafers having better geometry and nanotopography.

A hard material having a Mohs hardness of ≥ 6 is preferred as abrasive bonded in the working layers. Appropriate abrasive materials are preferably diamond, silicon carbide (SiC), cerium dioxide (CeO_2), corundum (aluminum oxide, Al_2O_3), zirconium dioxide (ZrO_2), boron

nitride (BN; cubic boron nitride, CBN), furthermore silicon dioxide (SiO_2), boron carbide (B_4C), through to significantly softer materials such as barium carbonate ($BaCO_3$), calcium carbonate ($CaCO_3$) or magnesium carbonate ($MgCO_3$). Diamond, silicon carbide (SiC) and aluminum oxide (Al_2O_3; corundum) are particularly preferred, however.

The average grain size of the abrasive should be less than 9 µm. The preferred size of the abrasive grains bonded in the working layers is on average 0.1 to 9 µm, and particularly preferably 0.1 to 6 µm in the case of diamond as abrasive. The diamonds are preferably bonded individually or as clusters in the bonding matrix of the working layer. In the case of cluster bonding, the grain diameters specified as preferred relate to the primary particle size of the cluster constituents.

Working layers with ceramic bonding are preferably used; a synthetic resin bonding is particularly preferred; in the case of working layers with clusters also a hybrid-bonded system (ceramic bonding within the clusters and synthetic resin bonding between clusters and working layer matrix).

The hardness of the working layer is preferably at least 80 Shore A. Particularly preferably the working layer is constructed in multilayer fashion, the upper and lower layers having different hardnesses, with the result that point elasticity and long-wave compliance of the working layer can be adapted to the method requirements independently of one another.

Prior to the first use of a working layer, the abrasive materials bonded into the working layer are preferably uncovered by removing the topmost layer in order to make them usable for the grinding operation. This initial dressing is carried out for example with the aid of grindstones or blades that are preferably

mounted on specifically modified carriers and lead over the two working disks by means of the rolling apparatus.

The dressing is preferably effected using grindstones containing abrasive grain having a similar grain size to the abrasive in the working layers. These "dressing blocks" may be for example ring-shaped and inserted into an externally toothed driver ring, such that they can be guided along between the upper and lower working layers in a suitable manner by means of the rolling apparatuses of the grinding machine. During trimming, the dressing blocks preferably sweep over the entire area of the working layers and particularly preferably even temporarily or else continuously run somewhat beyond the edge of said layers. Preferably, the abrasive grain is bonded in the dressing block in such a way that the wearing of the dressing blocks still permits an economic dressing operation, but during the dressing process at least one layer of loose dressing block grain is always situated in the working zone between dressing block and working layer surface, with the result that the dressing is predominantly effected by free (unbonded) grain.

This is because it has been shown that the dressing process produces a disturbed layer near the surface in the working layer, the depth of which has approximately the extent of the dressing grain. Therefore, a dressing block with excessively coarse grain impresses on the working layer a structure that is characterized by the grain of the dressing block and not by the properties of the working layer. This is disadvantageous for the desired process of self-dressing the working layer as uniformly as possible in the subsequent grinding operation. An excessively fine dressing block yields too little material removal and leads to an uneconomic dressing operation. Finally, it has been shown that dressing predominantly by means of free dressing grain,

on account of the rolling movement of the dressing grain during the dressing movement, exerts less directed forces on the working layer than dressing by means of predominantly fixed dressing grain and the result is a dressed working layer which, although rougher, is particularly isotropic.

Preferably, a grain that is softer than the abrasive grain used in the working layer is used for dressing or trimming the working layer. The dressing grain is particularly preferably made of corundum (Al_2O_3).

Abrasive material residues that have become blunt through continuous wear of the working layer are preferably removed and new abrasive materials with a high capacity for cutting are continuously uncovered. Continuous operation up to the complete wear of the working layers is thereby possible. This operating condition without intervening subsequent dressing intervention is referred to as "self-dressing working" of the working layers and is particularly preferred. The engaging of the grains exposed at the surface of the working layers into the surface of the semiconductor layers and the material removal effected by the relative movement of working layer and semiconductor wafers are technically referred to as "multigrain grinding with a geometrically indeterminate cutting edge".

It is furthermore preferred for the material removal to be effected by predominantly areal engagement of the working layer. "Areal engagement" should be understood to mean that that part of the area of the working layer which is actually in contact with the semiconductor wafer on average during the grinding machining is significantly larger than the contact area of the grinding coating of a cup grinding disk in the case of processing by means of a conventional cup grinding disk grinding process, for example DDG or SSG.

The carriers are preferably produced from a completely metal-free material, for example a ceramic material. However, carriers having a core made of, for example, steel or stainless steel which are coated with a non-metallic coating are also preferred. Such a coating preferably comprises thermoplastics or thermosetting plastics, ceramic or organic-inorganic hybrid polymers, diamond ("diamond-like carbon", DLC), but as an alternative also a hard chromium plating or nickel-phosphorus coating.

In the case of carriers made of metal or having a metal core, the walls of the cutouts for receiving the semiconductor wafers are preferably lined with a ceramic material. As a result, there is no direct contact between the semiconductor wafer and the metal of the carrier.

Preferably, the cutouts for receiving the semiconductor wafers in the carriers are provided eccentrically with respect to the center of the respective carrier in such a way that the midpoint of the carrier lies outside the area of the semiconductor wafers. A carrier preferably has three to eight cutouts for semiconductor wafers. During a grinding operation, preferably five to nine carriers are simultaneously situated in the grinding machine.

The pressure with which the working layers are pressed against the semiconductor wafers during machining, and the path velocity of the semiconductor wafers over the working layers are preferably chosen during the main load step such that the total removal rate, i.e. the sum of the removal rates on both sides of the semiconductor wafers, amounts to 2 to 60 µm/min. Main load step should be understood to mean the processing phase within which the greatest proportion of the total removal in the entire grinding treatment is brought

about, in which processing phase should in turn be understood to mean a time segment during which all the method parameters remain constant. Generally, the main load step is the processing phase with the highest pressure or the proportionally longest duration or both. In the case of a working layer with abrasive grains made of diamond having an average size of 3 to 15 µm, a removal rate of between 2.5 and 25 µm/min is particularly preferred.

For the pressure which the working disks exert on the semiconductor wafers during the main load step, a range of 0.007 to 0.5 bar is preferred and a range of 0.012 to 0.3 bar is particularly preferred. For this specification, the pressure is related to the total area of the semiconductor wafers situated for processing in the apparatus, and not to the effective contact area between working layer and semiconductor wafers.

Furthermore, it is preferred for the working disks to rotate in an opposite sense with regard to the average circulating speed of the carriers during the main load step of processing. In addition, it is particularly preferred for the pressures, rotational speeds and hence path velocities to assume different values for the various processing phases. Finally, it is also particularly preferred for the working disks to rotate in the same sense in specific low-pressure processing phases ("spark out" phases). Such a spark out phase is expedient, and therefore preferred, particularly right at the end of the entire grinding treatment.

Temperature prevailing in the working gap formed between the working layers is preferably kept constant during processing. For this purpose, the carriers can have openings through which cooling lubricant can be exchanged between lower and upper working disks, such that upper and lower working layers always have the

same temperature. This counteracts an undesired deformation of the working gap formed between the working layers as a result of the deformation of the working layers or working disks on account of thermal expansion under alternating load. Moreover, the cooling of the abrasives bonded in the working layers is improved and becomes more uniform, and the effective service life thereof is thereby increased.

The cooling lubricant used preferably comprises a water-based mixture with viscosity-modifying additives such as, for example, glycols, short- or longer-chain polyethylene glycols, alcohols, sols or gels and similar materials which are known as coolants or lubricants.

However, a particularly preferred cooling lubricant is also pure water without any additive.

The amounts of cooling lubricant that are fed to the working gap via the passage in the upper working disk are preferably within the range of between 0.2 and 50 l/min and particularly preferably between 0.5 and 20 l/min.

The preferred initial thickness prior to processing by step a) of the method according to the invention is 500 to 1000 µm. For silicon wafers having a diameter of 300 mm, an initial thickness of 775 to 950 µm is particularly preferred.

The final thickness of the semiconductor wafers after processing according to step a) of the method according to the invention is preferably 500 to 950 µm, and particularly preferably 775 to 870 µm.

The total removal, i.e. the sum of the individual removals from both sides of the semiconductor wafer,

preferably amounts to 7.5 to 120 µm, and particularly preferably 15 to 90 µm.

It is preferred to determine the form of the working gap formed between the working layers during grinding and to alter the form of the working surface of at least one working disk mechanically or thermally depending on the measured geometry of the working gap in such a way that the working gap has a predefined form.

Preferably, the semiconductor wafers temporarily leave the working gap, delimited by the working layers, with a part of their surface during processing, the maximum of the excursion in the radial direction before more than 0% and at most 20% of the diameter of the semiconductor wafer, the excursion being defined as the length - measured relative to the working disks in the radial direction - by which a semiconductor wafer projects beyond the inner or outer edge of the working gap at a specific point in time during grinding.

Step (b) - Rounding of the edge of the semiconductor wafer:

In step (b) the semiconductor wafer is provided with a rounded edge.

For this purpose, the semiconductor wafer is fixed on a rotating table and delivered by its edge against the likewise rotating working surface of a processing tool. The processing tools used in this case can be embodied as disks which are secured to a spindle and have circumferential surfaces serving as working surfaces for processing the edge of the semiconductor wafer. The material-removing grain can be fixedly anchored in the working surfaces of the processing tools. The grain used normally has a coarse granulation. The average

grain size is in this case preferably greater than or equal to 10 µm.

These grinding processing tools are suitable for providing the semiconductor wafer with a rounded edge. After edge rounding, however, a certain minimum roughness usually remains on the edge surface.

In a later processing step, the wafer edge that has been ground and treated with an etching medium is therefore polished in step (g).

For the case where PPG is used in step (a) of the method, it is preferred to carry out two edge grinding steps, the first edge rounding being effected prior to the PPG step.

Step (c) Grinding of front and rear sides of the semiconductor wafer

Both sides of the semiconductor wafer are ground in step c) of the method.

Front and rear sides are preferably ground sequentially.

For this purpose, the semiconductor wafer held on a wafer holder and a grinding disk lying opposite are rotated independently of one another, the grinding disk being arranged in a manner laterally offset relative to the semiconductor wafer and in this case being positioned in such a way that an axial center of the semiconductor wafer reaches a working region of the grinding disk, the grinding disk being moved at an advancing speed in the direction of the semiconductor wafer, whereby grinding disk and semiconductor wafer are delivered to one another, while semiconductor wafer and grinding disk rotate about parallel axes, such that a surface of the semiconductor wafer is ground, the

grinding disk being led back at a returning speed after a specific material removal has been attained.

It is preferred for grinding disk and semiconductor wafer to be delivered by a distance of 0.03-0.5 µm during a revolution of the semiconductor wafer. The choice of delivery during a revolution of the semiconductor wafer of 0.03-0.1 µm is especially preferred.

Preferably, a grinding disk having a grain size of greater than or equal to #2000 is used, especially preferably #2000 - #8000.

The grain size is usually specified in # ("mesh") in accordance with Japanese Industrial Standard JIS R 6001:1998.

An average particle size can be calculated from the mesh figures:

If grinding disks having fine granulation are used, the term fine grinding is often also employed. Such fine grinding disks have e.g. a granulation of from #1000 up to #4000, e.g. those commercially available from Disco Corporation.

It emerges during the conversion into particle sizes that, by way of example, #1200 corresponds to an average particle size of 9.5 µm, #5000 corresponds to an average particle size of 2.5 µm and #8000 corresponds to an average particle size of 1.2 µm.

The average particle sizes during fine grinding are therefore approximately greater than or equal to 1 µm and less than or equal to 10 µm.

A sequence of two serial grinding steps is particularly preferred, wherein the first step is carried out using

grinding disks having a granulation of less than or equal to #2000 in order to obtain the highest possible removal rates and shortest possible process times (coarse grinding) and the second, subsequent step is carried out using grinding disks having a granulation of greater than #2000 and less than or equal to #8000 in order to obtain particularly smoothly ground wafers with minimal damage of approximately 1 µm (fine grinding).

A preferred total removal in the fine grinding step is 25 µm, given symmetrical removal of approximately 12.5 µm per side.

The rotational speed of the grinding disk is preferably 1000-5000 min^{-1}.

The rotational speed of the semiconductor wafer is preferably 50-300 min^{-1}, especially preferably 200-300 min^{-1}.

The advancing speed is preferably 10-20 µm/min.

Step (d) - FAP polishing of at least one side of the semiconductor wafer

In step (d) at least one side of the semiconductor wafer is polished by means of a polishing pad containing abrasives.

Preferably, only the front side of the semiconductor wafer is polished in step (d).

Preferably, only the rear side of the semiconductor wafer is polished in step (d).

Preferably, both front and rear sides of the semiconductor wafer are polished in step (d).

During the polishing step, a polishing agent solution that is free of solids is preferably introduced between that side of the semiconductor wafer which is to be polished and the polishing pad.

The polishing agent solution is, in the simplest case, water, preferably deionized water (DIW) having the purity customary for use in the semiconductor industry.

However, the polishing agent solution can also contain compounds such as sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH) or any desired mixtures thereof. The use of potassium carbonate is especially preferred. In this case, the pH value of the polishing agent solution preferably lies in a range of 10 to 12 and the proportion of the stated compounds in the polishing agent solution is preferably 0.01 to 10% by weight, particularly preferably from 0.01 to 0.2% by weight.

The polishing agent solution can furthermore contain one or more further additives, for example surface-active additives such as wetting agents and surfactants, stabilizers acting as protective colloids, preservatives, biocides, alcohols and complexing agents.

A polishing pad is used which contains an abrasive material bonded in the polishing pad (FAP or FA pad).

Suitable abrasive materials comprise for example particles of oxides of the elements cerium, aluminum, silicon, zirconium and particles of hard materials such as silicon carbide, boron nitride and diamond.

Particularly suitable polishing pads have a surface topography characterized by replicated microstructures.

Said microstructures ("posts") have for example the form of columns having a cylindrical or polygonal cross section or the form of pyramids or truncated pyramids.

More detailed descriptions of such polishing pads are contained for example in WO 92/13680 A1 and US 2005/227590 A1.

The use of a polishing pad having cerium oxide abrasives fixedly bonded therein, as described e.g. in US 6602117 B1 is especially preferred.

The grain sizes of the FAP polishing pads used (size of the fixedly bonded abrasives / particles) are preferably greater than or equal to 0.1 µm and less than or equal to 1.0 µm.

A particle size of 0.1-0.6 µm is particularly preferred.

A particle size of 0.1-0.25 µm is especially preferred.

Removals of greater than or equal to 1 µm per side are preferably employed for the FA polishing, where in this regard the range of 1 - 3 µm is particularly preferred and a range of 1.5 - 2 µm is especially preferably employed.

The wafers processed by means of the FA polishing have preferably previously been processed on both sides by means of grinding disks with a granulation of #2000-#8000 (fine grinding).

Step (e) - Etching or cleaning of a semiconductor wafer

In step (e) of the method according to the invention, both sides of the semiconductor wafer are treated with an etching medium in conjunction with a material

removal of not more than 1 µm per side of the semiconductor wafer.

The minimum material removal per side of the semiconductor wafer is preferably 1 monolayer, that is to say approximately 0.1 nm.

The semiconductor wafer is preferably subjected to a wet-chemical treatment with an acidic medium.

Suitable acidic media include aqueous solutions of hydrofluoric acid, nitric acid or acetic acid.

It is especially preferred for the semiconductor wafer to be treated with a gaseous medium containing hydrogen fluoride and at least one oxidizing agent that oxidizes the surface of the semiconductor wafer. In this case, it is particularly advantageous if the gaseous medium flows against the surfaces of the semiconductor wafer at a relative speed in the range of 40 mm/s to 300 m/s.

The gaseous medium therefore contains hydrogen fluoride and at least one oxidizing agent. The oxidizing agent must be able to oxidize the semiconductor material, e.g. silicon.

When a silicon surface is oxidized, by way of example, a silicon oxide, preferably silicon dioxide arises. This in turn is chemically attacked by hydrogen fluoride, giving rise to hexafluorosilicic acid (H_2SiF_6), silicon tetrafluoride (SiF_4) and water as reaction products, which are discharged by the stream of the gaseous medium. The gaseous medium can furthermore contain further constituents, for example inert carrier gases such as nitrogen or argon, in order to influence the flow conditions and removal rates.

It is preferred to use at least one oxidizing agent selected from the group consisting of nitrogen dioxide,

ozone and chlorine. If pure chlorine is used, it is necessary to add water vapor in order to oxidize the silicon surface. If a mixture of nitrogen dioxide and chlorine and ozone and chlorine is used, the addition of chlorine serves to use the water which is released in the reaction of hydrogen fluoride with silicon dioxide to further oxidize the silicon surface, and thereby to prevent condensation of the water released in the reaction even at low flow velocities and temperatures. It is particularly preferred to use ozone, owing to its high oxidation potential, the fact that the reaction products do not present any problems, and the ease of providing it by means of ozone generators that are in widespread use in the semiconductor industry.

In order to produce the gaseous medium, the constituents can be mixed in the desired quantitative ratio. The ratio of hydrogen fluoride to oxidizing agent is typically chosen in the range of 1:1 to 4:1. The gaseous medium can be supplied either by the individual components being passed directly into the process chamber or a mixer connected upstream thereof, or by the gaseous oxidizing agent being passed through a liquid aqueous solution of hydrogen fluoride having a suitable concentration. This can take place, for example, in a so-called washing bottle or a comparable apparatus. As the gaseous oxidizing agent passes through the aqueous solution, it is enriched with water and hydrogen fluoride, such that the required gaseous medium arises.

With the same method parameters and a constant ratio of hydrogen fluoride to oxidizing agent, an increase in the temperature and an increase in the concentrations exhibit a reaction-accelerating effect.

The etching in the gas phase serves to reduce the roughness of the semiconductor wafer, whereby the

required polishing removal can be reduced, and in addition to remove impurities and reduce surface defects in the crystal structure.

The cleaning and etching methods described are preferably effected as single-wafer treatment.

Specifically for a semiconductor wafer having a diameter of 450 mm that is particularly preferred in the context of the method according to the invention, the SSEC 3400 ML from Solid State Equipment Corp./USA, which is designed for substrates up to a size of 500 mm × 500 mm, is suitable for this purpose.

Step (g) - Polishing of the edge of the semiconductor wafer

The edge of the semiconductor wafer is polished in step (g).

Commercially available automatic edge-polishing units are suitable for carrying out step (g) of the method according to the invention.

US 5,989,105 discloses such an apparatus for edge polishing, wherein the polishing drum is composed of an aluminum alloy and has a polishing pad applied to it.

The semiconductor wafer is usually fixed on a flat wafer holder, a so-called chuck. The edge of the semiconductor wafer projects beyond the chuck, such that it is freely accessible for the polishing drum. A centrally rotating polishing drum, to which the polishing pad is applied and which is inclined by a specific angle with respect to the chuck, and the chuck with the semiconductor wafer are delivered to one another and pressed onto one another with a specific contact pressure while the polishing agent is continuously supplied.

During the edge polishing, the chuck with the semiconductor wafer held thereon is rotated centrally.

Preferably, one revolution of the chuck lasts 20-300 s, particularly preferably 50-150 s (revolution time).

A polishing drum, which is covered with the polishing pad and is preferably rotated centrally at a rotational speed of 300-1500 min^{-1}, particularly preferably 500-1000 min^{-1}, and the chuck are delivered to one another, with the polishing drum being set obliquely at a setting angle with respect to the semiconductor wafer and the semiconductor wafer being fixed on the chuck in such a way that it projects slightly beyond the latter and is therefore accessible for the polishing drum.

The setting angle is preferably 30-50°.

Semiconductor wafer and polishing drum are pressed onto one another with a specific contact pressure and with a polishing agent being supplied continuously, preferably with a polishing agent flow rate of 0.1-1 liter/min, particularly preferably 0.15-0.40 liter/min, wherein the contact pressure can be set by means of weights attached to rolls and is preferably 1-5 kg, particularly preferably 2-4 kg.

Polishing drum and semiconductor wafer are preferably moved away from one another after 2-20, particularly preferably after 2-8, revolutions of the semiconductor wafer or of the chuck holding the semiconductor wafer.

In these customary edge polishing methods, the local geometry in the edge region of the semiconductor wafer is usually adversely influenced. This is associated with the fact that with the relatively "soft edge polishing pads" used in this case (relatively soft polishing pads to which silica sol is applied are

usually used), not only the edge itself but also an outer part on the front and/or rear of the semiconductor wafer is polished as well, which can be explained by the hard edge "dipping" into the polishing pad to which polishing agent slurry is applied. This has the effect that removal is indeed effected not only in the region of the actual edge but also in the adjoining region on the front and/or rear side.

Therefore, the edge polishing of the semiconductor wafer in the method according to the invention is preferably effected by fixing the semiconductor wafer on a centrally rotating chuck, delivering the semiconductor wafer and a centrally rotating polishing drum, to which a polishing pad containing fixedly bonded abrasives (FAP polishing pad) is applied and which is inclined with respect to the chuck, and pressing semiconductor wafer and polishing drum onto one another with the continuous supply of a polishing agent solution containing no solids.

This makes it possible to influence the wafer edge in a targeted manner without impairing the adjoining region of front and/or rear side of the semiconductor wafer, and thus for example to set the desired geometry and surface properties only on the wafer edge.

The FAP pad used is significantly harder and much less compressible than the polishing pads used as standard and affords the advantage, moreover, of producing the removal without alkaline loaded silica sol - e.g. just by using an alkaline solution - , which additionally avoids polishing agent entrainment onto the front side of the wafer and thus the additional adverse influencing of the wafer surface - in the form of e.g. increased defect rates such as e.g. LLS (localized light scatterers) on account of incipient etching.

A short soft polishing step using softly removing silica sol can additionally follow on the same FAP polishing pad, in order to realize a reduction of the edge roughness and edge defect rates.

The two polishing steps can then be coordinated with one another such that a targeted positive influencing of the wafer edge geometry and surface can be performed without adverse influencing of the wafer partial sites on the wafer front side and wafer rear side.

In principle, therefore, the semiconductor wafer is preferably polished by means of a polishing drum, adhesively bonded on the surface of which is a hard and not very compressible polishing pad comprising fixedly bonded abrasives, with an alkaline solution being supplied.

Preferably, a smoothing step is subsequently effected in a second step on the same polishing pad while a silica sol is supplied, such as e.g. *Glanzox 3900** with approximately 1% by weight of SiO_2.

**Glanzox 3900* is the product name for a polishing agent slurry offered as a concentrate by Fujimi Incorporated, Japan. The base solution of this concentrate has a pH of 10.5 and contains approximately 9% by weight of colloidal SiO_2 having an average particle size of 30 to 40 nm.

It has been found that the impairment of the local geometry in the edge region of the semiconductor wafer as observed in the prior art is entirely avoided by such edge polishing using an FAP pad.

A further advantage is that polishing agent entrainments in the removing step of the edge polishing and thus the occurrence of surface defects on account

of uncontrolled incipient etching on the wafer surface are avoided.

The polishing agent solution used during the edge polishing is, in the simplest case, water, preferably deionized water (DIW) having the purity customary for use in the semiconductor industry.

However, the polishing agent solution can also contain compounds such as sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethyl ammonium hydroxide (TMAH) or any desired mixtures thereof.

The use of potassium carbonate is especially preferred.

The pH value of the polishing agent solution preferably lies in a range of 10 to 12 and the proportion of the stated compounds in the polishing agent solution is preferably 0.01 to 10% by weight, particularly preferably from 0.01 to 0.2% by weight.

The polishing agent solution can furthermore contain one or more further additives, for example surface-active additives such as wetting agents and surfactants, stabilizers acting as protective colloids, preservatives, biocides, alcohols and complexing agents.

A polishing agent containing abrasives is used in the preferred second step of the edge polishing.

The proportion of the abrasive material in the polishing agent slurry is preferably 0.25 to 20% by weight, particularly preferably 0.25 to 1% by weight.

The size distribution of the abrasive material particles is preferably markedly monomodal.

The average particle size is 5 to 300 nm, particularly preferably 5 to 50 nm.

The abrasive material comprises a material that mechanically removes the substrate material, preferably one or more of the oxides of the elements aluminum, cerium or silicon.

A polishing agent slurry containing colloidally dispersed silica is particularly preferred.

In the optional second step of the edge polishing, in contrast to the first step, preferably no additives such as sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethyl ammonium hydroxide (TMAH) are added.

However, the polishing agent slurry can contain one or more further additives, for example surface-active additives such as wetting agents and surfactants, stabilizers acting as protective colloids, preservatives, biocides, alcohols and complexing agents.

Preferably, therefore, a polishing pad containing an abrasive material bonded in the polishing pad (FAP pad or FA pad) is used in step (g) of the method according to the invention.

Suitable abrasive materials comprise for example particles of oxides of the elements cerium, aluminum, silicon, zirconium and particles of hard materials such as silicon carbide, boron nitride and diamond.

Particularly suitable polishing pads have a surface topography characterized by replicated microstructures. Said microstructures ("posts") have for example the

form of columns having a cylindrical or polygonal cross section or the form of pyramids or truncated pyramids.

More detailed descriptions of such polishing pads are contained for example in WO 92/13680 A1 and US 2005/227590 A1.

The use of cerium oxide particles bonded in the polishing pad is particularly preferred, cf. also US6602117B1.

The average particle size of the FAP polishing pad is preferably 0.1-1.0 µm, particularly preferably 0.1-0.25 µm.

A polishing pad having a multilayered construction comprising a layer containing abrasives, a layer composed of a stiff plastic and also a compliant, non-woven layer, wherein the layers are bonded to one another by means of pressure-sensitive adhesive layers, is particularly suitable for carrying out the method.

The layer composed of a stiff plastic preferably comprises polycarbonate.

The polishing pad can contain an additional layer composed of polyurethane foam.

One of the layers of the polishing pad is compliant in this case.

The compliant layer is preferably a non-woven layer.

The compliant layer preferably comprises polyester fibers. A layer composed of polyester fibers impregnated with polyurethane is particularly suitable ("non-woven").

By means of the compliant layer, the pad height can be adapted and follow continuous transitions.

The compliant layer preferably corresponds to the bottommost layer of the polishing pad. Situated above that there is preferably a foam layer composed of polyurethane, for example, which is fixed on the compliant layer by means of an adhesive layer. Situated above the PU foam is a layer composed of a harder, stiff material, preferably composed of a hard plastic, for which polycarbonate, for example, is suitable. Situated above this stiff layer is the layer having the microreplicated structures, that is to say the actual fixed abrasive layer.

However, the compliant layer can also be situated between the foam layer and the stiff layer or directly below the fixed abrasive layer.

The various layers are fixed to one another preferably by means of pressure-sensitive adhesive layers (PSA).

The inventor has recognized that a polishing pad without the PU foam layer that is always present in the prior art of FAP polishing pads leads to good results.

In this case, the polishing pad comprises a layer having the microreplicated structures, a compliant layer and a layer composed of a stiff plastic such as polycarbonate, wherein the compliant layer can be either the middle or the bottommost layer of the polishing pad.

The grain sizes of the FAP polishing pads used are preferably greater than or equal to 0.1 µm and less than or equal to 1.0 µm, particularly preferably 0.1-0.25 µm.

Steps (f) and (h) - Double-side polishing by means of FAP and CMP

Furthermore, there is carried out in step (f) polishing of a front side of the semiconductor wafer using a polishing pad having fixedly bonded abrasives and simultaneous polishing of a rear side of the semiconductor wafer by means of a polishing pad which contains no abrasives, but in the case of which an abrasive-containing polishing agent is introduced between polishing pad and rear side of the semiconductor wafer.

Edge polishing as described above is effected in step (g).

Afterward, there is carried out in step (h) polishing of the rear side of the semiconductor wafer by means of a polishing pad comprising fixedly bonded abrasives and simultaneous polishing of the front side of the semiconductor wafer by means of a polishing pad which contains no fixedly bonded abrasives, wherein an abrasive-containing polishing agent is introduced between polishing pad and front side of the semiconductor wafer.

The invention therefore provides a combined simultaneous double-side polishing process in steps (f) and (h) by virtue of the fact that FAP polishing and CMP polishing take place simultaneously first on the front side/rear side and then on the rear side/front side. The conventional DSP step and the subsequent separate CMP step are dispensed with.

Steps (f) and (h) can be carried out on existing apparatuses for the double-side polishing of semiconductor wafers, e.g. on a commercially available double-side polishing machine of the AC2000 type from Peter Wolters, Rendsburg (Germany).

This polishing machine is equipped with pin interlocking of the outer and inner rings in order to drive the carriers. The apparatus can be designed for one or more carriers. Owing to the higher throughout, an apparatus for a plurality of carriers is preferred, such as is described for example in DE-100 07 390 A1 and in which the carriers move on a planetary path around the center of the apparatus. The apparatus includes a lower and an upper polishing plate, which are freely rotatable horizontally and are covered with a polishing pad. During the polishing, the semiconductor wafers are situated in the cutouts in the carriers and between the two polishing plates, which rotate and exert a specific polishing pressure on them while a polishing agent is continuously supplied. In this case, the carriers are also set in motion, preferably by means of rotating pin rings which engage in teeth on the circumference of the carriers.

A typical carrier comprises cutouts for receiving three semiconductor wafers. Situated on the circumference of the cutouts are inlays which are intended to protect the fracture-sensitive edges of the semiconductor wafers, in particular including against metals being released from the carrier body. The carrier body can comprise for example metal, ceramic, plastic, fiber-reinforced plastic, or metal coated with plastic or with a diamond-like carbon layer (DLC layer). Steels are preferred, however, stainless chromium steel being particularly preferred. The cutouts are preferably designed for receiving an odd number of semiconductor wafers having a diameter of at least 200 mm, preferably 300 mm, especially preferably 450 mm, and thicknesses of 500 to 1000 µm.

The polishing agent used during the polishing by means of a polishing pad containing no fixedly bonded

abrasives comprises abrasives. A polishing agent slurry is involved.

The size distribution of the abrasive material particles is preferably markedly monomodal.

The average particle size is 5 to 300 nm, particularly preferably 5 to 50 nm.

The abrasive material comprises a material that mechanically removes the substrate material, preferably one or more of the oxides of the elements aluminum, cerium or silicon.

The proportion of the abrasive material in the polishing agent slurry is preferably 0.25 to 20% by weight, particularly preferably 0.25 to 1% by weight.

The use of colloidally dispersed silica as polishing agent slurry is particularly preferred.

The aqueous polishing agents Levasil® 200 from Bayer AG and Glanzox 3900® from Fujimi are used, by way of example.

The polishing agent preferably contains additives such as sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethyl ammonium hydroxide (TMAH).

However, the polishing agent slurry can contain one or more further additives, for example surface-active additives such as wetting agents and surfactants, stabilizers acting as protective colloids, preservatives, biocides, alcohols and complexing agents.

A polishing pad containing an abrasive material bonded in the polishing pad (FAP or FA pad) is also used in the method according to the invention in accordance with steps (f) and (h).

Suitable abrasive materials comprise for example particles of oxides of the elements cerium, aluminum, silicon, zirconium and particles of hard materials such as silicon carbide, boron nitride and diamond.

Particularly suitable polishing pads have a surface topography characterized by replicated microstructures. Said microstructures ("posts") have for example the form of columns having a cylindrical or polygonal cross section or the form of pyramids or truncated pyramids.

More detailed descriptions of such polishing pads are contained for example in WO 92/13680 A1 and US 2005/227590 A1.

The use of a polishing pad having cerium oxide abrasives fixedly bonded therein, as described e.g. in US 6602117 B1 is especially preferred.

The grain sizes of the FAP polishing pads used (size of the fixedly bonded abrasives / particles) are preferably greater than or equal to 0.1 µm and less than or equal to 1.0 µm.

A particle size of 0.1-0.6 µm is particularly preferred.

A particle size of 0.1-0.25 µm is especially preferred.

One polishing plate is equipped with such an FAP pad.

The second polishing plate has a conventional CMP polishing pad applied to it.

The CMP polishing pads used are polishing pads having a porous matrix.

The polishing pad preferably comprises a thermoplastic or heat-curable polymer. A multiplicity of substances may be envisaged for the material, for example polyurethanes, polycarbonate, polyamide, polyacrylate, polyester, etc.

The polishing pad preferably comprises solid, microporous polyurethane.

It is also preferred to use polishing pads composed of foamed plates or felt or fiber substrates, which are impregnated with polymers.

Coated/impregnated polishing pads can also be configured such that there are a different pore distribution and different pore sizes in the substrate than in the coating.

The polishing pads can be substantially flat or else perforated.

In order to control the porosity of the polishing pad, fillers can be introduced into the polishing pad.

Commercially available polishing pads are, for example, the SPM 3100 from Rodel Inc. or the pads of the DCP series and the pads of the IC1000™, Polytex™ or SUBA™ brands from Rohm & Hass.

As mentioned above, when carrying out polishing in accordance with steps (f) and (h) of the method according to the invention on a double-side polishing machine, as is the case for example with the AC 2000 type from Peter Wolters / Rendsburg, the single-side haze-free polishing (CMP) which is obligatory in the prior art can be obviated since both the polishing

which determines the geometry and that which determines the surface quality are carried out fully on one type of machine.

In the prior art, by contrast, the stock removal and haze-free polishing (DSP and CMP) were carried out separately from one another and on different polishing machines. Only the front side of the semiconductor wafer was polished by means of CMP in the prior art.

In order to achieve an optimal wafer geometry, here primarily the edge geometry (edge roll-off elimination), simultaneous double-side polishing with planetary kinematics and a combined use of fixed-abrasive and CMP polishing pads affords advantages since the fixed-abrasive polishing process makes it possible to dispense with a component containing silica sol, on account of the hard pad, which can optionally be configured with an overhang, in order to obtain the necessary polishing removal, and additionally enables the edge region of the semiconductor wafer to be influenced in a targeted manner.

In addition, the CMP polishing is already integrated in the context of simultaneous double-side polishing by one of the polishing plates being equipped with a CMP polishing pad, on which the CMP step takes place.

The double-side polishing according to the invention takes place in two polishing substeps (f) and (h), between which the semiconductor wafer is subjected to edge polishing in accordance with step (g).

Two-stage edge polishing is preferably effected here, wherein a first edge polishing is carried out between the two substeps of the double-side polishing (f) and (h) and the second edge polishing is carried out after the complete double-side polishing has ended, that is to say after step (h), which makes it possible to more

finely tune the edge polishing by means of this division into two steps and thus to influence the edge geometry of the semiconductor wafer as little as possible.

Preferably, both steps of the edge polishing are effected by means of polishing pads having abrasives fixedly bonded therein.

Preferably, the second edge polishing is effected with supply of an abrasive-containing polishing agent slurry, like the optional soft polishing step described under (g).

In this case, the proportion of the abrasive materials in the polishing agent slurry is preferably 0.25 to 20% by weight.

The abrasive materials in the polishing agent slurry are preferably selected from one or more of the group consisting of oxides of the elements aluminum, cerium or silicon.

The polishing agent slurry is preferably colloidally dispersed silica.

The pH value of the polishing agent slurry is preferably 9 to 11.5.

The pH value of the polishing agent slurry is preferably set by adding additives selected from the group consisting of sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethyl ammonium hydroxide (TMAH) or any desired mixtures of these compounds.

In order to achieve a specifically desired defined rear side roughness of the polished wafer rear side, it may

be advantageous to perform additional single-side FAP polishing of the rear side:

This is preferably carried out in three steps in each case using a polishing pad which contains an abrasive material bonded in the polishing pad and which is pressed onto the rear side of the semiconductor wafer with a polishing pressure, wherein in the first step a polishing agent free of solids, whereas in the second and third steps a polishing agent containing abrasive materials, is introduced between polishing pad and rear side of the semiconductor wafer, wherein a polishing pressure in the first and second steps of 8-15 psi is reduced to 0.5-5 psi in the third step.

On the planar surfaces of its rear side, the semiconductor wafer preferably has an average surface roughness R_a in a wide range of from 0.3 to 4.5 nm, relative to the spatial wavelengths of less than or equal to 250 µm.

Suitable for determining the surface roughness is, by way of example, a Chapman Surface Profiler MP 2000 with a 250 µm filter (spatial wavelengths greater than 250 µm = waviness data, cf. Chapman Technical Note-TG-1, Rev-01-09).

If a high rear side roughness in the abovementioned range is desired, FAP pads have grain sizes of 0.5-1.0 µm are preferably used.

If a low rear side roughness is desired, FAP pads having grain sizes of 0.1-0.25 µm are preferably used.

The polishing agent solution in the first step of polishing the rear side of the silicon wafer in the method according to the invention is, in the simplest case, water, preferably deionized water (DIW) having

the purity customary for use in the semiconductor industry.

However, the polishing agent solution can also contain compounds such as sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethyl ammonium hydroxide (TMAH) or any desired mixtures thereof.

The use of potassium carbonate is especially preferred.

A polishing agent containing abrasives is used in the second step of polishing the rear side of the semiconductor wafer.

The abrasive material comprises a material that mechanically removes the substrate material, preferably composed of one or more of the oxides of the elements aluminum, cerium or silicon.

A polishing agent slurry containing colloidally dispersed silica is particularly preferred.

A polishing agent containing abrasives as used in the second step is likewise used in the third step of polishing the rear side of the semiconductor wafer. The polishing pressure is reduced by comparison with the first and second steps from 8-15 psi to 0.5-5 psi.

Conventional polishing machines such as e.g. the polishing machine "nHance 6EG" from Strasbaugh Inc. are suitable for carrying out these polishing processes.

The polishing machine from Strasbaugh Inc. has one polishing plate with one polishing pad and one polishing head, which processes a semiconductor wafer fully automatically. The polishing head is mounted cardanically and comprises a fixed baseplate coated

with a "backing pad", and a movable guide ring. Through holes in the baseplate, air cushions can be established in two concentric pressure zones, an inner and an outer zone, the semiconductor wafer floating on said air cushions during polishing. Pressure can be applied to the movable guide ring by means of compressed air bellows in order thus to pretension the polishing pad upon contact with the semiconductor wafer and to keep it plane.

Particularly preferred embodiments

Particularly preferred embodiments A-F of the method according to the invention are presented below. The abbreviations PPG, DDG, FAP and CMP used have been explained above.

A
Slicing a wafer from the single crystal - edge rounding - PPG - edge rounding - double-side fine grinding > double-side FAP - gas phase etching - FAP of the rear side and simultaneously CMP of the rear side > edge polishing - FAP rear side and simultaneously CMP front side - edge polishing

B
Slicing a wafer from the single crystal - edge rounding - PPG - edge rounding - double-side fine grinding > FAP of the rear side - gas phase etching - FAP of the rear side and simultaneously CMP of the rear side > edge polishing - FAP rear side and simultaneously CMP front side - edge polishing

C
Slicing a wafer from the single crystal - edge rounding - PPG - edge rounding - double-side fine grinding > FAP of the front side - gas phase etching - FAP of the rear side and simultaneously CMP of the rear side > edge

polishing - FAP rear side and simultaneously CMP front side - edge polishing

D

Slicing a wafer from the single crystal - DDG - edge rounding - double-side fine grinding > double-side FAP - gas phase etching - FAP of the rear side and simultaneously CMP of the rear side > edge polishing - FAP rear side and simultaneously CMP front side - edge polishing

E

Slicing a wafer from the single crystal - DDG - edge rounding - double-side fine grinding > FAP of the rear side - gas phase etching - FAP of the rear side and simultaneously CMP of the rear side > edge polishing - FAP rear side and simultaneously CMP front side - edge polishing

F

Slicing a wafer from the single crystal - DDG - edge rounding - double-side fine grinding > FAP of the front side - gas phase etching - FAP of the rear side and simultaneously CMP of the rear side > edge polishing - FAP rear side and simultaneously CMP front side - edge polishing

The concluding step of the edge polishing is preferably followed by a final cleaning.

Moreover, the semiconductor wafer can be subjected to a thermal treatment or be provided with an epitaxial layer.

Patent claims:

1. A method for producing a semiconductor wafer, comprising in the stated order:

(a) double-side material-removing processing of the semiconductor wafer sliced from a single crystal;

(b) rounding of the edge of the semiconductor wafer;

(c) grinding of front and rear sides of the semiconductor wafer, wherein in each case one side of the semiconductor wafer is fixedly held by means of a wafer holder while the other side is processed by means of a grinding tool;

(d) polishing of at least one side of the semiconductor wafer by means of a polishing pad comprising fixedly bonded abrasives;

(e) treatment of both sides of the semiconductor wafer with an etching medium in conjunction with a material removal of not more than 1 µm per side of the semiconductor wafer;

(f) polishing of a front side of the semiconductor wafer using a polishing pad having fixedly bonded abrasives and simultaneous polishing of a rear side of the semiconductor wafer by means of a polishing pad which contains no abrasives, but in the case of which an abrasive-containing polishing agent is introduced between polishing pad and rear side of the semiconductor wafer;

(g) polishing of the edge of the semiconductor wafer;

(h) polishing of the rear side of the semiconductor wafer by means of a polishing pad comprising fixedly bonded abrasives and simultaneous polishing of the front side of the semiconductor wafer by means of a polishing pad which contains no fixedly bonded

abrasives, wherein an abrasive-containing polishing agent is introduced between polishing pad and front side of the semiconductor wafer.

2. The method as claimed in claim 1, wherein simultaneous double-side grinding (DDG) is involved in step (a).

3. The method as claimed in claim 1, wherein step (a) is effected by means of PPG.

4. The method as claimed in claim 3, wherein the semiconductor wafer is provided with a rounded edge as early as before the PPG step in accordance with step (a) is carried out, and the edge of the semiconductor wafer is rounded once again in accordance with step (b) after the PPG step has been carried out.

5. The method as claimed in any of claims 1 to 4, wherein the grinding of front and rear sides in accordance with step (c) is effected sequentially.

6. The method as claimed in any of claims 1 to 5, wherein the grinding of front and rear sides in accordance with step (c) is effected by means of a grinding tool having a grain size of #2000 - #8000.

7. The method as claimed in any of claims 1 to 6, wherein the front side of the semiconductor wafer is polished in step (d).

8. The method as claimed in any of claims 1 to 6, wherein the rear side of the semiconductor wafer is polished in step (d).

9. The method as claimed in any of claims 1 to 6, wherein front and rear sides of the semiconductor wafer are polished in step (d).

10. The method as claimed in any of claims 1 to 9, wherein in step (d) a polishing agent solution that is free of solids is introduced between that side of the semiconductor wafer which is to be polished and the polishing pad.

11. The method as claimed in any of claims 1 to 10, wherein the polishing pad used in step (d) comprises abrasive particles selected from the group consisting of silicon carbide, boron nitride, diamond and oxides of the elements cerium, aluminum, silicon, zirconium.

12. The method as claimed in claim 11, wherein the grain sizes of the abrasive particles are greater than or equal to 0.1 µm and less than or equal to 1.0 µm.

13. The method as claimed in any of claims 1 to 12, wherein in step (f) the material removal per side of the semiconductor wafer is at least 0.1 nm and at most 1 µm.

14. The method as claimed in claim 13, wherein in step (f) the semiconductor wafer is treated with a gaseous medium containing hydrogen fluoride and at least one oxidizing agent that oxidizes the surface of the semiconductor wafer.

15. The method as claimed in any of claims 1 to 14, wherein in step (g) the edge of a centrally rotating semiconductor wafer is pressed with a specific force against a centrally rotating polishing drum, wherein a polishing pad containing fixedly bonded abrasives is applied to the

polishing drum and a polishing agent solution containing no solids is continuously supplied.

16. The method as claimed in claim 15, wherein the polishing pad containing abrasives that is used in step (g) corresponds to a polishing pad as claimed in claim 11 or 12.

17. The method as claimed in any of claims 1 to 16, wherein the one polishing pad containing abrasives that is used in steps (f) and (h) corresponds to a polishing pad as claimed in claim 11 or 12.

18. The method as claimed in claim 17, wherein the other polishing pad in each case comprises no abrasives and has a porous matrix.

19. The method as claimed in any of claims 1 to 18, wherein the abrasive-containing polishing agent used in steps (f) and (h) comprises particles selected from the group consisting of one or more of the oxides of the elements aluminum, cerium or silicon.

20. The method as claimed in any of claims 1 to 18, wherein the polishing agent is colloidally dispersed silica.

21. The method as claimed in any of claims 1 to 20, wherein a two-stage edge polishing is effected, wherein a first edge polishing is effected in step (g) and the second edge polishing is effected after step (h).

22. The method as claimed in claim 21, wherein the second edge polishing is effected with supply of an abrasive-containing polishing agent slurry which corresponds to the polishing agent in claim 19 or 20.

23. The method as claimed in any of claims 1 to 22, wherein an additional polishing of the rear side is effected after step (h) wherein the rear side is polished in three steps in each case using a polishing pad which contains an abrasive material bonded in the polishing pad and which is pressed onto the rear side of the semiconductor wafer with a polishing pressure, wherein in the first step a polishing agent free of solids, whereas in the second and third steps a polishing agent containing abrasive materials is introduced between polishing pad and rear side of the semiconductor wafer, wherein a polishing pressure in the first and second steps of 8-15 psi is reduced to 0.5-5 psi in the third step.