(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 February 2002 (21.02.2002)

PCT

(10) International Publication Number
WO 02/015249 A3

(51) International Patent Classification[7]: H01L 21/3065

(21) International Application Number: PCT/US01/25391

(22) International Filing Date: 13 August 2001 (13.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/637,838 12 August 2000 (12.08.2000) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US]; P.O. Box 450A, Santa Clara, CA 95052 (US).

(72) Inventors: **LIU, Wei**; 5035 Moorpark Avenue, San Jose, CA 95129 (US). **WILLIAMS, Scott**; 107 S. Mary Avenue #102, Sunnyvale, CA 94086 (US). **YUEN, Stephen**; 2435 Ruth Cabral Way, Santa Clara, CA 95050 (US). **MUI, David**; 1848 Sheri Ann Circle, San Jose, CA 95131 (US).

(74) Agents: **BERNADICOU, Michael, A.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States *(national)*: CN, JP, KR, SG.

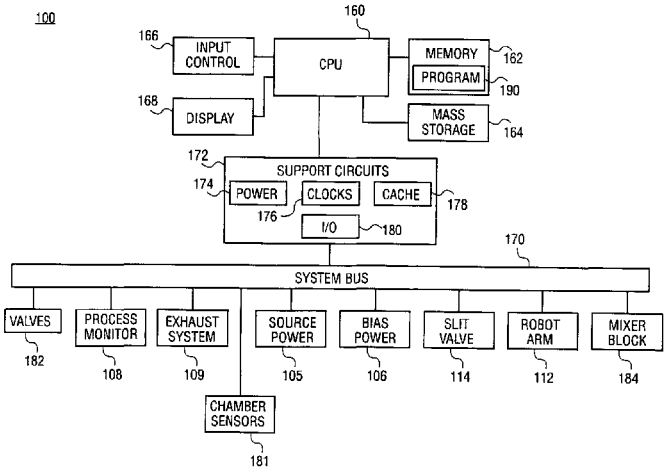
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

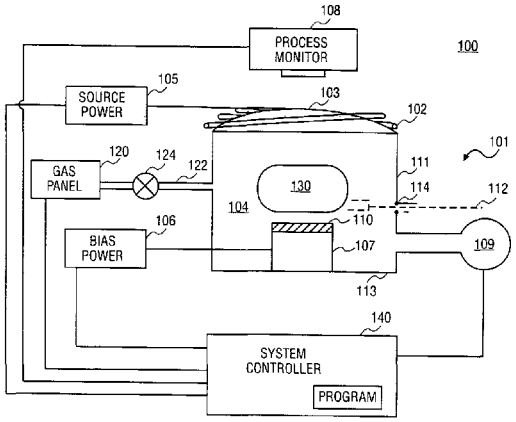
Published:
— *with international search report*

(88) Date of publication of the international search report:
12 September 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: INTEGRATED SHALLOW TRENCH ISOLATION PROCESS





(57) Abstract: A method for processing a silicon substrate disposed in a substrate process chamber includes transferring the substrate into the substrate process chamber. The substrate having a hard mask formed thereon and a patterned photoresist overlying the hard mask to expose portions of the hard mask. The chamber being the type having a source power system and a bias power system. The method further includes etching the exposed portions of the hard mask to expose portions of the silicon substrate underlying the hard mask. Tehereafter, the patterned photoresist is exposed to a fist plasma formed from a first process gas to remove the photoresist from the hard mask. Thereafter, the exposed silicon substrate is etched by exposing the substrate to a second plasma formed from a second process by applying RF energy from the source power system and biasing the plasma toward the substrate. The substrate is transferred out of the substrate processing chamber.

WO 02/015249 A3