METHODS OF FORMING SEMICONDUCTOR DEVICES USING EMBEDDED L-SHAPE SPACERS

BACKGROUND OF THE INVENTION

[0001] The present disclosure relates to semiconductor devices and methods of forming such devices using an embedded L-shape spacer.

[0002] Both theoretical and empirical studies have demonstrated that carrier mobility in metal oxide semiconductor field effect transistors (MOSFET's) can be greatly increased when a stress of sufficient magnitude is applied to the conduction channel region of a transistor to create a strain therein.

[0003] Accordingly, it has been proposed to increase the performance of MOSFET's by applying a stress enhancement layer to the channel regions. Most prior art methods require the use of multiple spacers and multiple etching steps. Unfortunately, the use of multiple spacers can lead to significant processing costs and the use of multiple etching steps, particularly when etching causing significant recesses in the silicon layers and/or etching away of silicide, which can lead to decreased transistor performance.

[0004] Therefore, there is a need for methods that overcome and/or mitigate one or more of the above and or other deleterious effects of prior art methods.

159159

G00002

BRIEF DESCRIPTION OF THE INVENTION

[0005]A method of forming a semiconductor device is provided. The method includes defining an L-shaped spacer on each side of a gate region of a substrate and embedding the L-shaped spacers in an oxide layer so that the oxide layer extends over a portion of the substrate a predetermined distance from a lateral edge of the L-shaped spacer.

[0006]A method of forming a semiconductor device is also provided that includes depositing a first oxide layer over a gate region and a semiconductor substrate, depositing a nitride layer on the first oxide layer, depositing a second oxide layer on the nitride layer, etching the first oxide layer, the second oxide layer, and the nitride layer to form an L-shaped spacer on each side of the gate region, and depositing a third oxide layer on the L-shaped spacers so that the third oxide layer covers a portion of the semiconductor substrate a predetermined distance from a lateral edge of the L-shaped spacer.

[0007]A semiconductor device is provided that includes a gate region, an L-shaped spacer, a source-drain region, and a silicide region. The gate region is on a semiconductor substrate. The L-shaped spacer is defined on at least one side of the gate region and includes a lateral edge. The source-drain region has an edge that is less than about ±200 Anstroms from the lateral edge. The silicide region has an edge that is substantially co-planar to the lateral edge.

[0008]The above-described and other features and advantages of the present invention will be appreciated and understood by those skilled in the art from the following detailed description, drawings, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]FIG. 1 is a schematic depiction showing a cross-sectional view of a semiconductor device according to the present disclosure, after formation of a pair of L-shaped spacers with additional oxide layer on opposing sides of a gate region;

[0010]FIG. 2 illustrates the semiconductor device of FIG. 1, after embedding the L-shaped spacers in an oxide layer;

[0011]FIG. 3 illustrates the semiconductor device of FIG. 2, after an etching process to remove a portion of the oxide layer;

[0012]FIG 4 illustrates the semiconductor device of FIG. 3, during ion implementation for defining ion implant regions;

[0013]FIG 5 illustrates the semiconductor device of FIG. 4, after annealing the implant regions to define source-drain regions;

[0014]FIG. 6 illustrates the semiconductor device of FIG. 5, after removal of the remaining portions of the oxide layer;

[0015]FIG. 7 illustrates the semiconductor device of FIG. 6, after forming silicide regions; and

[0016]FIG. 8 illustrates the semiconductor device of FIG. 7, after deposition of a stress layer.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Referring now to the drawings and in particular to FIGS. 1 through 8, an exemplary embodiment of a method according to the present disclosure of making a semiconductor device 10 is illustrated.

[0018] As shown in FIG. 1, semiconductor device 10 includes a substrate 12, a gate region 14, and a pair of L-shaped spacers 16 on opposite sides of the gate region, and a second oxide 26 on the L-shaped spacers. For purposes of clarity, semiconductor device 10 is illustrated by way of example having one gate region 14. Of course, it is contemplated by the present disclosure for semiconductor device 10 to include any number of gate regions and for some or all of such gate regions to have L-shaped spacers 16.

[0019] Gate region 14 includes a gate dielectric 18 and a gate material 20 overlying the gate dielectric. Gate dielectric 18 may be a conventional oxide, an oxynitride, other high-k materials, or any combinations thereof. Gate material 2-is, preferably, polysilicon, but may comprise of any conductive material. Substrate 12 is preferably silicon, but may be any semiconducting material or a layered substrate including at least one semiconducting material.

[0020] Each L-shaped spacer 16 includes a first oxide layer 22 and a nitride layer 24. In addition, the L-shaped spacer 16 can include a second oxide layer 26 disposed thereon during the process. First and second oxide layers 22, 26 can be made of many forms of silicon oxide, such as, but not limited to, low temperature oxide (LTO), Tetraethyl Orthosilicate (TEOS) oxide, High Density Plasma (HDP) oxide, atomic layer deposition (ALD) oxide, thermal oxide as well, and any combinations thereof. Nitride layer 24 can be made of materials, such as, but not limited to, of Rapid Thermal Chemical Vapor Deposition (RTCVD) nitride, Plasma Enhanced Chemical Vapor Deposition (PECVD) nitride, liquid phase chemical vapor deposition (LP CVD) nitride,

High Density Plasma (HDP) nitride, atomic layer deposition (ALD) nitride, and any combinations thereof.

[0021] During the method of the present disclosure, first oxide layer 22 is deposited on gate region 14. Next, nitride layer 24 is deposited on first oxide layer 22 and second oxide layer 26 is deposited on the nitride layer. Finally, the oxide and nitride layers 22, 24, 26 are etched to provide L-shaped spacers 16 as shown in FIG. 1. For example, a reactive-ion-etch (RIE) can be used to form L-shaped spacers 16.

[0022] L-shaped spacer 16 has a vertical component and a horizontal component, where the horizontal component is formed on a portion of substrate 12 and the vertical component is formed on the walls of gate region 14.

[0023] Advantageously, the method of the present disclosure embeds L-shaped spacer 16 in a third oxide layer 28 as shown in FIG. 2. For example, third oxide layer 28 is deposited such that a portion 30 of substrate 12 is covered by the third oxide layer. Thus, portion 30 extends a predetermined distance from a lateral edge 32 of L-shaped spacer 16. Preferably, portion 30 extends a predetermined distance of up to about 600 Angstroms from lateral edge 32, more preferably about between about 200 to about 400 Angstroms.

[0024] After deposition of third oxide layer 28, the third oxide layer is etched to reveal an upper portion 34 of polysilicon gate material 20 as shown in FIG. 3. For example, a reactive-ion-etch (RIE) can be used to remove portions of third oxide layer 28.

[0025] As shown in FIG. 4, semiconductor device 10 is subjected to a known ion implantation process 36 to define ion implant regions 38 in substrate 12.

Advantageously, third oxide layer 28 covers portion 30 of substrate 12 so that these portions are shielded from process 36. In this manner, ion implant regions 38 are defined the predetermined distance from lateral edges 32.

[0026] After ion implantation process 36, semiconductor device 10 is subjected to a known annealing process to diffuse the implanted ions in ion implant regions 38 to define source-drain regions 40 in substrate 12. As shown in FIG. 5, source-drain regions 40 have an edge 42 that is less than about ±200 Angstroms from lateral edge 32. In some embodiments, edge 42 is co-planar with lateral edge 32.

[0027] After defining source-drain regions 40, second and third oxide layers 26, 28 are removed as shown in FIG. 6. For example, a reactive-ion-etch (RIE) can be used to remove second and third oxide layers 26, 28.

[0028] It can be seen that portion 30 of substrate 12 that was previously covered by third oxide layer 28 is now exposed by the removal of the third oxide layer. As such, semiconductor device 10 can be exposed to a known process to define silicide contacts 44 on exposed surfaces of substrate 12 as shown in FIG. 7. In this manner, silicide contacts 44 can be defined with an inner edge 46 that is substantially co-planar to lateral edge 32. Advantageously, silicide contacts 44 can be defined without need for subsequent etching steps, which are known to damage the silicide contacts. Thus, semiconductor device 10 includes silicide contacts 44 having inner edge 46 substantially co-planar to lateral edge 32, where the silicide contacts are free of etch induced damage.

[0029] In order to induce and/or enhance stresses in the channel, semiconductor device can include a stress-enhancing layer 48 deposited thereon by known processes as shown in FIG. 8. Stress-enhancing layer

preferably comprises CA nitride, such as but not limited to Rapid Thermal Chemical Vapor Deposition (RTCVD) nitride, Plasma Enhanced Chemical Vapor Deposition (PECVD) nitride, High Density Plasma (HDP) nitride, and any combinations thereof.

[0030] Those skilled in the art will understand that various changes may be made to the invention and equivalents may be substituted for elements thereof without departing from the scope of the present disclosure. In addition, many modifications may be made to adapt a particular situation or material to the disclosure without departing from the scope thereof. It is intended that the present disclosure not be limited to the particular embodiments disclosed, but that the disclosure will include all embodiments falling within the scope of the appended claims.

CLAIMS

1. A method of forming a semiconductor device, comprising:

defining an L-shaped spacer on each side of a gate region of a substrate; and

embedding said L-shaped spacers in an oxide layer so that said oxide layer extends over a portion of said substrate a predetermined distance from a lateral edge of said L-shaped spacer.

2. The method of claim 1, wherein said predetermined distance is up to about 600 Angstroms

3. The method of claim 1, wherein said predetermined distance is between about 200 to about 400 Angstroms.

4. The method of claim 1, further comprising:

etching said oxide layer to reveal a top portion of said gate region and a top portion of said L-shaped spacer; and

implanting ions in said substrate to define an implant region at opposite sides of said oxide layer.

5. The method of claim 4, further comprising annealing said implant regions to define source-drain regions, said source-drain regions each having an edge that is less than about 200 Angstroms away from said lateral edge.

6. The method of claim 5, wherein said edge is co-planar with said lateral edge.

7. The method of claim 5, further comprising:

removing said oxide layer; and

forming a silicide region having an inner edge substantially co-planar to said lateral edge.

8. The method of claim 7, further comprising depositing a nitride stress layer over said silicide regions, said L-shaped spacer, and said top portion of said gate region.

9. A method of forming a semiconductor device, comprising:

depositing a first oxide layer over a gate region and a semiconductor substrate;

depositing a nitride layer on said first oxide layer;

depositing a second oxide layer on said nitride layer;

etching said first oxide layer, said second oxide layer, and said nitride layer to form an L-shaped spacer on each side of said gate region; and

depositing a third oxide layer on said L-shaped spacers so that said third oxide layer covers a portion of said semiconductor substrate a predetermined distance from a lateral edge of said L-shaped spacer.

10. The method of claim 9, wherein said predetermined distance is up to about 600 Angstroms.

11. The method of claim 9, wherein said predetermined distance is between about 200 to about 400 Angstroms.

12. The method of claim 9, further comprising:

etching said third oxide layer to reveal a top portion of said gate region and a top portion of said L-shaped spacer; and

implanting ions in said substrate to define an implant region in said substrate at said predetermined distance from said lateral edge.

13. The method of claim 12, further comprising annealing said implant region to define a source-drain region, said source-drain region having an edge that is less than about 200 Anstroms from said lateral edge.

14. The method of claim 13, wherein said edge is co-planar with said lateral edge.

15. The method of claim 13, further comprising:

removing said second and third oxide layers; and

forming a silicide region having an edge substantially co-planar to said lateral edge.

16. The method of claim 15, further comprising depositing a nitride stress layer over said silicide region, said L-shaped spacer, and said top portion of said gate region.

17. A semiconductor device comprising:

a gate region on a semiconductor substrate;

an L-shaped spacer defined on at least one side of said gate region, said L-shaped spacer having a lateral edge;

a source-drain region having an edge that is less than about ±200 Anstroms from said lateral edge; and

a silicide region having an edge that is substantially co-planar to said lateral edge.

18. The semiconductor device of claim 17, wherein said silicide region is free of etch induced damage.

19. The semiconductor device of claim 17, further a nitride stress layer over said silicide region, said L-shaped spacer, and said gate region.