CLAIMS

What is claimed is:

1. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region;

p-type and n-type source/drain regions in the substrate and adjacent to the channel region;

a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

a metal-germanide source/drain contact on the boron doped germanium layer.

2. The device of claim 1 wherein the device is one of a planar or FinFET transistor.

3. The device of claims 1 or 2 wherein the boron doped germanium layer is only on p-type source/drain regions of the device.

4. The device of any of the preceding claims further comprising an interlayer dielectric.

5. The device of the preceding claims, further comprising at least one of:

a graded buffer between the substrate and at least one of the p-type and n-type source/drain regions; and

a graded buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer.

6. The device of claim 5 wherein the graded buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with

the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 95 atomic %.

7. The device of claim 6 wherein the high concentration reflects pure germanium.

8. The device of claims 5, 6, or 7 wherein the graded buffer between the at least one of the p-type and n-type source/drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}.

9. The device of any of the preceding claims wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

10. The device of any of the preceding claims wherein the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %.

11. The device of any of the preceding claims wherein the p-type and n-type source/drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

12. The device of any of claims 1 through 4 wherein the p-type and n-type source/drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the at least one p-type and n-type source/drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least

one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}.

13. The device of any of the preceding claims wherein the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}.

14. An electronic device comprising:

a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as defined in any of the preceding claims.

15. The electronic device of claim 14 wherein the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices.

16. The electronic device of claims 14 or 15 wherein the device is a computing device.

17. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

p-type and n-type source/drain regions in the substrate and adjacent to the channel region, each of the p-type and n-type source/drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers;

a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

a metal-germanide source/drain contact on the boron doped germanium layer;

wherein the device is one of a planar or FinFET transistor.

18. The device of claim 17, the device further comprising:

a buffer between at least one of the p-type and n-type source/drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 2E20 cm^{-3}.

19. The device of claims 17 wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

20. The device of claim 17 wherein the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %.

21. The device of claim 20 wherein the p-type and n-type source/drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

22. The device of claim 17 wherein the p-type and n-type source/drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the p-type and n-type source/drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the p-type and n-type source/drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the p-type and n-type source/drain regions

CLAIMS

What is claimed is:

[Claim 1]

A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region;

p-type and n-type source/drain regions in the substrate and adjacent to the channel region;

a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3};

a metal-germanide source/drain contact on the boron doped germanium layer; and

a graded buffer between the p-type source/drain region and the boron doped germanium layer, wherein the graded buffer has a boron concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 1E20 cm^{-3}.

[Claim 2]

The device of claim 1 wherein the device is one of a planar or FinFET transistor.

[Claim 3]

The device of claims 1 or 2 wherein the boron doped germanium layer is only on p-type source/drain regions of the device.

[Claim 4]

The device of any of the preceding claims further comprising an interlayer dielectric.

[Claim 5]

The device of the preceding claims, comprising

a graded buffer between the substrate and the p-type source/drain region .

[Claim 6]

The device of any of the preceding claims wherein the graded buffer between the p-type source/drain region and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the p-typesource/drain region to a high concentration in excess of 95 atomic %.

[Claim 7]

The device of claim 6 wherein the high concentration reflects pure germanium.

[Claim 8]

The device of any of the preceding claims wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

[Claim 9]

The device of any of the preceding claims wherein the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a

base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %.

[Claim 10]

The device of any of the preceding claims wherein the p-type source/drain region comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

[Claim 11]

The device of any of claims 1 through 4 wherein the p-type and n-type source/drain regions comprise silicon or silicon germanium, the buffer having a germanium concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 1E20 cm^{-3}.

[Claim 12]

The device of any of the preceding claims wherein the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}.

[Claim 13]

An electronic device comprising:

a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as defined in any of the preceding claims.

[Claim 14]

The electronic device of claim 13 wherein the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices.

[Claim 15]

The electronic device of claim 13 or 14 wherein the device is a computing device.

[Claim 16]

A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

p-type and n-type source/drain regions in the substrate and adjacent to the channel region, each of the p-type and n-type source/drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers;

a boron doped germanium layer on at least a portion of the p-type source/drain region, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3};

a metal-germanide source/drain contact on the boron doped germanium layer; and

a graded buffer between the p-type source/drain region and the boron doped germanium layer,

wherein the graded buffer has a boron concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 1E20 cm^{-3}, and

wherein the device is one of a planar or FinFET transistor.

[Claim 17]

The device of claim 16, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 2E20 cm^{-3}.

[Claim 18]

The device of claims 16, wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

[Claim 19]

The device of claim 16wherein the p-type and n-type source/drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %.

[Claim 20]

The device of claim 19 wherein the p-type source/drain region have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

[Claim 21]

The device of claim 16 wherein the p-type and n-type source/drain regions comprise silicon germanium having a fixed germanium concentration, and , the buffer having a germanium concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the p-typesource/drain region to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

[Claim 22]

A method for forming a transistor device, comprising:

providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region; and

providing p-type and n-type source/drain regions in the substrate and adjacent to the channel region;

providing a boron doped germanium layer on at least a portion of the p-type source/drain region, the boron doped germanium layer comprising a germanium concentration in excess of 90

atomic % and a boron concentration in excess of 1E20 cm^{-3};

providing metal-germanide source/drain contacts on the boron doped germanium layer; and

providing a graded buffer between the p-type source/drain region and the boron doped germanium layer, wherein the graded buffer has a boron concentration that is graded from a base level concentration compatible with the p-type source/drain region to a high concentration in excess of 1E20 cm^{-3}.