CLAIMS

1. A semiconductor device comprising:

a gate structure including a gate electrode and a gate capping pattern on an upper surface of the gate electrode;

a source/drain pattern on at least one side of the gate structure;

a source/drain contact on and connected with an upper surface of the source/drain pattern, the source/drain contact extending along a sidewall of the gate electrode; and

an etch stop layer disposed on the source/drain contact,

wherein an upper surface of the source/drain contact includes a convex curved surface,

an upper surface of the gate capping pattern includes a concave curved surface, and

the etch stop layer is continuously disposed on the convex curved surface of the upper surface of the source/drain contact and the concave curved surface of the upper surface of the gate capping pattern.

2. The semiconductor device of claim 1, wherein a portion of the source/drain contact protrudes above an upper surface of the gate capping pattern.

3. The semiconductor device of claim 2, wherein

the source/drain contact includes a source/drain filling layer and a source/drain barrier layer extended along a sidewall of the source/drain filling layer, and

the source/drain filling layer and the source/drain barrier layer protrude above the upper surface of the gate capping pattern.

4. The semiconductor device of claim 2, wherein

the source/drain contact includes a source/drain filling layer and a source/drain barrier layer extended along a sidewall of the source/drain filling layer,

a portion of the source/drain filling layer protrudes above the upper surface of the gate capping pattern, and

the source/drain barrier layer is below the upper surface of the gate capping pattern.

5. The semiconductor device of any one of claims 1 to 4, further comprising:

a gate contact passing through the gate capping pattern and connecting with the gate electrode,

wherein an upper surface of the gate contact includes a convex curved surface.

6. The semiconductor device of any one of claims 1 to 4, further comprising:

a gate contact passing through the gate capping pattern and connecting with the gate electrode,

wherein an upper surface of the gate contact is a flat plane.

7. The semiconductor device of claim 1 or claim 2, wherein

the source/drain contact includes a source/drain filling layer, and

an upper surface of the source/drain filling layer is included in the upper surface of the source/drain contact including the convex curved surface.

8. The semiconductor device of claim 7, wherein the source/drain contact further includes a source/drain barrier layer extended along a sidewall of the source/drain filling layer.

9. The semiconductor device of any one of claims 1 to 8, wherein the upper surface of the source/drain contact includes a first portion having the convex curved surface and a second portion having a concave curved surface.

10. A semiconductor device comprising:

a gate structure including a gate electrode and a gate capping pattern on an upper surface of the gate electrode;

a source/drain pattern on at least one side of the gate structure;

a source/drain contact on and connected with an upper surface of the source/drain pattern; and

an etch stop layer disposed on the source/drain contact,

wherein at least a portion of the source/drain contact protrudes above an upper surface of the gate capping pattern, and

the upper surface of the gate capping pattern includes a concave curved surface,

an upper surface of the source/drain contact includes a convex curved surface, and

the etch stop layer is continuously disposed on the convex curved surface of the upper surface of the source/drain contact and the concave curved surface of the upper surface of the gate capping pattern.

11. The semiconductor device of claim 10, wherein an upper surface of the source/drain contact includes a first portion having a convex curved surface and a second portion having a concave curved surface.

12. The semiconductor device of claim 10 or claim 11, wherein

the source/drain contact includes a source/drain filling layer and a source/drain barrier layer extending along a sidewall of the source/drain filling layer,

at least a portion of the source/drain filling layer and the source/drain barrier layer protrude above the upper surface of the gate capping pattern, and

at least a portion of the source/drain filling layer protrudes above an upper surface of the source/drain barrier layer.

13. The semiconductor device of any one of claims 10 to 12, further comprising:

a gate contact passing through the gate capping pattern and connecting with the gate electrode,

wherein an upper surface of the gate contact includes a convex curved surface.

14. A semiconductor device comprising:

an active pattern including a lower pattern and a sheet pattern on the lower pattern;

a gate structure on the active pattern, the gate structure including a gate electrode and a gate capping pattern, the gate electrode surrounding the sheet pattern, and the gate capping pattern on an upper surface of the gate electrode;

a source/drain pattern on at least one side of the gate structure;

a source/drain contact on and connected with an upper surface of the source/drain pattern;

a gate contact passing through the gate capping pattern and connecting with the gate electrode; and

an etch stop layer disposed on the source/drain contact,

wherein a portion of the source/drain contact and a portion of the gate contact protrude above an upper surface of the gate capping pattern, and

an upper surface of the source/drain contact includes a convex curved surface,

an upper surface of the gate capping pattern includes a concave curved surface, and

the etch stop layer is continuously disposed on the convex curved surface of the upper surface of the source/drain contact and the concave curved surface of the upper surface of the gate capping pattern.

15. The semiconductor device of claim 14, wherein

the source/drain contact includes a source/drain filling layer and a source/drain barrier layer extended along a sidewall of the source/drain filling layer, and

a portion of the source/drain filling layer and a portion of the source/drain barrier layer protrude above the upper surface of the gate capping pattern.

16. The semiconductor device of claim 14 or claim 15, wherein

the gate contact includes a gate contact filling layer and a gate contact barrier layer extending along a sidewall of the gate contact filling layer, and

the gate contact filling layer and the gate contact barrier layer protrude above the upper surface of the gate capping pattern.