

SPECIFICATION

Focussing system for a photographic or cinematographic camera

5 The present invention relates to a focussing system for a photographic or a cinematographic camera comprising a radiation emitting element for producing a measuring beam, radiation receiving elements positioned adjacent to each other and arranged to receive radiation produced by the radiation emitting element, an output stage, and a lens positioned in front of the radiation receiving elements, the radiation receiving elements and the lens being movable relative to each other.

10 According to the present invention, there is provided a focussing system for a photographic or a cinematographic camera comprising a radiation emitting element for producing a measuring beam, radiation receiving elements positioned adjacent to each other and arranged to receive radiation produced by the radiation emitting element, an output stage, a lens positioned in front of the radiation receiving elements, the radiation receiving elements and the lens being movable relative to each other, a control circuit for energizing the radiation emitting element, during each cycle of the control circuit the radiation emitting element being energized for a predetermined duration by pulses having a predetermined frequency, and first and second multiplex stages, each multiplex stage having controllable switching elements and the switching elements of each multiplex stage being successively enabled during successive cycles of the control circuit, the input of each switching element of the first multiplex stage being responsive to an associated one of the radiation receiving elements and the output of each switching element of the second multiplex stage being connected to an associated memory element, the memory elements being connected to the output stage, and signal processing stages being provided between the commonly connected output of the first multiplex stage and the commonly connected input of the second multiplex stage.

50 The presence of the multiplex stages has the advantage of a saving in amplifier and filter stages, the filtering of signals from the radiation receiving elements being performed by the same filter and amplifier stages. In addition to the saving in further electrical components, such as capacitors, it is also ensured that the signals are identically processed, amplified and evaluated. A further advantage is that with the aid of the multiplex stages the separation between useful signals and interference signals is considerably improved. A further advantage lies in the fact that the switching elements of the multiplex stages need only be enabled during the period of energization of the radiation emitting element.

ment. No signal transmission occurs when the switching elements are not enabled so that the risk of evaluation or transmission of interference signals is greatly reduced. The use of memory elements has the advantage that the signals allowed to pass when the switching elements are enabled can also be stored and evaluated after the switching elements have been disenabled.

70 Conveniently, there are two radiation receiving elements and a convex lens is provided in front of the radiation receiving elements for concentrating the radiation received from the radiation emitting element into an area which is small relative to the area of the radiation receiving elements.

Preferably, the radiation receiving elements comprise infra-red sensitive diodes, each diode being connected to the inverting input of a differential amplifier, the non-inverting input of which is connected to earth, and each differential amplifier being arranged so that the amplification factor for DC input components does not exceed a predetermined value and the amplification factor for AC input components increases with frequency.

By connecting the non-inverting inputs of the differential amplifiers to earth, it is advantageously ensured that an increase in clarity is produced in a linear manner and not in a logarithmic manner. By limiting the DC amplification factor to a predetermined value, the amplifiers are prevented from being saturated by DC signals. Thus, the high value infrared components present in day light are advantageously not subject to preferential amplification. In consequence, primarily AC signals are amplified and transmitted.

The differential amplifiers can alternatively be located in the commonly connected stages between the two multiplex stages.

The differential amplifiers may comprise operational amplifiers, the output of each amplifier being connected to its inverting input through a chain of high value linear resistors, and a tapping of the chain being connected to earth through a capacitor.

The capacitor provides that the amplification of AC signals increases with frequency.

115 The output of each differential amplifier may be connected to the input of an AC amplifier, the output of which is connected to the input of an associated one of the switching elements of the first multiplex stage.

120 Preferably, the control circuit comprises an oscillator and a counter operating as a frequency divider, the last output of the counter either alone or in combination with one of the other outputs providing a resetting signal for the counter, the last output being connected to the input of a first gate, another input of which is connected to the oscillator, and the radiation emitting device being controlled by the first gate.

130 Conveniently, a second gate is positioned

between the oscillator and the first gate, the second gate having one input connected to the oscillator, another input connected to one of the other outputs of the counter, and its output connected to the first gate.

In this manner, the first gate receives only one pulse from the oscillator during each counting cycle.

Advantageously, the first gate has a further input connected to a delay circuit, the delay circuit providing a signal for disabling the first gate for a predetermined period after the system is energized.

By disabling the first gate for this predetermined period, the oscillator is allowed to stabilize before the radiation emitting element is energized. The radiation emitting element is matched with reference to its power consumption and load to the nominal frequency of the oscillator and, if it were energized before the oscillator were stabilised, it could be overloaded.

Conveniently, the counter comprises an n -bit counter, the n -th output and one of the other outputs being connected to the inputs of an AND-gate, the output of which provides said resetting signal.

This provides that the pulse period of the n -th output is shortened and is equal in duration to the pulse period of the said other output.

Preferably, the last output of the counter is connected to the CLOCK input of a first bistable element, and the last but one output of the counter is connected to the CLOCK input of a second bistable element, the second bistable element being arranged so that its output signals are inverted each time a pulse appears at its CLOCK input, and the system further includes a gate-stage, the outputs of which are connected to the control inputs of the second multiplex stage, one set of inputs of which are connected to the outputs of the second bistable element, and the other set of inputs of which are connected to the output of the first bistable element.

Preferably, the outputs of the second bistable element are connected to the control inputs of the first multiplex stage.

With this arrangement, the switching elements of the first and second multiplex stages are enabled successively during successive cycles of the control circuit. Also, during each cycle of the control circuit, the appropriate switching element of the first multiplex stage is enabled and transmits signals to the following amplifier and filter stages in good time to receive signals produced by energization of the radiation emitting element whereas the appropriate switching element of the second multiplex stage is enabled for a shorter period. Thus, the appropriate switching element of the first multiplex stage is enabled before energization of the radiation emitting element and before the appropriate switching element

of the second multiplex stage is enabled. This reduces the effects of interference signals.

The second bistable element may comprise a D-flip-flop having a Q and $\bar{Q}$ output, the $\bar{Q}$ output being connected to the D-input thereof.

With this arrangement, the outputs of the second bistable element flip-flop are inverted each time a pulse appears at its CLOCK input.

Conveniently, the gate stage comprises two AND-gates and the first bistable element comprises a D-flip-flop having a Q -output, one input of each of the AND-gates being connected to the Q -output of the first bistable element flip-flop and the other inputs of the AND-gates being connected respectively to the Q and the $\bar{Q}$ outputs of the second bistable element flip-flop.

The system may further include a third gate and a fourth gate, the last output of the counter being connected through a second delay circuit to one input of each of the third and fourth gates and the other inputs of the third and fourth gates being connected to the outputs of the gate stage, and there may be two memory elements each comprising a D-flip-flop, the outputs of the third and fourth gates being connected respectively to the RESET inputs of the memory element flip-flops.

In this manner, it is ensured that the memory elements are reset immediately before receiving a signal produced as a result of the radiation receiving elements receiving radiation emitted by the radiation emitting element. Where the output stage produces a visual indication of focussing, the period between reset and receiving a new signal is so short that it is not perceived by the human eye.

Where a visual indication is produced, the output stage may comprise two light emitting diodes, which may be marked with arrows to indicate the direction in which the camera lens should be adjusted. The arrangement may be set so that either both diodes are energised or both diodes are de-energized when focus is obtained.

In an alternative arrangement, the output stage comprises an electric motor for driving the camera lens, the motor being connected to the memory elements through a further control circuit.

Where there are two memory elements each comprising a D-flip-flop, the system may include a fifth gate and a sixth gate, one input of the fifth gate being connected to the Q -output of one of the memory element flip-flops and the other input being connected to incandescent lamps and luminescent tubes flip-flop, one input of the sixth gate being connected to the Q -output of said other memory element flip-flop and the other input being connected to a current source through a switch associated with the camera focussing mechanism, the switch being closed when the

camera lens is focussed at infinity, and the outputs of the fifth and sixth gates being connected to the output stage.

Since the memory element flip-flops are reset when the radiation emitting element is energized and are set only when they receive a signal from the second multiplex stage, they remain reset in the absence of such a signal. This may occur when the object to be photographed is so far away from the camera that the intensity of the reflected signal is insufficient to cause setting of the flip-flops. Where the output stage comprises a pair of light emitting diodes, in these circumstances one of the diodes will be energized thereby indicating that the camera lens should be rotated towards its infinity setting. When the infinity setting is reached, the switch mentioned above will be closed thereby energizing the second diode and indicating that focus has been obtained. Thus, the absence of signals sufficient to cause setting of the flip-flops can be used to indicate that the lens must be moved to its infinity setting. In the event of an object coming into the measuring radiation path in the close-up range, the relevant diode is de-energized, with the result that it is indicated to the user that the camera lens must be rotated into a close-up position.

The present invention will now be described in more detail, by way of example, with reference to the accompanying drawings in which:—

Figures 1 and 2 shows a focussing system embodying the present invention; and

Figure 3 shows another focussing system embodying the present invention.

Fig. 1 shows a camera housing 1 with an infra-red radiation emitting diode 2 in the camera lens section. The infra-red radiation emitted by the diode 2 is collected by a lens 3 located in front of the infra-red diode 2. The illustration shows a camera lens 4 and a fixed shutter 5. The optical axis is referenced 6.

Two infra-red radiation receiving diodes are shown at 7 and 8 positioned to receive radiation produced from diode 2. They are located in front of a lens 9 which moves in the direction of arrows A or B on rotating a distance adjuster ring 10 forming part of the lens focussing mechanism. A convex lens collecting radiation received from the diode 2 is shown at 11. The lens 11 sharply focuses radiation into an area which is small compared with the receiving area of diodes 7, 8. By means of lens 9 the radiation sharply focussed by lens 11 is moved backwards and forwards along both infra-red receiving diodes 7 and 8, which are located alongside each other.

The infra-red emitting diode 2 and both infra-red receiving diodes 7 and 8 are connected to a circuit as shown in Fig. 2. As shown in Fig. 2, a battery 12 can be connected by means of a switch 13 to the circuit.

Capacitors 14 and 15 stabilise the supply voltage, and a diode 16 and a resistor 17 connected in series are also used for stabilisation. Two equal value resistors 18 and 19 act as a potential divider to provide an earth for part of the circuit.

The infra-red receiving diode 7 is connected to the inverting input of an operational amplifier 20, of which the non-inverting input is connected to earth. The infra-red receiving diode 8 is connected to the inverting input of an operational amplifier 21, the non-inverting input of which is connected to earth.

Two resistors 22, 23 and 24, 25 are located in the feedback branch of each of the operational amplifiers 20 and 21. By means of resistors 22 and 23 or 24 and 25 the amplification of DC signal components is fixed at a predetermined value. The common point between resistors 22 and 23 or 24 and 25 is connected to earth through a capacitor 26 or 27. This ensures that for AC input signals a frequency-dependent impedance is achieved. As the frequency increases, the AC impedance of both capacitors 26 and 27 reduces. As the frequency increases there is consequently an increase in amplification of AC signals. The resistors 22 and 23 are preferably of the same value as resistors 24 and 25. The same applies to both capacitors 26 and 27.

In the first input channel, a coupling capacitor 28 is connected between the output of operational amplifier 20 and the inverting input of an operational amplifier 29, in the feedback branch of which a resistor 30 is connected, establishing the amplification of operational amplifier 29 in conjunction with a further resistor 31. The operational amplifier 29 is an AC amplifier.

The same applies to an operational amplifier 32 in the second input channel, for which the inverting input is connected by a coupling capacitor 33 with the input of operational amplifier 21. In the feedback branch of the operational amplifier 32 a resistor 34 is connected, which together with a further resistor 34 defines the amplification of the operational amplifier 32.

Both input channels lead to a multiplexer 36 having two switching elements 37 and 38. The multiplex stage 36 has two outputs commonly connected to a high pass filter consisting of an operational amplifier 39, resistors 40 and 41 as well as capacitors 42 and 43. The high pass filter is arranged in such a way that interference voltages in the frequency range of the mains AC supply and in the range of the interference voltages of incandescent lamps and luminescent tubes are not allowed through at double main frequency.

The output of the high pass filter 40 and 43 is connected by means of a coupling capacitor 44 to the input of an AC amplifier, consisting of an operational amplifier 45 and

feedback resistors 46 and 47. The output of operational amplifier 45 is connected by means of a coupling capacitor 48 to the input of a further operational amplifier 49, the amplification factor of which is determined by both resistors 50 and 51. A resistor 52 serves to discharge capacitor 48 when no signal is available.

A second multiplex stage 53 has two switching elements 54 and 55. Switching element 54 of the multiplex stage 53 is connected to the CLOCK input of a D-flip-flop 56, whereas switching element 55 of multiplex stage 53 is connected to the CLOCK input of a second D-flip-flop 57.

The D-inputs of both flip-flops 56 and 57 are connected to the positive terminal of battery 12.

The Q-output of flip-flop 57 and the $\bar{Q}$ -output of flip-flop 56 are connected to the two inputs of an OR-gate 58, the output of which is connected through a resistor 59 to the base of a transistor 60.

The Q-output of flip-flop 56 is connected to one input of an OR-gate 62. The other input of OR-gate 62 is connected to the positive terminal of the battery 12 through a switch 61. The output of OR-gate 62 is connected through a resistor 63 to the base of a transistor 64. The switch 61 is associated with the focussing mechanism of the camera lens and is arranged so that it closes when the lens is at its infinity setting. The positive side of the switch 61 is connected to the negative terminal of the battery through a resistor 65.

The collector of transistor 60 is connected through a light emitting diode 66 and an associated resistor 67 to the positive terminal of the battery 12. The collector of transistor 64 is connected through a light-emitting diode 68 and an associated resistor 69 to the positive terminal of the battery 12. The light emitting diodes 66 and 68 show the user of the camera by means of their relevant arrows, the direction in which the lens must be adjusted to obtain focus.

A square wave oscillator 70 is connected to the CLOCK input of a counter 71. The first output Q 1 of counter 71 leads to a NOR-gate 72, the other input of which is connected to the oscillator 70. The output of NOR-gate 72 is connected to the first input of an AND-gate 73. Thus at this point of gate 73, pulses are applied at the frequency of the oscillator 70 but blocked during the period of pulses at output Q 1. A further input of gate 73 is connected to output Q 4 of counter 71. The period of pulses at output Q 4 is shorter than the period of pulses at output Q 3. Output Q 4 as well as output $\bar{Q}$ 2 are connected to an AND gate 74, the output of which is connected to the RESET input R of counter 71. In this way the period of pulses at output Q 4 is the same as the period of pulses at output Q 2.

The components 70 to 74 comprise a control circuit, each cycle of which is terminated by the reset pulse produced by AND-gate 74.

The output Q 3 is connected to the CLOCK input of a D-flip-flop 75, the D-input is connected with its output $\bar{Q}$. The output Q of the D-flip-flop 75 is connected to the control input of switching element 38 of multiplex stage 36 and the output $\bar{Q}$ is connected to the control input of switching element 37 of multiplex stage 36. The connection of the D-input with the $\bar{Q}$ -input of the D-flip-flop ensures that the potential at the outputs Q and $\bar{Q}$ are inverted each time a positive going pulse is received from output Q 3. Between the two positive going edges of two adjacent pulses, the output Q or $\bar{Q}$ is of positive or negative potential.

The switching elements 37 and 38 of the multiplex stage 36 are consequently enabled and disenabled alternately. Output Q is also connected to the first input of an AND gate 77. A connection to the first input of an AND gate 76 leads from the output $\bar{Q}$ of D-flip-flop 75. The second inputs of both AND-gates 76 and 77 are connected in common to the output Q of a further D-flip-flop 78, of which the CLOCK input is connected to output Q 4 of counter 71. On the positive going edge of each Q 4 pulse, the output Q produces a positive control potential. The RESET input R of D-flip-flop 78 is connected to the output of AND-gate 74. At the end of each Q 4 pulse, the D-flip-flop 78 is thus reset, which results in the potential at output Q dropping to zero. A driving potential is thus applied to the corresponding inputs of AND-gates 76 and 77 in sequence with the Q 4 pulse of counter 71. The outputs of both AND gates 76 and 77 are connected to the control inputs of switching elements 54 and 55 of the multiplex stage 53. Whereas multiplex stage 36 is controlled by the positive going edge of the Q 3 pulses from counter 71, the control of the second multiplex stage 53 only occurs with the positive going edge of the Q 4 pulses from counter 71. Furthermore the relevant switching elements 36 and 37 of the multiplex stage 36 are enabled correspondingly longer than the relevant switching elements 54 or 55 of the multiplex stage 53.

The AND gate 73 has a third input connected to a delay circuit consisting of a capacitor 79 and a resistor 80. The time constant of the delay components 79, 80 is selected in such manner that the positive potential at the gate 73 only occurs after the oscillator 70 has reached its nominal frequency after having been switched on.

From the output of AND gate 73 a connection leads by way of a resistor 81 to the base of a transistor 82, the emitter of which is connected to the base of a transistor 83, connected as an emitter follower. An emitter resistor is shown at reference 84. The collector of transistor 83 is connected to the infra-

red emitting diode 2.

In sequence with the Q 4 pulses of counter 71, the diode 2 is energised with a pulse having a period equal to the period of the pulses provided by the oscillator 70.

From output Q 4 of counter 71 a connection leads by way of a delay stage consisting of a resistor 85 and a capacitor 86, to an inverter 87 with its output connected to an AND-gate 88. The other input of the AND gate 88 is connected directly to the Q 4 output of counter 71. The output of the AND gate 88 is connected to one input of each of two AND-gates 89 and 90. The other input of AND-gate 89 is connected to the output of AND-gate 76 and the other input of AND gate 90 is connected to the output of AND gate 77. From the output of AND gate 89 a connection leads to the RESET input R of D-flip-flop 56, whereas the output of the AND gate 90 is connected to the RESET input R of D-flip-flop 57. By means of AND-gates 89 and 90 the re-setting is ensured for the D-flip-flop 56 or 57. The CLOCK inputs are connected respectively to the outputs of switching elements 54 and 55 of the second multiplex stage 53. The reset pulse duration for both D-flip-flops 56 and 57 is determined by the time constant of the delay circuit 85, 86. The switching elements 54 and 55 of the multiplex stage 53 are periodically and alternately enabled for the period of the pulses at output Q 4 of counter 71. During this period a signal from receiving diode 7 may reach D-flip-flop 57 and from receiving diode 8 may reach D-flip-flop 56 by way of switching element 54 and 55. The memory status of both D-flip-flops 57 and 56 is checked at the beginning of each pulse at output Q 4 of counter 71 by the application of the control potential to the RESET input R of the D-flip-flop connected with the appropriate switching element of the second multiplex stage 53. In the event of focus, when both receiving diodes 7 and 8 are equally influenced by radiation produced by diode 2, both transistors 64 and 60 receive a base current so that both light emitting diodes 68 and 66 are energized and so indicate that the lens is properly focussed. The example shown in Fig. 3 is generally similar to the example shown in Fig. 2 and like components bear the same references. Instead of diodes 66, 68, resistors 67 and 69, and transistors 60 and 64, a motor control circuit is included. The motor control circuit comprises a first transistor 91, the emitter of which is connected to the emitter of a second transistor 92. Both emitters are also connected to one terminal of a DC motor 93, the other terminal of which is connected to the earth. The collector of transistor 91 is connected to the positive terminal of battery 12 and the collector of transistor 92 is connected to the negative terminal of battery 12. The base of transistor 91 is connected to the

output OR-gate 62 and the base of transistor 92 is connected to the base of a NOR-gate 94, which is used in place of OR-gate 58.

The motor 93 operates the camera lens and also the lens 9 shown in Fig. 1 and rotates to the left or right until both diodes 7 and 8 are equally influenced by radiation emitted by the diode 2. When this condition is reached, the camera lens is in focus and the motor 93 is de-energized.

CLAIMS

1. A focussing system for a photographic or a cinematographic camera comprising a radiation emitting element for producing a measuring beam, radiation receiving elements positioned adjacent to each other and arranged to receive radiation produced by the radiation emitting element, an output stage, a lens positioned in front of the radiation receiving elements, the radiation receiving elements and the lens being movable relative to each other, a control circuit for energizing the radiation emitting element, during each cycle of the control circuit the radiation emitting element being energized for a predetermined duration by pulses having a predetermined frequency, and first and second multiplex stages, each multiplex stage having controllable switching elements and the switching elements of each multiplex stage being successively enabled during successive cycles of the control circuit, the input of each switching element of the first multiplex stage being responsive to an associated one of the radiation receiving elements and the output of each switching element of the second multiplex stage being connected to an associated memory element, the memory elements being connected to the output stage, and signal processing stages being provided between the commonly connected output of the first multiplex stage and the commonly connected input of the second multiplex stage.
2. A system as claimed in Claim 1 in which there are two radiation receiving elements and in which a convex lens is provided in front of the radiation receiving elements for concentrating the radiation received from the radiation emitting element into an area which is small relative to the area of the radiation receiving elements.
3. A system as claimed in Claim 1 or Claim 2 in which the radiation receiving elements comprise infra-red sensitive diodes, each diode being connected to the inverting input of a differential amplifier, the non-inverting input of which is connected to earth, and each differential amplifier being arranged so that the amplification factor for DC input components does not exceed a predetermined value and the amplification factor for AC input components increases with frequency.
4. A system as claimed in Claim 3 in which the differential amplifiers comprise op-



red emitting diode 2.

In sequence with the Q 4 pulses of counter 71, the diode 2 is energised with a pulse having a period equal to the period of the

5 pulses provided by the oscillator 70.

From output Q 4 of counter 71 a connection leads by way of a delay stage consisting of a resistor 85 and a capacitor 86, to an inverter 87 with its output connected to an
10 AND-gate 88. The other input of the AND gate 88 is connected directly to the Q 4 output of counter 71. The output of the AND gate 88 is connected to one input of each of two AND-gates 89 and 90. The other input of
15 AND-gate 89 is connected to the output of AND-gate 76 and the other input of AND gate 90 is connected to the output of AND gate 77. From the output of AND gate 89 a connection leads to the RESET input R of D-flip-flop 56, whereas the output of the AND
20 gate 90 is connected to the RESET input R of D-flip-flop 57. By means of AND-gates 89 and 90 the re-setting is ensured for the D-flip-flop 56 or 57. The CLOCK inputs are connected
25 respectively to the outputs of switching elements 54 and 55 of the second multiplex stage 53. The reset pulse duration for both D-flip-flops 56 and 57 is determined by the time constant of the delay circuit 85, 86. The
30 switching elements 54 and 55 of the multiplex stage 53 are periodically and alternately enabled for the period of the pulses at output Q 4 of counter 71. During this period a signal from receiving diode 7 may reach D-flip-flop
35 57 and from receiving diode 8 may reach D-flip-flop 56 by way of switching element 54 and 55. The memory status of both D-flip-flops 57 and 56 is checked at the beginning of each pulse at output Q 4 of counter 71 by
40 the application of the control potential to the RESET input R of the D-flip-flop connected with the appropriate switching element of the second multiplex stage 53. In the event of focus, when both receiving diodes 7 and 8
45 are equally influenced by radiation produced by diode 2, both transistors 64 and 60 receive a base current so that both light emitting diodes 68 and 66 are energized and so indicate that the lens is properly focussed.

50 The example shown in Fig. 3 is generally similar to the example shown in Fig. 2 and like components bear the same references. Instead of diodes 66, 68, resistors 67 and 69, and transistors 60 and 64, a motor control
55 circuit is included. The motor control circuit comprises a first transistor 91, the emitter of which is connected to the emitter of a second transistor 92. Both emitters are also connected to one terminal of a DC motor 93, the
60 other terminal of which is connected to the earth. The collector of transmitter 91 is connected to the positive terminal of battery 12 and the collector of transistor 92 is connected to the negative terminal of battery 12. The
65 base of transistor 91 is connected to the

output OR-gate 62 and the base of transistor 92 is connected to the base of a NOR-gate 94, which is used in place of OR-gate 58.

The motor 93 operates the camera lens and
70 also the lens 9 shown in Fig. 1 and rotates to the left or right until both diodes 7 and 8 are equally influenced by radiation emitted by the diode 2. When this condition is reached, the camera lens is in focus and the motor 93 is
75 de-energized.

CLAIMS

1. A focussing system for a photographic or a cinematographic camera comprising a
80 radiation emitting element for producing a measuring beam, radiation receiving elements positioned adjacent to each other and arranged to receive radiation produced by the radiation emitting element, an output stage, a
85 lens positioned in front of the radiation receiving elements, the radiation receiving elements and the lens being movable relative to each other, a control circuit for energizing the radiation emitting element, during each cycle of
90 the control circuit the radiation emitting element being energized for a predetermined duration by pulses having a predetermined frequency, and first and second multiplex
95 stages, each multiplex stage having controllable switching elements and the switching elements of each multiplex stage being successively enabled during successive cycles of the control circuit, the input of each switching
100 element of the first multiplex stage being responsive to an associated one of the radiation receiving elements and the output of each switching element of the second multiplex
105 stage being connected to an associated memory element, the memory elements being connected to the output stage, and signal processing stages being provided between the commonly connected output of the first multiplex stage and the commonly connected input of the second multiplex stage.

110 2. A system as claimed in Claim 1 in which there are two radiation receiving elements and in which a convex lens is provided in front of the radiation receiving elements for concentrating the radiation received from the
115 radiation emitting element into an area which is small relative to the area of the radiation receiving elements.

3. A system as claimed in Claim 1 or Claim 2 in which the radiation receiving elements comprise infra-red sensitive diodes,
120 each diode being connected to the inverting input of a differential amplifier, the non-inverting input of which is connected to earth, and each differential amplifier being arranged so
125 that the amplification factor for DC input components does not exceed a predetermined value and the amplification factor for AC input components increases with frequency.

4. A system as claimed in Claim 3 in
130 which the differential amplifiers comprise op-

erational amplifiers, the output of each amplifier being connected to its inverting input through a chain of high value linear resistors, and a tapping of the chain being connected to earth through a capacitor.

5 A system as claimed in Claim 3 or Claim 4 in which the output of each differential amplifier is connected to the input of an AC amplifier, the output of which is connected to the input of an associated one of the switching elements of the first multiplex stage.

6 A system as claimed in any one of the preceding claims, in which the control circuit comprises an oscillator and a counter operating as a frequency divider, the last output of the counter either alone or in combination with one of the other outputs providing a resetting signal for the counter, the last output being connected to the input of a first gate, another input of which is connected to the oscillator, and the radiation emitting device being controlled by the first gate.

7 A system as claimed in Claim 6, in which a second gate is positioned between the oscillator and the first gate, the second gate having one input connected to the oscillator, another input connected to one of the other outputs of the counter, and its output connected to the first gate.

8 A system as claimed in Claim 6 or Claim 7 in which the first gate has a further input connected to a delay circuit, the delay circuit providing a signal for disabling the first gate for a predetermined period after the system is energized.

9 A system as claimed in any one of Claims 6 to 8 in which the counter comprises an n-bit counter, the n-th output and one of the other outputs being connected to the inputs of an AND-gate, the output of which provides said resetting signal.

10 A system as claimed in any one of Claims 6 to 9 in which the last output of the counter is connected to the CLOCK input of a first bistable element, and the last but one output of the counter is connected to the CLOCK input of a second bistable element, the second bistable element being arranged so that its output signals are inverted each time a pulse appears at its CLOCK input, and in which the system further includes a gate-stage, the outputs of which are connected to the control inputs of the second multiplex stage, one set of inputs of which are connected to the outputs of the second bistable element, and the other set of inputs of which are connected to the output of the first bistable element.

11 A system as claimed in Claim 10 in which the second bistable element comprises a D-flip-flop having a Q and a $\bar{Q}$ output, the $\bar{Q}$ -output being connected to the D-input thereof.

12 A system as claimed in Claim 11 in

which the gate-stage comprises two AND-gates and the first bistable element comprises a D-flip-flop having a Q-output, one input of each of the AND-gates being connected to the Q-output of the first bistable element flip-flop and the other inputs of the AND-gates being connected respectively to the Q and the $\bar{Q}$ outputs of the second bistable element flip-flop.

13 A system as claimed in Claim 10 further including a third gate and a fourth gate, the last output of the counter being connected through a second delay circuit to one input of each of the third and fourth gates, the other inputs of the third and fourth gates being connected to the outputs of the gate stage, and in which there are two memory elements each comprising a D-flip-flop, the outputs of the third and fourth gates being connected respectively to the RESET inputs of the memory element flip-flops.

14 A system as claimed in any one of the preceding claims, in which the memory elements are connected to the output stage through a logic circuit, the arrangement being such that the output stage produces a focussing signal in the absence of radiation from the radiation emitting element being received by the radiation receiving elements, the focussing signal being cancelled when the camera lens is focussed at infinity by a switch associated with the camera lens focussing mechanism.

15 A system as claimed in Claim 14 in which there are two memory elements each comprising a D-flip-flop, and in which the system includes a fifth gate and a sixth gate, one input of the fifth gate being connected to the Q-output of one of the memory element flip-flops and the other input being connected to the $\bar{Q}$ -output of the other memory element flip-flop, one input of the sixth gate being connected to the Q-output of said other memory element flip-flop and the other input being connected to a current source through said switch associated with camera lens focussing mechanism, the switch being closed when the camera is focussed at infinity and the outputs of the fifth and sixth gates being connected to the output stage.

16 A focussing system as claimed in Claim 15 in which the fifth and sixth gates comprise OR-gates.

17 A focussing system for a cinematographic or a photographic camera substantially as hereinbefore described with reference to and as shown in Figs. 1 and 2 or Figs. 1 and 3 of the accompanying drawings.