Description

The present invention relates to a circuit for amplifying signals produced by a magnetoresistive (MR) element, and more particularly to a circuit which has low noise and yet protects the MR element from large undesirable currents resultant from electrical short circuits between the MR element and its surrounding environment, such as a magnetic recording disk, or similarly conductive surface.

MR elements or heads can read data from a magnetic surface at high linear densities. An MR head detects magnetic field signals through resistance changes which are a function of the magnitude and direction of the magnetic flux sensed by the head.

US patent 4,706,138 discloses a current biased, current sensing amplifier that biases and amplifies the signals produced by an MR element. The amplifier senses a current signal derived from the MR element which corresponds to dRh/Rh, where Rh is the resistance of the MR element and dRh is the magnetic-signal-induced change or delta in MR element resistance. This amplifier provides no short circuit protection and does not include means to maintain the MR element at a prescribed voltage (e.g., with reference to ground). It also employs so-called "bang-bang" feedback control and inputs a fixed signal approximating minimum offset error instead of changing the gain and linear response of the feedback loop.

US patent 4,879,610 discloses an amplifier for biasing and amplifying the signals produced by a MR element. The amplifier amplifies a current signal derived from the MR element which corresponds solely to dRh, where dRh (as in USP 4,706,138) is the magnetic-signal-induced change in MR element resistance. This amplifier provides short circuit protection and is very suitable for use in applications involving high data rates provided the signal amplitude is relatively large. However, this amplifier provides an output with a relatively low signal-to-noise ratio. Signal-to-noise ratio becomes an increasingly serious problem in view of the trend in magnetic recording to continually increase track density and reduce signal amplitude.

US patent 4,743,861 discloses a frequency compensation circuit adapted to increase high frequency bandwidth when data rate is high, and under certain circumstances, when input lead inductance is high and input loop resistance is low.

None of these references or any other prior art known to applicants provides both short circuit protection and low noise. There is a need for a circuit that has (a) low noise to enable use in applications involving low amplitude input signals, (b) provides short circuit protection between the MR element and its environment, and (c) also varies the gain and frequency response of a feedback loop to enable faster switching between a plurality of MR elements.

In accordance with the present invention, there is now provided an amplifier circuit for amplifying an input signal (Vin) generated by a magnetoresistive (MR) element (Rmr) to produce an output signal having a magnitude substantially proportional to dRh/Rh, where Rh is the resistance of the MR element (Rmr) and dRh is the magneto-signal-induced change in the resistance of the MR element (Rmr), the circuit comprising: an MR element (Rmr); a current source for coupling to the MR element (Rmr) to produce a bias current in the MR element (Rmr); characterised in that the circuit further comprises: first and second interconnected feedback loops, the first feedback loop amplifying the input signal (Vin) in the form of deviations from the bias current in such a manner that any DC offset error is minimised, the second feedback loop providing short circuit protection of the MR element (Rmr) by maintaining the MR element (Rmr) in the event of a short circuit between the MR element (Rmr) and an adjacent conductive surface.

Viewing the present invention from a second aspect there is now provided a circuit for simultaneously producing electrical output signals whose magnitude is representative of signals produced by a magnetoresistive (MR) element and protecting said MR element from electrical short circuits between said element and its environment said circuit comprising: means including a first feedback loop for biasing the MR element with a bias current and amplifying a signal current for causing the MR element to produce a circuit output signal corresponding to dRh/Rh, a second feedback loop for insuring that the MR element is held at at a preselected reference potential and concurrently insuring that no current will flow sufficient to damage the MR element in event of a short circuit between the MR element and its environment.

Viewing the present invention from a third aspect, there is now provided a circuit for simultaneously producing electrical output signals whose magnitude is representative of signals produced by a magnetoresistive (MR) element and protecting said MR element from electrical short circuits between said element and its environment, said circuit comprising: an MR element; means including a first feedback loop for biasing the MR element with a bias current and amplifying a signal current for causing the MR element to produce a circuit output signal corresponding to dRh/Rh and in which any dc offset error is minimized; and a second feedback loop for insuring that the MR element is held at a preselected reference potential and concurrently insuring that no current will flow sufficient to damage the MR element in event of a short circuit between the MR element and its environment.

Viewing the present invention from a fourth aspect, there is now provided a circuit for simultaneously producing electrical output signals whose magnitude is representative of signals produced by a mag-

netoresistive (MR) element and protecting said MR element from electrical short circuits between said element and its environment, said circuit comprising: an MR element having a first and a second terminal; a current source coupled to said first terminal for producing a bias current through said MR element; an input stage having at least one pair of bipolar transistors and also having two output terminals, both said terminals of said MR element being coupled to the emitters of said transistors of each pair for amplifying current deviations from the bias current; first feedback circuit means coupled to the collectors of said transistors of each pair to sense any offset between said output terminals of said input stage to produce a control signal, said control signal being coupled to the bases of said transistors of each pair to substantially eliminate any offset potential between said output terminals; circuit means coupled across said terminals of said MR element for sensing a centre potential of said element substantially midway between said terminals; second feedback circuit means responsive to the difference between the sensed centre potential of said MR element and a predetermined reference potential to produce a control signal; and means responsive to said control signal to apply a bias signal to the bases of said transistors to maintain said centre potential of said MR element substantially at said predetermined reference potential, while concurrently insuring that substantially no current will flow through any accidental short circuit between any point along said MR element and its environment.

In a preferred example of the preset invention, there is provided an amplifier circuit for simultaneously producing electrical output signals whose magnitude is representative of signals produced by a magnetoresistive (MR) element and protecting said MR element from electrical short circuits between said element and its environment. A means including a first feedback loop biases the MR element with a bias current and amplifies a signal current for causing the MR element to produce a circuit output signal corresponding to dRh/Rh and in which any dc offset error is minimized. A second feedback loop insures that the MR element is held at a preselected reference potential and concurrently insures that no current will flow sufficient to damage the element in event of a short circuit between the element and its environment. The feedback loops are interconnected by outputs of the respective feedback loops being commonly connected to the bases of a pair of input bipolar transistors, whose respective emitters are connected to opposite terminals of the MR element.

Each feedback loop comprises an operational transconductance amplifier (OTA) for converting an error voltage to a control current output. The OTA for the first feedback loop provides a differential control current output for adjusting the potential between the bases of the input transistors to insure that a reference current will be divided equally between each input transistor of the pair for maintaining the MR element biased at a prescribed bias current. The OTA for the second feedback loop provides currents of substantially equal magnitude to the base of each bipolar input transistor of the pair to provide respective emitter currents whose sum is substantially equal to a predetermined reference current.

An embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a schematic diagram illustrating the basic concept of a circuit of the present invention;

Fig. 2 is a circuit diagram of a preferred embodiment of low noise amplifier circuit of the present invention; and

Fig. 3 is a plot of short circuit current vs. time, depicting a short circuit current as a function of circuit topology and input-transistor base parasitic capacitance.

As illustrated in simplified form in Fig. 1, the low noise amplifier circuit embodying the invention provides short circuit protection for a magnetoresistive (MR) element Rmr, such as an MR head in a magnetic disk file. Bipolar NPN transistors Q1 and Q2 are the input devices to the amplifier. These transistors, together with a capacitor C1 and a resistor R1 interposed in parallel between said transistors, constitute an input stage 10 to the amplifier circuit. A biasing current Iref is fixed at a value equal to twice the value of current needed to bias MR element Rmr.

According to the feature of the invention, the amplifier circuit has two feedback loops which are interconnected by virtue of their outputs being commonly connected to the respective bases of transistors Q1 and Q2.

One loop is a common mode feedback loop comprising resistors R3, R4 and R7, and an operational transconductance amplifier (OTA) g1 for which a resistor R2 and capacitor C2 in parallel combination determine the dominant time constant of this loop. The purpose of this loop is to control the common mode voltage at the bases of input transistors Q1 and Q2, in such manner that the dc potential at the electrical centre of the MR element Rmr will be maintained equal to a reference voltage Vref. Usually, and as illustrated, Vref is made ground.

The other loop is a differential feedback loop comprising an OTA g2, resistors R5, R6 and R1, and a capacitor C1. The purpose of this loop is to insure that the emitter currents through both input devices are equal; that is, equal to Iref/2. Capacitor C1 and resistor R1 are connected in parallel combination to determine the dominant time constant in this other loop.

Assuming an MR element of steady-state resistance Rh is used, and that the bias current Iref/2 = Ib, then a bias voltage defined as :

$$Vb = Ib\ Rh]$$

will exist across the MR element, and is constant in value across the frequency band of interest. Resistance Rh is made up of a fixed resistance Rh and dRh, the magnetic-signal-induced change in resistance of the MR element; and the current through Rh is made up of a constant time-averaged value of bias current I and a variable signal current dI.

Taking the derivative with respect to time of both sides of Equation (1) above, the following equation is derived after manipulation:

$$dI = (- I\,dRh) / Rh$$

If the collector resistors (R5 and R6) of the amplifier in Fig. 1 are defined as Rc, then the expression for Vout becomes

$$Vout = (2\,Rc\,I\,dRh) / Rh$$

which is of the form K dRh/Rh. So, the amplifier produces an output signal corresponding to dRh/Rh.

In Fig. 2, which depicts in more detail an amplifier circuit according to a preferred embodiment of the invention, similar reference characters are used to identify similar components. OTA g1 comprises a current source Jff3, transistors Q12 and Q11 and resistors R8 and R9. OTA g1 produces a current proportional to the difference in potential between Vref (ground, as illustrated) and the electrical centre of the MR element Rmr at the junction of resistors R4, R3 and R7. At the collector of transistor Q11, this differential current is converted to a control reference voltage across capacitor C2. Diode Q13 is preferably provided for temperature stability. As in Fig. 1, capacitor C2 in parallel with resistor R2 primarily determines the dominant time constant in this loop, and also effectively eliminates noise at the output of OTA g1.

The control reference voltage generated across capacitor C2 is converted to two currents of equal magnitude by the transistor/resistor pairs Q14,R11 and Q15,R12. These equal magnitude currents are the base currents needed by the two input transistors Q1 and Q2. These base currents, when multiplied by the current gain of the input transistors Q1 and Q2, result in the respective emitter currents needed in said transistors to satisfy the requirements of current source J1. When the sum of these emitter currents is equal to the bias current Iref, as provided by source J1, and this requirement is thus satisfied, no current will flow to Vref (ground, as illustrated) through resistor R7 and the voltage at the electrical centre of the MR element Rmr will be at the potential of Vref (ground, as illustrated).

The other feedback loop is necessary to insure that in addition to having the electrical centre of MR element Rmr at a preselected potential, the dc offset at Vout is small. This is necessary because a large dc voltage will exist at Vin due to the effect of the large dc bias current through MR element Rmr. This large dc voltage is not desirable at Vout because it contains no information. Only the small ac signal at Vin is desired to be amplified at Vout as a data signal for later detection.

For this reason, this other loop, which is a differential feedback loop, is connected between Vout and the bases of the input transistors Q1 and Q2. First, the signal at Vout is level shifted via emitter followers Q16 and Q17 and level shifting series diodes D1n and D2n; each n denoting a plurality of diodes in series. Biasing for these level shifters is supplied by current sources J4 and J5.

The Vout terminals of the amplifier circuit are preferably connected to input terminals of a buffer/amplifier 11 to buffer and further amplify the circuit output signal from Vout in order to increase the bandwidth and level of said output signal, respectively, at the buffer/amplifier output.

OTA g2 comprises transistors Q3, Q4, Q5, Q6, Q7, Q8, Q9 and Q10, and current source J2. OTA g2 converts the voltage at Vout to a current between the two outputs of the OTA, thereby creating a voltage drop across resistor R1 to control the dc voltage at Vout sbstantially at zero. If the loop gain is high, the dc voltage across resistor R1 will equal the voltage across MR element Rmr. Both input transistors Q1 and Q2 will then have equal biasing current (i.e., R5a,b = R6a,b), so that MR element Rmr will have one half the value of J1 as a bias current. Capacitor C1 across resistor R1 creates the dominant zero in this differential feedback loop, and when modified by the loop gain, creates a dominant pole in the forward transfer function from Vin to Vout.

According to a feature of the invention, by inserting capacitor C1 between the bases of the input transistors Q1 and Q2, differential noise in the loop is eliminated.

According to other features of the invention, differential feedforward currents Jff1 and Jff2 are assumed to be substantially equal. They are applied to the bases of transistors Q1 and Q2, respectively, and develop a voltage across resistor R1 which is substantially equal to the statistically nominal voltage needed across MR element Rmr to minimize the dc offset at Vout and insure that the correct bias current Iref is applied through said MR element. Also, a common-mode third feedforward current Jff3 is applied between resistors R8,R9 and -V. It is adjusted such that the potential at the electrical centre of MR element Rmr will be precisely equal to Vref under statistically nominal conditions.

The term "statistically nominal conditions" is intended to connote that the process parameters of all transistors and resistors are at their mean values, and the term "statically nominal voltage" signifies the voltage developed across an MR element of mean resistance when a mean bias current Iref is applied through said element.

The noise of an amplifier of the present invention is low compared to amplifiers heretofore disclosed to provide short circuit protection for signals from MR

elements. The lower noise is achieved by providing only one biasing current source (Iref) for the both MR element Rmr and input stage 10. By eliminating additional biasing stages or reference resistors, noise desirably is reduced in the order of several dB.

The equations and proofs relating to gain, frequency response and short circuit protection are set out below.

Assume that transconductance amplifier g2 does not exhibit an output offset current and that feedforward currents Jff1 and Jff2 result, which are substantially equal, in an ideal compensation (that is, Jff1 ≈ {Rmr | | (R3 + R4)} J1/2R1). Under this assumed condition, the voltage Vcm at the centre of the MR element Rmr relative to Vref (ground) is given by

$$Vcm = (Jff3 - \frac{J1R11)}{\beta R2}\frac{(R8+R9}{2} + 2\frac{Vt}{Jff3}) \quad (1)$$

where

Vcm = actual voltage at centre of MR head element
R3 = R4
R8 = R9
R11 = R12
β = current gain of NPN devices
Vt = 2 6 mV. (the thermal voltage)

The initial short circuit (Isib) from the most negative terminal of MR head element Rmr to ground (Vref) at time = 0+ is given by

$$Isib = -\frac{RmrR3}{(Rmr+2R3)(R3+R7)}\frac{J1}{}. \quad (2)$$

In the event of a short circuit between the most positive terminal of MR head element Rmr and ground (Vref), the current (Isit) through the short circuit is initially

$$Isit = -Isib. \quad (3)$$

The short circuit current from the most negative terminal of MR head element Rmr to ground (Vref) will slowly increase to a final value (Isfb) at time = ∞, given by

$$Isfb = \frac{Bg'R'Jff3-\varepsilon Jff1}{1+g'R'} - J1, \quad (4)$$

with

$$g' = \frac{1}{1+2g2\beta RL}\frac{2\beta}{R1} + \frac{2}{Rmr} + \frac{1}{R3},$$

$$R' = \frac{2R7+R3}{1+2g1\beta R7},$$

$$\varepsilon = \frac{2\beta}{1+2g2\beta RL},$$

$$g1 = \frac{R2}{R11(R8+R9+\frac{2Vt}{Jff3})}$$

$$g2 = \frac{J2}{4Vt}$$

$$R3 = R4$$

and

$$R5a = R6a = RL.$$

If it is assumed βg'R'<<1, ε<<1, and Isfb≈-J1, then the final short circuit current (Isft) from most positive terminal of head element Rmr to ground is given by

$$Isft = \frac{\beta g'R'Jff3+\varepsilon Jff1}{1+g'R'} + \frac{1-g'R'}{1+g'R'}J1. \quad (5)$$

As a result of the above assumptions, Isft≈J1.

Acknowledging that parasitic capacitances C' exist between the bases of the bipolar input transistors (like Q1 and Q2) and ground (Vref) or a substrate, such as a magnetic recording disk, the stored charge is nearly instantaneously discharged during a shorting event from MR element Rmr to the environment. The energy dissipated by the MR element Rmr during such an event is approximated by the expression

$$E = 0.5\beta C'V^2 \quad (6)$$

where V^2 is the square of the voltage difference between ground (Vref) and the sum of Vcm and one half the bias current (Iref/2) multiplied by the resistance of MR element Rmr.

The transfer function Vout/Vin has a high-pass frequency characteristic with a -3 dB frequency given by

$$f-3dBlow = \frac{1+g2R1\frac{R5a+R6a}{Rmr+2re}}{2\pi\tau 1} \quad (7)$$

and a gain in the frequence band of interest of

$$G = \frac{R5+R6}{Rmr+2re} \quad (8)$$

where

R5 = R5a + R5b,
R6 = R6a + R6b,
τ1 = R1C1,
g2 = J2/4Vt, and
re = 2Vt/J1.

The high frequency bandwidth of the circuit may be limited by the inductance of the leads from the MR element Rmr to the input devices together with the low input resistance of the amplifier if the input device transition frequency ft is sufficiently high. The expression for the high frequency bandwidth of the amplifier then becomes

$$f-3dBhigh = \frac{Ri}{2\pi Li} \quad (9)$$

where

Li = differential series inductance of leads from MR element to amplifier, and
Ri = sum of the resistances in the input loop of the amplifier

$$Ri = Rmr + 2re + (2rbb'/\beta)$$

where rbb' is the base spreading resistance associated with each input transistor.

Fig. 3 plots short circuit current vs. time and depicts the effect of such parasitic capacitance C'. Assume that at time t0 a short occurs. Instead of the value of initial short circuit current indicated by Equations (2) or (3) for either Isib or Isit, which is indicated

as A, a larger current due to the parasitic capacitance C' occurs. Capacitance C' is to the sum of those parasitic capacitances associated with the base circuit of the input transistors Q1 and Q2. The dashed line A-B indicates what the short circuit profile of the circuit would be without parasitic capacitance. Therefore, the area under the actual short circuit current profile above the dashed line A-B represents the energy approximated in Equation (6); and the total energy dissipated by MR element Rmr is represented by the total area under that profile between the onset and cessation of a short circuit. The short circuit current profile beyond point B is, in the absence of any nonlinear slew rate limitations caused by a the size of capacitor C2 and current Jff3, an exponentially shaped curve with a time constant governed by C2 and its parallel resistance R2 modified by the appropriate gain of what was earlier described as the common mode feedback loop.

The curve depicted in Fig.3 will increase with time until the final value of short circuit current previously defined in Equation (5) is attained. The time needed from initial to final value of short circuit current is then linearly calculated from the resultant time constant. In the event of slew rate limitation of the common mode feedback loop feedforward current Jff3 and capacitance C2, the time needed from initial to final value of short circuit current is calculated in much the same way as in the above cited U.S. patent 4,879,610, and will be longer than that value which is linearly calculated.

It will be understood by those skilled in the art that changes in form and detail may be made in the embodiments of amplifier circuit herein described without departing from the scope and teaching of the invention. Accordingly, the low noise amplifier circuit and method herein disclosed are to be considered merely as illustrative, and the invention is to be limited only as specified in the claims.

Claims

1. An amplifier circuit for amplifying an input signal (Vin) generated by a magnetoresistive (MR) element (Rmr) to produce an output signal having a magnitude substantially proportional to dRh/Rh, where Rh is the resistance of the MR element (Rmr) and dRh is the magneto-signal-induced change in the resistance of the MR element (Rmr), the circuit comprising:

   an MR element (Rmr);

   a current source (J1) coupled to the MR element (Rmr) to produce a bias current in the MR element (Rmr);

   characterised in that the circuit further comprises:

   first and second interconnected feedback loops,

   the first feedback loop for amplifying the input signal (Vin) in the form of deviations from the bias current in such a manner that any DC offset error in the output signal is minimised,

   the second feedback loop providing short circuit protection of the MR element (Rmr) by maintaining the MR element (Rmr) at a reference potential to limit current flow through the MR element (Rmr) in the event of a short circuit between the MR element (Rmr) and an adjacent conductive surface.

2. A circuit as claimed in claim 1 wherein, in use, the feedback loops cooperate to increase the short circuit protection as the bias current decreases and to decrease the short circuit protection as the bias current increases.

3. A circuit as claimed in claim 2 comprising an input stage (10) having a pair of bipolar transistors (Q1,Q2), the collectors of the transistors (Q1,Q2) forming output terminals of the input stage (10), the emitters of the transistors (Q1,Q2) being connected to opposite terminals of the MR element (Rmr) for amplifying the input signal, the feedback loops having outputs commonly connected to the bases of the transistors (Q1,Q2).

4. A circuit as claimed in claim 3, wherein the first feedback loop is connected to the collectors of the transistors (Q1,Q2) to generate a first control signal in response to any offset potential between the output terminals of the input stage (10), the first control signal being coupled to the bases of the transistors (Q1,Q2) to substantially eliminate any offset potential between the output terminals.

5. A circuit as claimed in claim 4 wherein the first control signal is in the form of a differential current signal for adjusting the potential between the bases of the transistors (Q1,Q2) in such a manner that a reference current is divided substantially equally between the transistors (Q1,Q2) to produce the bias current.

6. A circuit as claimed in claim 5, wherein the first feedback loop comprises an impendance derived from a resistor (R1) and a capacitor (C1) interposed in parallel between the transistors (Q1,Q2) for defining the frequency response of the circuit in such a manner that the circuit has a dominant zero frequency below a dominant pole frequency to provide a high pass characteristic, the capacitor (C1) serving, to shunt noise generated by the resistor (R1).

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as A, a larger current due to the parasitic capacitance C' occurs. Capacitance C' is to the sum of those parasitic capacitances associated with the base circuit of the input transistors Q1 and Q2. The dashed line A-B indicates what the short circuit profile of the circuit would be without parasitic capacitance. Therefore, the area under the actual short circuit current profile above the dashed line A-B represents the energy approximated in Equation (6); and the total energy dissipated by MR element Rmr is represented by the total area under that profile between the onset and cessation of a short circuit. The short circuit current profile beyond point B is, in the absence of any nonlinear slew rate limitations caused by a the size of capacitor C2 and current Jff3, an exponentially shaped curve with a time constant governed by C2 and its parallel resistance R2 modified by the appropriate gain of what was earlier described as the common mode feedback loop.

The curve depicted in Fig.3 will increase with time until the final value of short circuit current previously defined in Equation (5) is attained. The time needed from initial to final value of short circuit current is then linearly calculated from the resultant time constant. In the event of slew rate limitation of the common mode feedback loop feedforward current Jff3 and capacitance C2, the time needed from initial to final value of short circuit current is calculated in much the same way as in the above cited U.S. patent 4,879,610, and will be longer than that value which is linearly calculated.

It will be understood by those skilled in the art that changes in form and detail may be made in the embodiments of amplifier circuit herein described without departing from the scope and teaching of the invention. Accordingly, the low noise amplifier circuit and method herein disclosed are to be considered merely as illustrative, and the invention is to be limited only as specified in the claims.

Claims

1. An amplifier circuit for amplifying an input signal (Vin) generated by a magnetoresistive (MR) element (Rmr) to produce an output signal having a magnitude substantially proportional to dRh/Rh, where Rh is the resistance of the MR element (Rmr) and dRh is the magneto-signal-induced change in the resistance of the MR element (Rmr), the circuit comprising:

   an MR element (Rmr);

   a current source (J1) coupled to the MR element (Rmr) to produce a bias current in the MR element (Rmr);

   characterised in that the circuit further comprises:

   first and second interconnected feedback loops,

   the first feedback loop for amplifying the input signal (Vin) in the form of deviations from the bias current in such a manner that any DC offset error in the output signal is minimised,

   the second feedback loop providing short circuit protection of the MR element (Rmr) by maintaining the MR element (Rmr) at a reference potential to limit current flow through the MR element (Rmr) in the event of a short circuit between the MR element (Rmr) and an adjacent conductive surface.

2. A circuit as claimed in claim 1 wherein, in use, the feedback loops cooperate to increase the short circuit protection as the bias current decreases and to decrease the short circuit protection as the bias current increases.

3. A circuit as claimed in claim 2 comprising an input stage (10) having a pair of bipolar transistors (Q1,Q2), the collectors of the transistors (Q1,Q2) forming output terminals of the input stage (10), the emitters of the transistors (Q1,Q2) being connected to opposite terminals of the MR element (Rmr) for amplifying the input signal, the feedback loops having outputs commonly connected to the bases of the transistors (Q1,Q2).

4. A circuit as claimed in claim 3, wherein the first feedback loop is connected to the collectors of the transistors (Q1,Q2) to generate a first control signal in response to any offset potential between the output terminals of the input stage (10), the first control signal being coupled to the bases of the transistors (Q1,Q2) to substantially eliminate any offset potential between the output terminals.

5. A circuit as claimed in claim 4 wherein the first control signal is in the form of a differential current signal for adjusting the potential between the bases of the transistors (Q1,Q2) in such a manner that a reference current is divided substantially equally between the transistors (Q1,Q2) to produce the bias current.

6. A circuit as claimed in claim 5, wherein the first feedback loop comprises an impendance derived from a resistor (R1) and a capacitor (C1) interposed in parallel between the transistors (Q1,Q2) for defining the frequency response of the circuit in such a manner that the circuit has a dominant zero frequency below a dominant pole frequency to provide a high pass characteristic, the capacitor (C1) serving, to shunt noise generated by the resistor (R1).

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7. A circuit as claimed in any one of claims 4,5, or 6 comprising:

first circuit means connected to the MR element (Rmr) to detect a centre potential substantially midway between the terminals of the MR element (Rmr), the second feedback loop being configured to generate a second control signal in response to a difference between the sensed centre potential and a predetermined reference potential; and

second circuit means responsive to the second control signal to apply bias signals to the bases of the transistors (Q1,Q2) to maintain the centre potential substantially at the reference potential.

8. A circuit as claimed in claim 6 wherein the bias signals are substantially equal currents for maintaining the sum of the emitter currents of the transistors (Q1,Q2) substantially equal to a reference current.

9. A circuit as claimed in any preceding claim wherein the second feedback loop comprises delay means (R2,C2) for delaying response of the circuit to a short circuit until the short circuit has ceased, the delay means comprising a resistor (R2) and a capacitor (C2) connected in parallel.

10. A circuit as claimed in any preceding claim wherein the first and second feedback loops comprise respective differential transconductance amplifiers (g1,g2) for converting an error voltage into a control current output.

11. A circuit as claimed in any preceding claim comprising a buffer amplifier (11) for amplifying the circuit output signal and for increasing the bandwidth of the circuit output signal.

12. A method of producing electrical output signals whose magnitude is representative of signals produced by a magnetoresistive (MR) element (Rmr) while concurrently protecting the MR element from electrical short circuits between the element and its environment, said method comprising the steps of:

coupling a current source (J1) to one of two terminals of an MR element (Rmr) for producing a bias current through the MR element;

providing an input stage (10) having at least two bipolar transistors (Q1,Q2) and output terminals;

coupling both terminals of said MR element (Rmr) to emitters of said transistors (Q1,Q2) for amplifying current deviations from a time average value of said bias current;

coupling a first feedback circuit means to collectors of said transistors (Q1,Q2) to sense the time average potential between said output terminals to produce a differential control signal, and coupling said differential control signal to bases of said transistors (Q1,Q2) to substantially eliminate the time average offset potential between said output terminals;

coupling other circuit means across both terminals of said MR element (Rmr) for sensing the centre potential of said MR element substantially midway between said both terminals;

using a second feedback circuit means, producing two substantially similar control signals in response to the difference between the sensed centre potential of the MR element (Rmr) and a predetermined reference potential; and

in response to said two similar control signals, applying bias signals to the bases of said transistors (Q1,Q2) to maintain said sensed centre potential substantially at said predetermined reference potential and concurrently insure that substantially no current will flow through any accidental short circuit between any point along said MR element (Rmr) and its said environment.

Patentansprüche

1. Gemäß der vorliegenden Erfindung wird nun eine Verstärkerschaltung zur Verstärkung eines Eingangssignals (Vin), das von einem magnetoresistiven (MR-Element) Element (Rmr) bereitgestellt wird und ein Ausgangssignal erzeugt, das proportional zu dRh/Rh ist, wobei Rh der Widerstand des MR-Elements (Rmr) und dRh die vom magnetischen Signal induzierte Änderung im Widerstand des MR-Elements (Rmr) ist, wobei die Schaltung folgendes umfaßt:
ein MR-Element (Rmr);
eine Stromquelle (J1) zur Kopplung an das MR-Element (Rmr) zur Erzeugung eines Vorbelastungsstroms im MR-Element (Rmr);
dadurch charakterisiert, daß die Schaltung des weiteren folgendes umfaßt:
eine erste und eine zweite Feedbackschleife, die miteinander verbunden sind,
wobei die erste Feedbackschleife das Eingangssignal (Vin) in Form von Abweichungen vom Vorbelastungsstrom verstärkt, so daß jeglicher Offset-Fehler des Gleichstroms auf ein Minimum reduziert wird,
wobei die zweite Feedbackschleife einen Kurzschlußschutz des MR-Elements (Rmr) bietet, indem sie das MR-Element (Rmr) auf einem Referenzpotential hält, um den Stromfluß durch das MR-Element (Rmr) im Fall eines Kurzschlusses zwischen dem MR-Element (Rmr) und einer benachbarten leitenden Oberfläche zu beschrän-

ken.

2. Eine Schaltung gemäß Anspruch 1, bei der, wenn sie in Verwendung ist, die Feedbackschleifen zusammenwirken, um den Kurzschlußschutz zu erhöhen, während der Vorbelastungsstrom sinkt, und um den Kurzschlußschutz zu verringern, während der Vorbelastungsstrom ansteigt.

3. Eine Schaltung gemäß Anspruch 2, die eine Eingangsstufe (10) aufweist, die ein Paar an bipolaren Transistoren (Q1, Q2) umfaßt, wobei die Kollektoren der Transistoren (Q1, Q2) Ausgangsanschlußstellen der Eingangsstufe (10) bilden, und wobei die Emitter der Transistoren (Q1, Q2) an unterschiedliche Anschlußstellen des MR-Elements (Rmr) angeschlossen sind, um das Eingangssignal zu verstärken, wobei die Feedbackschleifen Ausgänge aufweisen, die gemeinsam an die Basen der Transistoren (Q1, Q2) angeschlossen sind.

4. Eine Schaltung gemäß Anspruch 3, wobei die erste Feedbackschleife an die Kollektoren der Transistoren (Q1, Q2) angeschlossen ist und als Reaktion auf ein beliebiges Offsetpotential zwischen den Ausgangsanschlußstellen der Eingangsstufe (10) ein erstes Steuersignal erzeugt, wobei das erste Steuersignal an die Basen der Transistoren (Q1, Q2) gekoppelt ist, um ein beliebiges Offsetpotential zwischen den Ausgangsanschlußstellen im wesentlichen zu eliminieren.

5. Eine Schaltung gemäß Anspruch 4, bei der das erste Steuersignal in Form eines differentialen Stromsignals zur Einstellung des Potentials zwischen den Basen der Transistoren (Q1, Q2) vorliegt, so daß ein Referenzstrom unter den Transistoren (Q1, Q2) im wesentlichen zu gleichen Teilen aufgeteilt wird, um den Vorbelastungsstrom zu erzeugen.

6. Eine Schaltung gemäß Anspruch 5, bei der die erste Feedbackschleife eine Impedanz umfaßt, die von einem Widerstand (R1) und einem Kondensator (C1) abgeleitet ist, die parallel zwischen den Transistoren (Q1, Q2) angeordnet sind, um den Frequenzgang der Schaltung so zu definieren, daß die Schaltung die dominante Nullfrequenz unterhalb der dominanten Polfrequenz aufweist, um eine Hochpaßeigenschaft bereitzustellen, wobei der Kondensator (C1) dazu dient, die vom Widerstand (R1) erzeugten Geräusche abzuzweigen.

7. Eine Schaltung gemäß einem der Ansprüche 4, 5 oder 6, bestehend aus:
einem ersten Schaltmittel, das an das MR-Element (Rmr) angeschlossen ist, um ein Mittepotential aufzunehmen, das sich im wesentlichen in der Mitte zwischen den Anschlußstellen des MR-Elements (Rmr) befindet, wobei die zweite Feedbackschleife so konfiguriert ist, daß sie als Reaktion auf eine Differenz zwischen dem gemessenen Mittepotential und einem vorbestimmten Referenzpotential ein zweites Steuersignal erzeugt; und
einem zweiten Schaltmittel, das auf das zweite Steuersignal reagiert und an die Basen der Transistoren (Q1, Q2) Vorbelastungssignale anlegt, um das Mittepotential im wesentlichen auf dem Pegel des Referenzpotentials zu halten.

8. Eine Schaltung gemäß Anspruch 6, bei der die Vorbelastungssignale im wesentlichen gleiche Ströme sind, um die Summe der Emitterströme der Transistoren (Q1, Q2) im wesentlichen auf dem gleichen Pegel wie ein Referenzstrom zu halten.

9. Eine Schaltung gemäß jedem vorherigen Anspruch, bei der die zweite Feedbackschleife Verzögerungsmittel (R2, C2) umfaßt, um die Ansprechzeit der Schaltung bei einem Kurzschluß solange zu verzögern, bis der Kurzschlußzustand beendet ist, wobei das Verzögerungsmittel einen Widerstand (R2) und einen Kondensator (C2) umfaßt, die parallel angeschlossen sind.

10. Eine Schaltung gemäß jedem vorherigen Anspruch, bei der die erste und die zweite Feedbackschleife entsprechende differentiale Transkonduktanzverstärker (g1, g2) enthalten, um eine Fehlerspannung in einen Steuerstromausgang zu verwandeln.

11. Eine Schaltung gemäß jedem vorherigen Anspruch, die einen Pufferverstärker (11) zur Verstärkung des Schaltungsausgangssignals und zur Erhöhung der Bandbreite des Schaltungsausgangssignals enthält.

12. Ein Verfahren zur Erzeugung elektrischer Ausgangssignale, deren Größe repräsentativ ist für die durch ein magnetoresistives (MR) Element (Rmr) erzeugten Signale, während gleichzeitig das MR-Element (Rmr) vor elektrischen Kurzschlüssen zwischen dem Element und seiner Umgebung geschützt wird, wobei das Verfahren die folgenden Schritte umfaßt:
Kopplung einer Stromquelle (J1) an eine der beiden Anschlußstellen eines MR-Elements (Rmr) zur Erzeugung eines Vorbelastungsstroms durch das MR-Element;
Bereitstellung einer Eingangsstufe (10) mit mindestens zwei bipolaren Transistoren (Q1, Q2)

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und Ausgangsanschlußstellen;
Kopplung beider Anschlußstellen des genannten MR-Elements (Rmr) an Emitter der genannten Transistoren (Q1, Q2) zur Verstärkung von Abweichungen des Stroms von einem Zeitdurchschnittswert des genannten Vorbelastungsstroms;
Kopplung eines ersten Feedbackschaltungsmittels an Kollektoren der genannten Transistoren (Q1, Q2) zur Messung des Zeitdurchschnittspotentials zwischen den genannten Ausgangsanschlußstellen, um ein differentiales Steuersignal zu erzeugen, und Kopplung des genannten differentialen Steuersignals an die Basen der genannten Transistoren (Q1, Q2), um das Zeitdurchschnittsoffsetpotential zwischen den genannten Ausgangsanschlußstellen im wesentlichen zu eliminieren;
Kopplung anderer Schaltmittel an beide Anschlußstellen des genannten MR-Elements (Rmr) zur Aufnahme des Mittepotentials des genannten MR-Elements (Rmr) in die Mitte zwischen den beiden genannten Anschlußstellen;
Verwendung eines zweiten Feedbackschaltmittels, das zwei im wesentlichen ähnliche Steuersignale als Reaktion auf die Differenz zwischen dem aufgenommenen Mittepotential des MR-Elements (Rmr) und einem vorbestimmten Referenzpotential erzeugt; und
Anlegen von Vorbelastungssignalen als Reaktion auf die beiden genannten ähnlichen Steuersignale an die Basen der genannten Transistoren (Q1, Q2), um das genannte aufgenommene Mittepotential im wesentlichen auf dem Pegel des genannten vorbestimmten Referenzpotentials zu halten, und um sicherzustellen, daß bei einem beliebigen zufälligen Kurzschluß zwischen einem beliebigen Punkt entlang des genannten MR-Elements (Rmr) und seiner Umgebung kein Strom fließt.

Revendications

1. Circuit amplificateur pour amplifier un signal d'entrée (Vin) généré par un élément magnétorésistif MR (Rmr) pour produire un signal de sortie ayant une valeur substantiellement proportionnelle à dRh/Rh, où Rh est la résistance de l'élément MR (Rmr) et dRh est la modification induite par le signal, de la résistance de l'élément MR (Rmr), le circuit comprenant :
   un élément MR (Rmr),
   une source de courant (J1) connectée à l'élément MR (Rmr) pour produire un courant de polarisation dans l'élément MR (Rmr),
   caractérisé en ce que le circuit comprend en outre:
   des première et seconde boucles de réaction interconnectées, la première boucle de réaction pour amplifier le signal d'entrée (Vin) sous la forme de variations du courant de polarisation de manière telle que tout écart DC soit minimisé,
   la seconde boucle de réaction fournissant une protection contre les court-circuits de l'élément MR (Rmr) en maintenant l'élément MR (Rmr) à un potentiel de référence pour limiter le courant dans l'élément MR (Rmr) dans le cas d'un court-circuit entre l'élément MR (Rmr) et une surface conductrice adjacente.

2. Circuit tel que revendiqué dans la revendication 1 dans lequel, en utilisation, les boucles de réaction coopèrent pour accroître la protection contre les court-circuits au fur et à mesure que le courant de polarisation diminue et décroître la protection contre les court-circuits au fur et à mesure que le courant de polarisation augmente.

3. Circuit tel que revendiqué dans la revendication 2 comprenant un étage d'entrée (10) ayant une paire de transistors bipolaires (Q1, Q2), les collecteurs des transistors (Q1, Q2) formant les bornes de sortie de l'étage d'entrée (20), les émetteurs des transistors (Q1, Q2) étant connectés aux bornes opposées de l'élément MR (Rmr) pour amplifier le signal d'entrée, les boucles de réaction ayant des sorties connectées communément aux bases des transistors (Q1, Q2).

4. Circuit tel que revendiqué dans la revendication 3, dans lequel la première boucle de réaction est connectée aux collecteurs des transistors (Q1, Q2) pour générer un premier signal de commande en réponse à tout écart de potentiel entre les bornes de sortie de l'étage d'entrée (20), le premier signal de commande étant couplé aux bases des transistors (Q1, Q2) pour éliminer substantiellement tout écart de potentiel entre les bornes de sortie.

5. Circuit tel que revendiqué dans la revendication 4 dans lequel le premier signal de commande est sous la forme d'un signal de courant différentiel pour ajuster le potentiel entre les bases des transistors (Q1, Q2) de manière telle qu'un courant de référence est divisé substantiellement également entre les transistors (Q1, Q2) pour produire le courant de polarisation.

6. Circuit tel que revendiqué dans la revendication 5, dans lequel la première boucle de réaction comprend une impédance dérivée d'une résistance (R1) et d'une capacité (C1) interposée en parallèle entre les transistors (Q1, Q2) pour définir la réponse en fréquence du circuit d'une ma-

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nière telle que le circuit ait une fréquence zéro dominante inférieure à une fréquence polaire dominante pour fournir une caractéristique passe-haut, la capacité (C1) servant à shunter le bruit généré par la résistance (R1).

7. Circuit tel que revendiqué dans une quelconque des revendications 4, 5 ou 6 comprenant:

un premier moyen de circuit connecté à l'élément MR (Rmr) pour détecter le potentiel central substantiellement à mi-chemin entre les bornes de l'élément MR (Rmr), la seconde boucle de réaction étant configurée pour générer un second signal de commande en réponse à une différence entre le potentiel central détecté et un potentiel de référence prédéterminé, et

un second moyen de circuit sensible au second signal de commande pour appliquer des signaux de polarisation aux bases des transistors (Q1, Q2) pour maintenir le potentiel central substantiellement au potentiel de référence.

8. Circuit tel que revendiqué dans la revendication 6 dans lequel les signaux de polarisation sont des courants substantiellement égaux pour maintenir la somme des courants d'émetteur des transistors (Q1, Q2) substantiellement égale au courant de référence.

9. Circuit tel que revendiqué dans une des revendications précédentes, dans lequel la seconde boucle de réaction comprend un moyen de retard (R2, C2) pour retarder la réponse du circuit à un court-circuit jusqu'à ce qu'il ait cessé, le moyen de retard comprenant une résistance (R2) et une capacité (C2) connectées en parallèle.

10. Circuit tel que revendiqué dans une revendication précédente, dans lequel les première et seconde boucles de réaction comprennent des amplificateurs différentiels à conductance de transfert respectifs (g1, g2) pour convertir une tension d'erreur en une sortie de courant de commande.

11. Circuit tel que revendiqué dans une des revendications précédentes comprenant un amplificateur tampon (11) pour amplifier le signal de sortie du circuit et pour accroître la largeur de bande du signal de sortie du circuit.

12. Méthode pour produire des signaux de sortie électriques dont la valeur est représentative des signaux produits par un élément magnéto-résistif MR (Rmr) et en même temps protéger l'élément MR des court-circuits électriques entre l'élément et son environnement, ladite méthode comprenant les étapes de:

connecter une source de courant (J1) à une des deux bornes d'un élément MR (Rmr) pour produire un courant de polarisation dans l'élément MR,

fournir un étage d'entrée (10) ayant au moins deux transistors bipolaires (Q1, Q2) et des bornes de sortie,

connecter les deux bornes dudit élément MR (Rmr) aux émetteurs desdits transistors (Q1, Q2) pour amplifier les écarts de courant à partir d'une valeur moyenne dans le temps dudit courant de polarisation,

connecter un premier moyen de circuit de réaction aux collecteurs desdits transistors (Q1, Q2) pour détecter le potentiel moyen dans le temps entre lesdites bornes de sortie pour produire un signal de commande différentiel, et coupler ledit signal de commande différentiel aux bases desdits transistors (Q1, Q2) pour éliminer substantiellement l'écart de potentiel moyen dans le temps entre lesdites bornes de sortie,

connecter un autre moyen de circuit de réaction aux deux bornes dudit élément MR (Rmr) pour détecter le potentiel central dudit élément MR substantiellement à mi-chemin entre lesdites bornes,

utiliser un second moyen de circuit de réaction, produisant deux signaux de commande substantiellement similaires en réponse à la différence entre le potentiel central détecté de l'élément MR (Rmr) et un potentiel de référence prédéterminé, et

en réponse auxdits signaux de commande similaires, appliquer des signaux de polarisation aux bases desdits transistors (Q1, Q2) pour maintenir ledit potentiel central détecté substantiellement égal audit potentiel de référence prédéterminé et assurer en même temps que substantiellement aucun courant ne circule dans un court-circuit accidentel entre un point de l'élément MR (Rmr) et son environnement.