

Description

The invention relates to a current divider for splitting up an input current into substantially equal output currents, comprising:

- an input terminal for receiving the input current,
- first and second output terminals for supplying the output currents,
- current branches for providing current conduction paths from the input terminal, the first output terminal and the second output terminal to respective connecting terminals,
- switching means for interconnecting the connecting terminals in a switching cycle under the control of switching signals,
- first and second current memory circuits inserted in respective ones of current branches, each current memory circuit comprising
 - first and second current terminals and a control terminal for receiving a control signal,
 - a transistor having a control electrode and having first and second main electrodes coupled to the first and second current terminals respectively, the transistor of the first current memory circuit being of a first conductivity type and the transistor of the second current memory circuit being of a second conductivity type opposite to the first conductivity type,
 - a hold-capacitor connected between the control electrode and the first main electrode and
 - a switch between the control electrode and the second main electrode which switch is open during a first level of the control signal and closed during a second level of the control signal, and
 - a clock generator for generating the switching signals for the switching means and respective control signals for the current memory circuits during consecutive switching cycles until the output currents are substantial equal.

Current dividers are used, for example, in digital-to-analog converters in which a reference current is divided by means of a plurality of current dividers into a binary weighted series of currents which are connected to a junction point by means of switches in response to the bit values of a digital word to be converted. With an augmenting number of bits ever more strict requirements are made on the accuracy of the current dividers. In static current dividers the attainable accuracy is restricted by tolerances in the manufacturing and design process of the components used.

United States Patent US-A-3 982 172 discloses a precision current source arrangement with a multiple current source arrangement which supplies a number of currents which are identical in a first approximation. These currents are each individually applied to one of the input terminals of a coupling circuit which has an equal number of input and output terminals. By means

of a periodic control signal this coupling circuit realizes such a connection pattern between the input and output terminals in a cyclically permuting fashion, that each of the output terminals is coupled to each of the input terminals within a constant cycle time during identical time intervals. By subjecting the currents which appear at the output terminals to a low-pass filter action, a number of very accurately identical currents are obtained.

A current divider as specified in the opening paragraph is known from the article entitled "Very accurate current divider", Electronics Letters, 6 July 1989, Vol. 25, No. 14.

This known current divider comprising CMOS transistors is of the dynamic type, in which the accuracy of the current division is substantially insensitive to the tolerances in the manufacturing and design process of the transistors used. The input current to be divided is distributed according to a cyclic switching pattern over a number of current branches comprising current memory circuits by means of the switching means controlled by switching signals. In dependence on the level of the control signals the current memory circuits operate as current consumer or current supplier, the supplied current being substantially equal to the previously consumed current. When the switch of the current memory circuit is closed, the transistor is arranged as a diode and across the hold-capacitor a voltage is built up which is a criterion for the current impressed through the transistor. When the switch is open, the transistor acts as a current source whose strength, as a result of the storing operation of the hold-capacitor, is substantially equal to the previously impressed current. This type of current memory circuit is also known from IEEE Journal of Solid-State Circuits, Vol. SC-24, NO. 6, p 1517 - 1522, Fig. 2. A clock generator supplies switch and control signals which are selected such that irrespective of the initial distribution of the current over the current branches, the currents through specific current branches converge to final values which are about half the input current. These currents form the output currents of the current divider.

A detrimental effect of the known current divider is that the output currents are available only during part of the cycle period of the switching pattern, which impedes the use of this divider in digital-to-analog converters which require continuously flowing currents.

It is an object of the present invention to provide a dynamic current divider having continuously available output currents.

Therefore, a current divider according to the invention of the type set out in the preamble is characterised in that

- the input terminal is coupled through a first current branch to a first connecting terminal and through a second current branch to a second connecting terminal, the first current branch comprising a first variable current source and the second current branch comprising the first current memory circuit whose

- first current terminal is coupled to the input terminal,
- the first and second output terminals are coupled through third and fourth current branches respectively, to third and fourth connecting terminals, the third current branch comprising the second current memory circuit whose first current terminal is coupled to the first output terminal,
- the switching means couple, during a first phase of the switching cycle the first to the third connecting terminal and the second to the fourth connecting terminal, and couple, during a second phase of the switching cycle the first to the fourth connecting terminal and the second to the third connecting terminal, and
- the control signals for the first and second current memory circuits respectively having the first and the second level respectively, during at least part of the first phase of the switching cycle and having the second and the first level respectively, during at least part of the second phase of the switching cycle.

In this configuration the input current is divided over the first and second current branches. During the first phase of the switching cycle the switching means couple the first current branch to the first output terminal through the third current branch and couple the second current branch to the second output terminal through the fourth current branch. The first current memory circuit in the second current branch is then arranged as a current supplier whose supplied current is available on the second output terminal through the fourth current branch. The variable current source in the first current branch delivers a current to the third current branch which current is equal to the difference between the input current and the current flowing through the second current branch. The current memory circuit included in the third current branch acts as a current consumer for the current supplied by the variable current source and passes this current to the first output terminal.

During the second phase of the switching cycle the switching means couple the first current branch to the fourth current branch and the second current branch to the third current branch, the first and second current memory circuits being changed over so that the first branch now acts as a current consumer and the second branch as a current supplier. The current flowing through the first and third current branches during the first phase now flows through the second and third current branches during the second phase. A current which is the difference between the input current and the new current through the second branch now flows through the first and fourth current branches.

Subsequent thereto, the first phase of the switching cycle is repeated. Since the proportion between the consumed and supplied powers of the current memory circuits is never exactly equal to unity, the originally unequal currents flowing through the first and second current branches will converge after a number of cycles to final

values which are substantially equal to half the input current. Since the switching means connect the first and second current branches either directly or cross-wise to the first and second output terminals during both phases of the switching cycle, the output currents are continuously available.

A further advantage of the current divider according to the invention is that the switching cycle has only two phases due to which the clock generator has a simpler structure than the prior-art current divider which operates with three phases.

A further embodiment of a current divider according to the invention is characterised, in that in the second current branch a second variable current source for supplying a current proportional to the current of the first variable current source is connected in parallel to the first current memory circuit.

The second variable current source in the second current branch in conjunction with the first variable current source in the first current branch forms a static current divider whose dividing factor is determined by the proportionality factor of the currents. The dynamic controller of the current divider now acts only on the possible difference between the currents in the first and second variable current sources and may be considered a fine adjustment of the static current division. Consequently, the current divider has a more accurate operation when reaching the final values of the currents through the current branches.

A further embodiment of a current divider according to the invention is characterised in that the first variable current source comprises a transistor of the first conductivity type having first and second main electrodes and a control electrode which are coupled to the input terminal, the first connecting terminal and a reference voltage terminal respectively.

The first variable current source in the first current branch comprises a transistor whose control electrode is maintained at a fixed voltage. The voltage difference between the first main electrode and the control electrode of this transistor continuously adjusts itself to a value which is necessary for enabling a current to flow which current is equal to the difference between the input current and the current flowing through the second current branch.

Another embodiment of a current divider according to the invention is characterised in that the fourth current branch comprises a transistor of the second conductivity type, first and second main electrodes of which transistor being coupled to the second output terminal and the fourth connecting terminal respectively, and a control electrode being coupled to the second main electrode.

When the final values of the currents through the current branches are reached, the transistor in the fourth current branch provides a better matching of the voltages on the second main electrode of the transistor of the second current memory circuit during the first and second phases of the switching cycle. This enhances the match-

ing of the current consumed and supplied by the second current memory circuit and hence the accuracy of the current divider.

Again another embodiment of a current divider according to the invention is characterised in that the second variable current source comprises a transistor of the first conductivity type having first and second main electrodes which are connected to the respective first and second main electrodes of the transistor of the first current memory circuit and having a control electrode connected to the control electrode of the transistor of the first variable current source.

The proportionality factor of the currents of the first and second variable current sources are in this case determined by transistor dimensions of the transistors used in the variable current sources.

The invention will now be further explained with reference to the appended drawing, in which:

Fig. 1 shows a first embodiment of a current divider according to the invention in two different operational modes,

Fig. 2 shows a second embodiment of a current divider according to the invention, and

Fig. 3 shows a third embodiment of a current divider according to the invention.

In the Figs. 1, 2 and 3 equivalent components are denoted by equivalent reference characters.

Fig. 1 shows a first embodiment of a current divider according to the invention. The transistors shown are of the field-effect type in which the control electrode, the first main electrode and the second main electrode correspond to the respective gate, source and drain of the field-effect transistors. The input current I_{in} to be distributed of current source 1 is connected to an input terminal 2 of the current divider and divides through a first current branch 10 which comprises a variable current source 22, to a first connecting terminal 18 and through a second current branch 12 which comprises a first current memory circuit 24, to a second connecting terminal 20. The partial currents I_{out1} and I_{out2} flow respectively, through a third current branch 7 from a first output terminal 3 to a third connecting terminal 14 and through a fourth current branch 8 from a second output terminal 4 to a fourth connecting terminal 16. Current branch 7 comprises a second current memory circuit 32. Current branch 8 establishes a direct connection between the output terminal 4 and connecting terminal 16.

The connecting terminals 14, 16, 18 and 20 of the four current branches 7, 8, 10 and 12 are interconnected through switching means 40 which are arranged as a change-over switch S1 which couples the connecting terminal 18 to connecting terminal 14 or connecting terminal 16, and a change-over switch S2 which couples the connecting terminal 20 to connecting terminal 16 or connecting terminal 14. The change-over switches S1 and S2 are operated by a switching signal 42 originating

from a clock generator 9.

The variable current source 22 comprises a transistor M1 of a first conductivity type, whose source is coupled to input terminal 2 and whose drain is coupled to connecting terminal 18. The gate of transistor M1 is connected to a reference voltage terminal 5 to which a reference voltage source 6 is connected. The input current source and the reference voltage source 6 are further connected to a suitably selected point having a fixed potential for which purpose ground has been chosen here by way of example.

The first current memory circuit 24 comprises a transistor M2 of the first conductivity type, whose source and drain are connected to a first current terminal 26 and a second current terminal 28 respectively, which in turn are coupled to the input terminal 2 and connecting terminal 20 respectively. A hold-capacitor C1 which, for that matter, may also be formed by an internal gate-source capacitance of the transistor M2, is arranged across the gate and source of transistor M2. The current memory circuit 24 further includes a switch S3 connected between the drain and the gate of transistor M2 and is operated by a control signal 44 from the clock generator 9 arriving at control terminal 30. If the switch S3 is closed, transistor M2 will be arranged as a diode and a current impressed to transistor M2 from elsewhere will cause a voltage difference across hold-capacitor C1 to be maintained after the switch S3 has been opened. Transistor M2 will then operate as a current source whose delivered current is substantially equal to the previously impressed current.

The second current memory circuit 32, whose operation is identical with that of the first current memory circuit 24, comprises a transistor M3 of a second conductivity type which is the opposite to the first conductivity type. The source and drain of transistor M3 are connected to the respective first and second current terminals 34 and 36 coupled to the output terminal 3 and the connecting terminal 14 respectively. The current memory circuit 32 further includes a hold-capacitor C2 and a switch S4 connected in a manner similar to that of current memory circuit 24. Switch S4 is operated by a control signal 46 from clock generator 9 which arrives at a control terminal 38 of current memory circuit 32.

The clock generator 9 controls the switches S1 ... S4 in a two-phase switching cycle. Fig. 1a shows the switches in the state assumed during the first phase of the switching cycle. Switch S1 couples connecting terminal 18 to connecting terminal 14, switch S2 couples connecting terminal 20 to connecting terminal 16, whereas switch S3 is open switch S4 is closed. The states of the switches during the second phase of the switching cycle are shown in Fig. 1b. Switch S1 now couples connecting terminal 18 to connecting terminal 16, switch S2 couples connecting terminal 20 to connecting terminal 14 whilst switch S3 is closed and S4 is open.

The operation of the current divider is as follows. During the first phase of the switching cycle the third tran-

sistor M3 is arranged as a diode and the second transistor as a current source, as is represented in Fig. 1a. Furthermore, the transistor M3 and the transistor M1 are connected in series between the output terminal 3 and the input terminal 2 and the transistor M2 is inserted between the second output terminal 4 and the input terminal 2. Assuming that initially the voltage across the hold-capacitor C1 is still zero, the input current i_{in} of current source 1 will completely flow through transistor M1, because the gate-source voltage of transistor M2 is zero Volts. Across the hold-capacitor C2 a voltage corresponding with the current i_{in} through transistor M3 adjusts itself. In output terminal 3 a current i_{out1} flows which is equal to i_{in} . In output terminal 4 a current i_{out2} flows which is equal to zero. During the second phase of the switching cycle all switches are changed, as is represented in Fig. 1b. The current i_{in} through the transistor M3, now acting as a current source, flows through the transistor M2 arranged as a diode while a voltage corresponding to the current through transistor M2 is built up across the hold-capacitor C1. The current i_{out1} remains equal to i_{in} and the current i_{out2} remains equal to zero, but the currents through the transistors M1 and M2 are exchanged. During the first phase of the next period of the switching cycle the exchanged currents through transistors M1 and M2 are again directly connected to the output terminals 3 and 4, so that a current $i_{out1}=0$ flows through output terminal 3 and a current $i_{out2}=i_{in}$ flows through output terminal 4. The values of the currents i_{out1} and i_{out2} are thus exchanged after each second phase, whereas the sum of the currents i_{out1} and i_{out2} remains equal to the input current i_{in} . Since the proportional number of the current impressed to the transistor M3 during the first phase to the current supplied by the transistor M3 during the second phase is never exactly equal to unity, the exchanging of the currents will be accompanied with a slight loss. Consequently, the value of the one current which initially was equal to i_{in} will finally decrease and, because the sum of the currents remains constant, the value of the other current will increase from the initial value of zero. A similar process will take place if the exchanging of the currents is accompanied with a slight amplification. Irrespective of the initial distribution of the input current i_{in} over the transistors M1 and M2, the values of the currents i_{out1} and i_{out2} will converge to each other after a number of periods of the clock signal and will both reach a final value which is substantially equal to half the input current i_{in} . The accuracy of the mutual equality is determined by the conversion from impressed current to supplied current in transistor M3.

Fig. 2 shows a second embodiment of a current divider according to the invention. The current branch 8 comprises a fourth transistor M4 arranged as a diode, which transistor has the same conductivity type and about the same dimensions as the third transistor M3. The source is connected to output terminal 4 and the interconnected gate and drain to connecting terminal 16. The fourth transistor M4 provides that when the final sit-

uation is reached the voltages on the drains of transistor M1 and transistor M2 are substantially equal, assuming that the potentials on the first and second output terminals 3, 4 are equal. The drain voltage of transistor M3 will then hardly change any longer during the first and second phases of the switching cycle, which will benefit the accuracy of the current divider.

Fig. 3 shows a third embodiment of a current divider according to the invention. A similar fifth transistor M5, whose source and drain are connected to the corresponding electrodes of transistor M2 and whose gate is connected to the reference voltage terminal 5, is arranged in parallel to the transistor M2. Transistor M5, like transistor M1, is arranged as a variable current source and provides a current which is proportional to that of transistor M1. The proportionality is determined by the dimensions of the transistors M1 and M5. The transistors M1 and M5 together form a static current divider which divides the input current i_{in} into two parts of which the proportion is determined by the dimensions of the transistors M1 and M5. The current divider now only needs to provide a dynamic control of the difference between the currents through transistors M1 and M5. This too will benefit the accuracy of the current divider. It will be evident that in the embodiment as shown in Fig. 3 the fourth transistor M4 may also be omitted.

The switches may further be arranged in a conventional manner, for example, by means of switching transistors in MOS or CMOS technology. The exemplary embodiments shown are arranged in MOS transistors, but bipolar transistors or Darlington transistors are likewise possible. The values of the first and second hold-capacitors C1, C2 are not critical. The gate-source capacitance of the transistors concerned may also be used as hold-capacitors. In order to increase the output impedance of variable current source 22, one or a plurality of transistors may be cascoded in series with the drain of transistor M1.

Claims

1. A current divider for splitting up an input current into substantially equal output currents, comprising:
 - an input terminal (2) for receiving the input current,
 - first (3) and second (4) output terminals for supplying the output currents,
 - current branches (10, 12, 7, 8) for providing current conduction paths from the input terminal (2), the first output terminal (3) and the second output terminal (4) to respective connecting terminals (18, 20, 14, 16),
 - switching means (40) for interconnecting the connecting terminals (18, 20, 14, 16) in a switching cycle under the control of switching signals (42),

sistor M3 is arranged as a diode and the second transistor as a current source, as is represented in Fig. 1a. Furthermore, the transistor M3 and the transistor M1 are connected in series between the output terminal 3 and the input terminal 2 and the transistor M2 is inserted between the second output terminal 4 and the input terminal 2. Assuming that initially the voltage across the hold-capacitor C1 is still zero, the input current i_{in} of current source 1 will completely flow through transistor M1, because the gate-source voltage of transistor M2 is zero Volts. Across the hold-capacitor C2 a voltage corresponding with the current i_{in} through transistor M3 adjusts itself. In output terminal 3 a current i_{out1} flows which is equal to i_{in} . In output terminal 4 a current i_{out2} flows which is equal to zero. During the second phase of the switching cycle all switches are changed, as is represented in Fig. 1b. The current i_{in} through the transistor M3, now acting as a current source, flows through the transistor M2 arranged as a diode while a voltage corresponding to the current through transistor M2 is built up across the hold-capacitor C1. The current i_{out1} remains equal to i_{in} and the current i_{out2} remains equal to zero, but the currents through the transistors M1 and M2 are exchanged. During the first phase of the next period of the switching cycle the exchanged currents through transistors M1 and M2 are again directly connected to the output terminals 3 and 4, so that a current $i_{out1}=0$ flows through output terminal 3 and a current $i_{out2}=i_{in}$ flows through output terminal 4. The values of the currents i_{out1} and i_{out2} are thus exchanged after each second phase, whereas the sum of the currents i_{out1} and i_{out2} remains equal to the input current i_{in} . Since the proportional number of the current impressed to the transistor M3 during the first phase to the current supplied by the transistor M3 during the second phase is never exactly equal to unity, the exchanging of the currents will be accompanied with a slight loss. Consequently, the value of the one current which initially was equal to i_{in} will finally decrease and, because the sum of the currents remains constant, the value of the other current will increase from the initial value of zero. A similar process will take place if the exchanging of the currents is accompanied with a slight amplification. Irrespective of the initial distribution of the input current i_{in} over the transistors M1 and M2, the values of the currents i_{out1} and i_{out2} will converge to each other after a number of periods of the clock signal and will both reach a final value which is substantially equal to half the input current i_{in} . The accuracy of the mutual equality is determined by the conversion from impressed current to supplied current in transistor M3.

Fig. 2 shows a second embodiment of a current divider according to the invention. The current branch 8 comprises a fourth transistor M4 arranged as a diode, which transistor has the same conductivity type and about the same dimensions as the third transistor M3. The source is connected to output terminal 4 and the interconnected gate and drain to connecting terminal 16. The fourth transistor M4 provides that when the final sit-

uation is reached the voltages on the drains of transistor M1 and transistor M2 are substantially equal, assuming that the potentials on the first and second output terminals 3, 4 are equal. The drain voltage of transistor M3 will then hardly change any longer during the first and second phases of the switching cycle, which will benefit the accuracy of the current divider.

Fig. 3 shows a third embodiment of a current divider according to the invention. A similar fifth transistor M5, whose source and drain are connected to the corresponding electrodes of transistor M2 and whose gate is connected to the reference voltage terminal 5, is arranged in parallel to the transistor M2. Transistor M5, like transistor M1, is arranged as a variable current source and provides a current which is proportional to that of transistor M1. The proportionality is determined by the dimensions of the transistors M1 and M5. The transistors M1 and M5 together form a static current divider which divides the input current i_{in} into two parts of which the proportion is determined by the dimensions of the transistors M1 and M5. The current divider now only needs to provide a dynamic control of the difference between the currents through transistors M1 and M5. This too will benefit the accuracy of the current divider. It will be evident that in the embodiment as shown in Fig. 3 the fourth transistor M4 may also be omitted.

The switches may further be arranged in a conventional manner, for example, by means of switching transistors in MOS or CMOS technology. The exemplary embodiments shown are arranged in MOS transistors, but bipolar transistors or Darlington transistors are likewise possible. The values of the first and second hold-capacitors C1, C2 are not critical. The gate-source capacitance of the transistors concerned may also be used as hold-capacitors. In order to increase the output impedance of variable current source 22, one or a plurality of transistors may be cascoded in series with the drain of transistor M1.

Claims

1. A current divider for splitting up an input current into substantially equal output currents, comprising:
 - an input terminal (2) for receiving the input current,
 - first (3) and second (4) output terminals for supplying the output currents,
 - current branches (10, 12, 7, 8) for providing current conduction paths from the input terminal (2), the first output terminal (3) and the second output terminal (4) to respective connecting terminals (18, 20, 14, 16),
 - switching means (40) for interconnecting the connecting terminals (18, 20, 14, 16) in a switching cycle under the control of switching signals (42).



- first (24) and second (32) current memory circuits inserted in respective ones of current branches (10, 12, 7, 8), each current memory circuit comprising
- first (26, 34) and second (28, 36) current terminals and a control terminal (30, 38) for receiving a control signal,
- a transistor (M2, M3) having a control electrode and having first and second main electrodes coupled to the first (26, 34) and second (28, 36) current terminals respectively, the transistor (M2) of the first current memory circuit (26) being of a first conductivity type and the transistor (M3) of the second current memory circuit (32) being of a second conductivity type opposite to the first conductivity type,
- a hold-capacitor (C1, C2) connected between the control electrode and the first main electrode and
- a switch (S3, S4) between the control electrode and the second main electrode which switch (S3, S4) is open during a first level of the control signal and closed during a second level of the control signal, and
- a clock generator (9) for generating the switching signals (42) for the switching means (40) and respective control signals (44, 46) for the current memory circuits (24, 32) during consecutive switching cycles until the output currents are substantial equal, characterized in that
- the input terminal (2) is coupled through a first current branch (10) to a first connecting terminal (18) and through a second current branch (12) to a second connecting terminal (20), the first current branch (10) comprising a first variable current source (22) and the second current branch (12) comprising the first current memory circuit (24) whose first current terminal (26) is coupled to the input terminal (2),
- the first (3) and second (4) output terminals are coupled through third (7) and fourth (8) current branches respectively, to third (14) and fourth (16) connecting terminals, the third current branch (7) comprising the second current memory circuit (32) whose first current terminal (34) is coupled to the first output terminal (3),
- the switching means (40) couple, during a first phase of the switching cycle the first (18) to the third (14) connecting terminal and the second (20) to the fourth (16) connecting terminal, and couple, during a second phase of the switching cycle the first (18) to the fourth (16) connecting terminal and the second (20) to the third (14) connecting terminal, and
- the control signals (44, 46) for the first (24) and second (32) current memory circuits respectively having the first and the second level respec-

tively, during at least part of the first phase of the switching cycle and having the second and the first level respectively, during at least part of the second phase of the switching cycle.

2. A current divider as claimed in Claim 1, characterised in that in the second current branch (12) a second variable current source (M5) for supplying a current proportional to the current of the first variable current source (22) is connected in parallel to the first current memory circuit (24).
3. A current divider as claimed in Claim 1 or 2, characterised in that the first variable current source (22) comprises a transistor (M1) of the first conductivity type having first and second main electrodes and a control electrode which are coupled to the input terminal (2), the first connecting terminal (18) and a reference voltage terminal (5) respectively.
4. A current divider as claimed in Claim 1, 2 or 3, characterised in that the fourth current branch (8) comprises a transistor (M4) of the second conductivity type, first and second main electrodes of which transistor (M4) being coupled to the second output terminal (4) and the fourth connecting terminal (16) respectively, and a control electrode being coupled to the second main electrode.
5. A current divider as claimed in Claim 2, 3 or 4, characterised in that the second variable current source comprises a transistor (M5) of the first conductivity type having first and second main electrodes which are connected to the respective first and second main electrodes of the transistor (M2) of the first current memory circuit (24) and having a control electrode connected to the control electrode of the transistor (M1) of the first variable current source (22).
6. A current divider as claimed in any of the preceding claims, characterised in that the hold-capacitor (C1, C2) is formed by the internal capacitance between the control electrode and the first main electrode of the transistor (M2, M3) of the current memory circuit (24, 32).

Patentansprüche

1. Stromteiler zum Aufspalten eines Eingangsstroms in nahezu gleiche Ausgangsströme, mit:
 - einer Eingangsklemme (2) zum Empfangen des Eingangsstroms,
 - einer ersten (3) und einer zweiten (4) Ausgangsklemme zum Liefern der Ausgangsströme,
 - Stromzweigen (10, 12, 7, 8) zum Verschaffen



- von Stromleitungspfaden von der Eingangs-
klemme (2), der ersten Ausgangsklemme (3)
und der zweiten Ausgangsklemme (4) zu jewei-
ligen Verbindungsklemmen (18, 20, 14, 16),
- Schaltmitteln (40), um die Verbindungsklem- 5
men (18, 20, 14, 16) in einem Schaltzyklus unter
der Steuerung von Schaltsignalen (42) mitein-
ander zu verbinden,
 - einer ersten (24) und einer zweiten (32) in je- 10
weils einen der Stromzweige (10, 12, 7, 8) ein-
gefügteten Stromspeicherschaltung, wobei jede
Stromspeicherschaltung folgendes umfaßt:
 - eine erste (26, 34) und eine zweite (28, 36)
Stromklemme und eine Steuerungsklemme 15
(30, 38) zum Empfangen eines Steuersignals,
 - einen Transistor (M2, M3) mit einer Steuerelek-
trode und mit einer ersten und einer zweiten, mit
der ersten (26, 34) bzw. der zweiten (28, 36)
Stromklemme gekoppelten Hauptelektrode, 20
wobei der Transistor (M2) der ersten Stromspei-
cherschaltung (26) von einem ersten Leitungs-
typ und der Transistor (M3) der zweiten Strom-
speicherschaltung (32) von einem zweiten, dem
ersten Leitungstyp entgegengesetzten Lei-
tungstyp ist,
 - einen zwischen die Steuerelektrode und die er-
ste Hauptelektrode geschalteten Haltekonden-
sator (C1, C2) und
 - einen Schalter (S3, S4) zwischen der Steuer-
elektrode und der zweiten Hauptelektrode, wel- 30
cher Schalter (S3, S4) während eines ersten
Pegels des Steuersignals geöffnet und wäh-
rend eines zweiten Pegels des Steuersignals
geschlossen ist, und
 - einen Taktgenerator (9) zum Generieren der 35
Schaltsignale (42) für die Schaltmittel (40) und
jeweiliger Steuersignale (44, 46) für die Strom-
speicherschaltungen (24, 32) während aufein-
anderfolgender Schaltzyklen, bis die Aus-
gangsströme nahezu gleich sind, 40
dadurch gekennzeichnet, daß
 - die Eingangsklemme (2) über einen ersten
Stromzweig (10) mit einer ersten Verbindungs-
klemme (18) und über einen zweiten Strom-
zweig (12) mit einer zweiten Verbindungsklem- 45
me (20) gekoppelt ist, wobei der erste Strom-
zweig (10) eine erste variable Stromquelle (22)
und der zweite Stromzweig (12) die erste
Stromspeicherschaltung (24) umfaßt, deren er-
ste Stromklemme (26) mit der Eingangsklemme 50
(2) gekoppelt ist,
 - die erste (3) und die zweite (4) Ausgangsklem-
me über einen dritten (7) bzw. vierten (8) Strom-
zweig mit einer dritten (14) und vierten (16) Ver-
bindungsklemme gekoppelt sind, wobei der drit- 55
te Stromzweig (7) die zweite Stromspeicher-
schaltung (32) umfaßt, deren erste Stromklem-
me (34) mit der ersten Ausgangsklemme (3) ge-

koppelt ist,

- die Schaltmittel (40) während einer ersten Pha-
se des Schaltzyklus die erste (18) mit der dritten
(14) Verbindungsklemme und die zweite (20)
mit der vierten (16) Verbindungsklemme kop-
peln und während einer zweiten Phase des
Schaltzyklus die erste (18) mit der vierten (16)
Verbindungsklemme und die zweite (20) mit der
dritten (14) Verbindungsklemme koppeln,
 - wobei die Steuersignale (44, 46) für die erste
(24) bzw. die zweite (32) Stromspeichersch-
altung während zumindest eines Teils der ersten
Phase des Schaltzyklus den ersten bzw. zwei-
ten Pegel haben, und während zumindest eines
Teils der zweiten Phase des Schaltzyklus den
zweite bzw. den ersten Pegel haben.
2. Stromteiler nach Anspruch 1, dadurch gekenn-
zeichnet, daß in dem zweiten Stromzweig (12) eine
zweite variable Stromquelle (M5) zum Liefern eines
zum Strom der ersten variablen Stromquelle (22)
proportionalen Stromes parallel zur ersten Strom-
speicherschaltung (24) geschaltet ist.
 3. Stromteiler nach Anspruch 1 oder 2, dadurch
gekennzeichnet, daß die erste variable Stromquelle
(22) einen Transistor (M1) des ersten Leitungstyps
mit einer ersten und einer zweiten Hauptelektrode
und einer Steuerelektrode umfaßt, die mit der Ein-
gangsklemme (2), der ersten Verbindungsklemme
(18) bzw. einer Bezugsspannungsklemme (5)
gekoppelt sind.
 4. Stromteiler nach Anspruch 1, 2 oder 3, dadurch
gekennzeichnet, daß der vierte Stromzweig (8)
einen Transistor (M4) des zweiten Leitungstyps
umfaßt, wobei eine erste und eine zweite Hauptelek-
trode dieses Transistors (M4) mit der zweiten Aus-
gangsklemme (4) bzw. der vierten Verbindungs-
klemme (16) gekoppelt sind und eine Steuerelek-
trode mit der zweiten Hauptelektrode gekoppelt ist.
 5. Stromteiler nach Anspruch 2, 3 oder 4, dadurch
gekennzeichnet, daß die zweite variable Strom-
quelle einen Transistor (M5) des ersten Leitungs-
typs umfaßt, mit einer ersten und einer zweiten
Hauptelektrode, die mit der ersten bzw. zweiten
Hauptelektrode des Transistors (M2) der ersten
Stromspeicherschaltung (24) gekoppelt sind, und
mit einer mit der Steuerelektrode des Transistors
(M1) der ersten variablen Stromquelle (22) gekop-
pelten Steuerelektrode.
 6. Stromteiler nach einem der vorhergehenden
Ansprüche, dadurch gekennzeichnet, daß der Hal-
tekondensator (C1, C2) von der inneren Kapazität
zwischen der Steuerelektrode und der ersten Haupt-
elektrode des Transistors (M2, M3) der betreffenden



Stromspeicherschaltung (24, 32) gebildet wird.

Revendications

1. Diviseur de courant pour diviser un courant d'entrée en courants de sortie pratiquement égaux comprenant:

- une borne d'entrée (2) pour la réception du courant d'entrée, 10
- des premières (3) et deuxième (4) bornes de sortie pour délivrer les courants de sortie,
- des branches de courant (10, 12, 7, 8) pour prévoir des trajets de courant à partir de la borne d'entrée (2), de la première borne de sortie (3) et de la deuxième borne de sortie (4) à des bornes de connexion respectives (18, 20, 14, 16), 15
- des moyens de commutation (40) pour interconnecter les bornes de connexion (18, 20, 14, 16) dans un cycle de commutation sous commande de signaux de commutation (42), 20
- des premiers (24) et deuxième (32) circuits de mémoire de courant insérés dans les branches de courant respectives (10, 12, 7, 8), chaque circuit de mémoire de courant comprenant 25
- des premier (26, 34) et deuxième (28, 36) bornes de courant et une borne de commande (30, 38) pour la réception d'un signal de commande, 30
- un transistor (M2, M3) présentant une électrode de commande et des première et deuxième électrodes principales couplées respectivement aux première (26, 34) et deuxième (28, 36) bornes de courant, le transistor (M2) du premier circuit de mémoire de courant (26) étant d'un premier type de conductivité et le transistor (M3) du deuxième circuit de mémoire de courant (32) étant d'un deuxième type de conductivité opposé au premier type de conductivité, 35
- un condensateur de maintien (C1, C2) connecté entre l'électrode de commande et la première électrode principale et 40
- un commutateur (S3, S4) entre l'électrode de commande et la deuxième électrode principale, lequel commutateur (S3, S4) est ouvert pendant le premier niveau du signal de commande et fermé pendant un deuxième niveau du signal de commande et 45
- un générateur d'horloge (9) pour engendrer les signaux de commutation (42) pour les moyens de commutation (40) et des signaux de commande respectifs (44, 46) pour les circuits de mémoire de courant (24, 32) pendant des cycles de commutation consécutifs jusqu'à ce que les courants de sortie soient pratiquement égaux, caractérisé en ce que 50
- la borne d'entrée (2) est couplée par l'intermédiaire d'une première branche de courant (10) 55

à une première borne de connexion (18) et par l'intermédiaire d'une deuxième branche de courant (12) à une deuxième borne de connexion (20), la première branche de courant (10) comprenant une première source de courant variable (22) et la deuxième branche de courant (12) comprenant le premier circuit de mémoire de courant (24) dont la première borne de courant (26) est couplée à la borne d'entrée (2),

- les première (3) et deuxième (4) bornes de sortie sont couplées respectivement par l'intermédiaire de troisième (7) et quatrième (8) branches de courant à respectivement des troisième (14), quatrième (16) bornes de connexion, la troisième branche de courant (7) comprenant le deuxième circuit de mémoire de courant (32) dont la première borne de courant (34) est couplée à la première borne de sortie (3),

- les moyens de commutation (40) assurant le couplage, pendant une première phase du cycle de commutation, de la première borne de connexion (18) à la troisième borne de connexion (14) et de la deuxième borne de connexion (20) à la quatrième borne de connexion (16) et, pendant une deuxième phase du cycle de commutation, de la première borne de connexion (18) à la quatrième borne de connexion (16) et de la deuxième borne de connexion (20) à la troisième borne de connexion (14) et

- les signaux de commande (44, 46) respectivement pour les premier (24) et deuxième (32) circuits de mémoire de courant présentant respectivement les premier et deuxième niveaux, pendant au moins une partie de la première phase du cycle de commutation et présentant respectivement les deuxième et premier niveaux pendant au moins une partie de la deuxième phase du cycle de commutation.

2. Diviseur de courant selon la revendication 1, caractérisé en ce que dans la deuxième branche de courant (12) une deuxième source de courant variable (M5) pour délivrer un courant proportionnel au courant de la première source de courant variable (22) est montée en parallèle avec le premier circuit de mémoire de courant (24).
3. Diviseur de courant selon la revendication 1 ou 2, caractérisé en ce que la première source de courant variable (22) est munie d'un transistor (M1) du premier type de conductivité présentant des première et deuxième électrodes principales et une électrode de commande qui sont couplées respectivement à la borne d'entrée (2), la première borne de connexion (18) et une borne de tension de référence (5).
4. Diviseur de courant selon la revendication 1, 2 ou 3, caractérisé en ce que la quatrième branche de cou-



rant (8) est munie d'un transistor (M4) du deuxième type de conductivité, dont les première et deuxième électrodes principales sont couplées respectivement à la deuxième borne de sortie (4) et la quatrième borne de connexion (18), et une électrode de commande étant couplée à la deuxième électrode principale.

5. Diviseur de courant selon la revendication 2, 3 ou 4, caractérisé en ce que la deuxième source de courant variable est munie d'un transistor (M5) du premier type de conductivité présentant des première et deuxième électrodes principales qui sont connectées aux première et deuxième électrodes principales respectives du transistor (M2) dans le premier circuit de mémoire de courant (24) et présente une électrode de commande connectée à l'électrode de commande du transistor (M1) de la première source de courant variable (22).
6. Diviseur de courant selon l'une des revendications précédentes, caractérisé en ce que le condensateur de maintien (C1, C2) est formé par la capacité interne entre l'électrode de commande et la première électrode principale du transistor (M2, M3) du circuit de mémoire de courant (24, 32).

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