CLAIMS

1. A semiconductor construction comprising a plurality of trenched regions having narrow bottom portions and upper wide portions over the bottom portions, the upper wide portions having wider dimensions than the narrow bottom portions, said trenched regions also having voids retained at least substantially entirely within the narrow bottom portions; the voids having peripheries that are devoid of linear portions -

wherein sidewalls of the narrow bottom portions are curved relative to sidewalls of the upper wide portions and a bottomwall is linear extending between the curved sidewalls-;

wherein each of the plurality of the trenched regions extends lengthwise in a first direction; and

a first gate extending lengthwise in a second direction, the second direction is perpendicular to the first direction, and

a second gate over the first gate, the second gate extending lengthwise in a direction perpendicularly to the lengthwise direction of the first gate.

2. The construction of claim 1 wherein one or more of said trenched regions differ in shape relative to at least one other of said trenched regions.

3. The construction of claim 1 wherein the voids are gaseous regions.

4. The construction of claim 1 wherein said trenched regions are trenched isolation regions.

5. The construction of claim 4 further comprising transistor devices adjacent the isolation regions.

6. The construction of claim 5 wherein at least some of the transistor devices having source/drain regions that elevationally overlap the voids.

7. The construction of claim 6 wherein the isolation regions comprise electrically insulative material within the top and bottom portions.

8. The construction of claim 7 wherein the electrically insulative material is substantially homogeneous in composition throughout the top and bottom portions.

9. The construction of claim 1 wherein said the voids are retained entirely within said bottom portions.

10. The construction of claim 1 wherein individual bottom portions have a substantially vertical sidewall, and wherein individual upper portions join the individual bottom portions through a step which extends substantially perpendicularly to the sidewall.

11. The construction of claim 10 wherein the upper portions are at least about twice as wide as the bottom portions.

12. A memory array, comprising:

a plurality of transistors over a semiconductor substrate, the transistors comprising gates and source/drain regions adjacent the gates;

a plurality of charge storage devices electrically coupled with some of the source/drain regions; and

a plurality of isolation regions extending within the substrate and providing electrical isolation for at least some of the transistors; at least some individual isolation regions comprising lower narrow portions joining to upper wide portions at steps, comprising substantially solid insulative material within the narrow portions and wide portions, and comprising voids substantially entirely contained within the narrow portions.

13. The memory array of claim 12 wherein at least a majority of the transistor gates of the memory array are floating gates of programmable memory devices.

14. The memory array of claim 12 wherein at least a majority of the transistor gates of the memory array are not floating gates of programmable memory devices.

15. The memory array of claim 12 wherein at least some of the upper wide portions are at least about twice as wide as the bottom narrow portions they are joined to.

16. The memory array of claim 12 wherein at least some of the bottom narrow portions have substantially vertical sidewalls, and wherein at least some of the steps extend substantially perpendicularly to such sidewalls.

17. The memory array of claim 12 wherein the substantially solid electrically insulative material comprises silicon dioxide.

18. The memory array of claim 12 wherein at least some of the upper wide portions extend to a depth of at least about 1 micron within the substrate.

19. The memory array of claim 12 wherein at least some of the source/drain regions are adjacent individual voids and elevationally overlap such individual voids.

20. The memory array of claim 12 wherein the charge storage devices are capacitors.

21. The memory array of claim 12 wherein the voids are gaseous regions.

22. An electronic system, comprising:

a processor;

a memory device in data communication with the processor; and

wherein at least one of the memory device and the processor includes one or more electrical isolation regions comprising lower narrow portions joining to upper wide portions at steps, comprising a non-gaseous material within the narrow portions and wide portions, and comprising voids substantially entirely contained within the narrow portions.

23. The electronic system of claim 22 wherein the voids are gaseous regions.

24. The electronic system of claim 22 further comprising transistors adjacent at least some of the electrical isolation regions.

25. The electronic system of claim 22 further comprising programmable memory devices adjacent at least some of the electrical isolation regions.

26. The electronic system of claim 22 wherein at least some of the upper wide portions are at least about twice as wide as the bottom narrow portions they are joined to.

27. The electronic system of claim 22 wherein at least some of the bottom narrow portions have substantially vertical sidewalls, and wherein at least some of the steps extend substantially perpendicularly to such sidewalls.

28. The electronic system of claim 22 wherein the non-gaseous material is a substantially solid electrically insulative material.

29. The electronic system of claim 28 wherein the substantially solid electrically insulative material comprises silicon dioxide.

30. A method of forming a semiconductor construction, comprising:

providing a semiconductor substrate;

forming a pair of openings extending into the substrate, the individual openings having an upper portion of a first width and a lower portion of a second width less than the first width, with the first and second width portions joining at a step; the openings being spaced from one another by a region of the semiconductor substrate;

forming electrically insulative material within the openings; the electrically insulative material substantially filling the upper portions of the openings and leaving voids within the lower portions of the openings; and

forming a transistor having a floating gate over said region of the semiconductor substrate; and

forming a control gate over the floating gate.

31. The method claim 30 wherein the upper portions of the openings are at least about twice as wide as the lower portions.

32. The method claim 30 wherein the lower portions have substantially vertical sidewalls, and wherein the steps extend substantially perpendicularly to such sidewalls.

33. The method of claim 30 further comprising an insulative cap extending lengthwise over and along an upper surface of the floating gate, the insulative cap comprising a width only as wide as a width of the floating gate.

34. The method of claim 30 further comprising an insulative cap extending lengthwise over and along an upper surface of the control gate, the insulative cap comprising a width that equals a width of the control gate.

35. The method of claim 30 wherein the voids comprise ambient gas.

36. The method of claim 30 wherein the voids are surrounded by insulative material, and wherein the voids comprise gas from the insulative material.

37. The method of claim 30 further comprising sidewall spacers on opposite sides of the floating gate and wherein the transistor comprises source/drain regions, the sidewall spacers overlap, in a vertical direction, a portion of the source/drain regions.

38. The method of claim 30 wherein the transistor comprises a gate dielectric under the floating gate and source/drain regions elevationally below the gate dielectric wherein an outer edge of the gate dielectric is aligned with an inner edge of one of the source/drain regions.

39. The method of claim 30 wherein the transistor comprises a gate dielectric under the floating gate and an insulative cap over the floating gate, and wherein an outer edge of the gate dielectric is aligned with an outer edge of the insulative cap.

40. The method of claim 30 wherein the transistor comprises:

a gate dielectric under the floating gate;

source/drain regions elevationally below the gate dielectric; and

an insulative cap over the floating gate and wherein an outer edge of the gate dielectric is aligned with an outer edge of the insulative cap, and wherein both outer edges are aligned with an inner edge of one of the source/drain regions.