

Abstract

When a memory cell (MC) is downsized by reducing the distance between a drain region (12a) and a source region (12b) on the surface of a fin (S2) with a high impurity concentration inside the fin (S2), the shape of the fin (S2) can be set such that a potential difference between a memory gate electrode (MG) and the fin (S2) is reduced to suppress the occurrence of disturbance. Accordingly, the memory cell (MC) achieves downsizing and suppression of the occurrence of disturbance.