

Description

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to radio receivers and, more particularly, is directed to a radio receiver using frequency synthesizer tuning that can provide the operator with a fine tuning feel similar to that given by a variable-capacitor tuned radio receiver.

Description of the Background

In radio receivers employing a frequency synthesizer in the tuning circuitry, a local oscillation signal is formed by a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL) configuration. When the frequency-dividing ratio N of the variable frequency-dividing circuit that is part of the phase-locked loop is varied, the local oscillation frequency varies in response and a change in the reception frequency occurs.

Accordingly, in the frequency synthesizer receiver channel selection can be performed by simple key operations that drive the tuned frequency up and down. For example, the reception frequency can be sequentially and continuously changed by simply depressing an up-channel key or a down-channel key. Nevertheless, although this kind of tuning is modern in technique when channel selection is accomplished by the aforementioned key operations it has been found to be troublesome and wearisome for the listener/operator.

On the other hand, in the more old-fashioned radio receiver utilizing a so-called variable capacitor to perform channel selection, the listener finds it more enjoyable to tune the receiver by rotating a knob, while listening to sounds emanating from the loudspeaker of the receiver. It has been found that the listener feels better about tuning the reception frequency in the variable capacitor type receiver than when tuning the frequency synthesizer receiver.

A frequency synthesizer receiver has been proposed in which a dial, that is, a knob, is provided so that the frequency-dividing ratio N of the synthesizer is varied in response to rotation of the dial, thereby changing the reception frequency just like the variable-capacitor tuner.

It is also known that in a phase-locked loop (PLL), when the frequency-dividing ratio N is changed the loop requires a finite lock-up time to stabilize itself relative to the frequency-dividing ratio N thus changed. During this lock-up time, the reception frequency is not stabilized and, therefore, muting of the output sound must be effected.

In an example based on the broadcast standards of the United States of America, if the reception fre-

quency is varied by one step, for example 100 kHz, by changing the frequency-dividing ratio N by 1 in an FM radio receiver, the lock-up time is as short as 2 milliseconds. Nevertheless, when the reception frequency is changed a large amount all at once, for example, from 87.5 MHz to 108 MHz, by changing the frequency-dividing ratio N from the minimum value to the maximum value, the lock-up time will increase to approximately 200 milliseconds.

Furthermore, even when the reception frequency is changed step by step, in increments of 100 kHz by changing the frequency-dividing ratio N by 1 each time, if the dial is continuously turned at a relatively high speed, then the frequency-dividing ratio N is considerably varied in a short period of time, so that the required lock-up time will be extended just like the case where the frequency-dividing ratio N is changed from its minimum value to its maximum value all at once. In other words, if the frequency-dividing ratio N is increased by a very large amount per unit time, the lock-up time of the phase-locked loop increases unacceptably.

Therefore, in a synthesizer receiver employing a dial, muting is effected during operation of the dial and the duration of the muting period is in a range of from 500 milliseconds to 1000 milliseconds.

More specifically, when the dial is rotated by one tuning increment amount corresponding to 100 kHz in an FM receiver, a device that detects the rotation of the dial will produce a pulse P_r , as shown in Fig. 1A. Then, at the leading edge of the pulse P_r the muting is turned ON from its OFF state, as shown in Fig. 1B. Further, when a preceding muting period T_a , for example, 10 milliseconds, elapses after the muting is turned ON, the frequency-dividing ratio N whose value is changed by 1 is set in the phase-locked loop.

When a succeeding muting period T_b , for example, 500 milliseconds, elapses after the new frequency-dividing ratio N is set in the phase locked loop, the muting is turned OFF.

On the other hand, when the dial is rotated more quickly, a number of pulses P_r proportional to the rotational amount of the dial will be generated with a pulse width and cycle corresponding to the rotational speed, as shown in Fig. 2A. Referring to Fig. 2B, the muting is turned ON at a timing point of the first pulse P_r of the string of pulses and, as shown in Fig. 2C, a frequency-dividing ratio N whose value is changed by 1 at every leading edge of a pulse P_r is set in the phase-locked loop. Just as in the single increment example, when the period T_b elapses following the time T_a , in which the frequency dividing ratio is changed, the muting is turned OFF.

Accordingly, in this previously proposed system regardless of the rotational speed of the dial, the duration of the period T_b will be longer than that of the lock-up time of the phase-locked loop with respect to all pulses P_r , so that the muting is performed without

fail during the lock-up time period of the phase-locked loop. Nevertheless, if the muting period T_b is determined as described above, when the fine tuning is performed by slowly rotating the dial in the forward or backward direction or when the reception frequency is varied by slowly rotating the dial, the duration of the muting period, that is, the period in which no sound is produced, will increase, so that the user finds it difficult and annoying to make fine tuning adjustments to the receiver.

A phase locked loop type tuner circuit in which the frequency can be set by a rotary dial is described in GB-A-2 046 043. The circuit has a time delay element for limiting the speed of the regulating loop in dependence upon the speed at which the tuning frequency is scanned, the latter being materialized by counting pulses. The idea is to ensure that the regulating loop can follow the counting state of the pulses sufficiently rapidly over a range of counting speeds.

Finally, an example of a phase locked loop receiver corresponding to the preamble of claim 1 can be found in JP-A-55 26348. Here, the circuit produces muting pulses of fixed duration each time an index on the rotational tuning dial is detected.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved synthesizer tuned receiver that can eliminate the aforementioned shortcomings and disadvantages encountered with previously proposed receivers.

Another object of the present invention is to provide a synthesizer tuned receiver in which the muting time is reduced so as to provide a fine tuning feeling similar to that of a receiver utilizing variable-capacitor tuning.

A further object of the present invention is to provide a synthesizer tuned receiver in which muting can be positively performed during the lock-up time of a phase-locked loop used in the synthesizer tuner.

According to an aspect of the present invention, a synthesizer tuned receiver is provided in which a local oscillation signal is generated from a phase-locked loop and a frequency-dividing ratio of a variable frequency-dividing circuit in the phase-locked loop is varied, so that the frequency of the local oscillation signal is changed to vary the reception frequency. The receiver further comprises a dial, a rotary encoder connected so that rotation of the dial rotates the encoder, a circuit for varying the frequency-dividing ratio on the basis of an output from the rotary encoder, a muting circuit provided in the audio signal line, a circuit for controlling the muting circuit on the basis of the output from the rotary encoder, and a circuit responsive to the output of the rotary encoder for varying in the length of time the muting circuit is operational in proportion to the speed of rotation of the dial.

The above and other objects, features, and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, in which like reference numerals represent the same or similar parts in the several views.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B, and 1C are waveform diagrams useful in explaining the operation of a previously proposed synthesizer tuned receiver;

Figs. 2A, 2B, and 2C are waveform diagrams useful in explaining the operation of a previously proposed synthesizer tuned receiver when the tuning dial is turned quickly;

Fig. 3 is a schematic in block diagram form showing a synthesizer-type receiver according to an embodiment of the present invention;

Fig. 4 is a table of a frequency dividing ratio, a local oscillation frequency, and a reception frequency useful in explaining the operation of the present invention;

Figs. 5A and 5B combine to form a flow chart useful in explaining the operation of the present invention; and

Fig. 6 is a waveform diagram useful in explaining the operation of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT.

Fig. 3 is a block diagram showing an embodiment of a synthesizer-type receiver according to the present invention, in which the circuit elements designated by reference numerals 1 to 14R constitute a receiving system.

More specifically, a broadcast signal is received at an antenna 1 and supplied to an antenna tuning circuit 2 of the electronic tuning type, from which there is derived an FM broadcast wave signal S_r having a frequency f_r . This signal S_r is supplied through a high-frequency amplifier 3 to a mixing circuit 4, and a voltage controlled oscillator (VCO) 21 derives an oscillation signal S_o having a frequency f_o expressed as:

$$f_o = f_r + 10.7 \text{ (MHz)} \quad (1)$$

This oscillation signal S_o is supplied to mixer circuit 4 as a local oscillation signal, and the broadcast signal S_r is frequency converted to an intermediate frequency (IF) signal S_i . In this case the intermediate frequency is 10.7 MHz.

The intermediate frequency signal S_i is supplied through an intermediate frequency (IF) amplifier 5 to an FM demodulating circuit 6, in which it is demodulated to provide a stereo composite signal or a monaural signal. The stereo composite signal, for example, is supplied to a stereo demodulating circuit 11,

wherein it is demodulated to provide left and right channel stereo audio signals, L and R. Signals L and R are then supplied through switching circuits 12L and 12R and amplifiers 13L and 13R to output terminals 14L and 14R, respectively. The switches 12L and 12R are used to mute the left and right stereo signals L and R.

In the receiver of Fig. 3, voltage controlled oscillator 21 and the circuits numbered 22 to 25 constitute a phase-locked loop indicated generally at 20. More specifically, the signal S_o from voltage controlled oscillator 21 is supplied to a variable frequency-divider 22, in which it is frequency divided by N. The frequency-divided signal from the variable-frequency divider 22 is supplied to a phase-comparing circuit 23 along with an oscillation signal S_p having a reference frequency of 100 kHz that is generated by an oscillation circuit 24. Oscillation signal S_p is compared with the frequency divided signal in comparing circuit 23, and the compared output is supplied through a low-pass filter (LPF) 25 to voltage controlled oscillator 21 as the control voltage. The output of low-pass filter 25 is also supplied to tuning circuit 2 as a channel selection voltage.

Accordingly, in the steady state, a frequency-divided signal from frequency-dividing circuit 22 and the oscillation signal S_p are equal to each other in frequency so that the frequency f_o of the oscillation signal S_o is expressed as:

$$f_o = 100 \text{ (kHz)} \times N \quad (2)$$

At that time, equation (1) is established.

Therefore, if the frequency-dividing ratio N is changed by 1 increment each in a range of from 982 to 1187, as represented in the first line of the chart of Fig. 4, the local oscillation frequency f_o is changed in steps of 0.1 MHz in the range from 98.2 MHz to 118.7 MHz, as represented by the second line in the chart of Fig. 4. Thus, as shown in the third line of the chart of Fig. 4, a reception frequency f_r is changed in steps of 0.1 MHz in the range from 87.5 MHz to 108 MHz, in response to changes in the frequency-dividing ratio N.

In the circuit of Fig. 3, a microcomputer 30 is used to control the overall operation of this synthesizer tuned receiver embodying the present invention. In microcomputer 30 there are provided a central processing unit (CPU) 31, a read only memory (ROM) 32 in which there is written a routine 100 shown in detail in Fig. 5, a random access memory (RAM) 33 providing a processing work area, an input port 34, and an output port 35.

The frequency-dividing ratio N is supplied from microcomputer 30 and is set in frequency-dividing circuit 22, and a muting control signal S_m is supplied from system control circuit 30 to control switching circuits 12L and 12R. A rotary encoder 41 is electrically connected to microcomputer 30, whereby a pulse Pr and a pulse Pq are supplied to microcomputer 30 from

rotary encoder 41. The phase of the pulse Pq is advanced or delayed relative to the phase of pulse Pr in response to the rotational direction of the input shaft of rotary encoder 41. A dial or knob 42 is attached to the input shaft of rotary encoder 41 for manual actuation.

A detecting circuit 7 is connected to intermediate frequency amplifier 5 to detect whether the intermediate frequency signal S_i is present, and a detected output signal from detecting circuit 7 is fed to microcomputer 30. As a practical matter, a liquid crystal display (LCD) device 43 is connected to microcomputer 30 to display the received frequency f_r in a digital fashion.

Microcomputer 30 operates under control of its central processing unit 31 that follows a predetermined routine 100, shown in the flowchart of Figs. 5A and 5B. Referring to Figs. 5A and 5B, when a power switch of the receiver is turned ON in step 101 processing of CPU 31 begins in step 102 with the initialization of flags and parameters. More specifically, period T_b is selected to be 100 milliseconds, and a preceding muting flag AFLG and a succeeding muting flag BFLG are both reset to "0".

The processing of the CPU 31 proceeds to step 103 where a waiting period of 10 milliseconds is carried out and, following that period, the processing of CPU 31 proceeds to decision step 104. It is determined in step 104 whether rotary encoder 41 is generating the pulse Pr, that is, whether dial 42 is being rotated. If the pulse Pr is not obtained at step 104, the processing of the CPU 31 proceeds from step 104 to step 121. In decision step 121, the status of the flag AFLG is checked. In this case, since AFLG = "0" was initially established, the processing of CPU 31 proceeds to decision step 131, where the status of the flag BFLG is checked. In this case, since BFLG = "0" was initially established, then the processing of CPU 31 proceeds from step 131 to step 141, where it is determined whether any other processing was requested. If a NO is output at step 141, the processing of CPU 31 returns from step 141 to step 103. If a YES is output at step 141, then the processing of the CPU 31 proceeds from step 141 to step 142, where the requested processing is executed. Following that, the processing of CPU 31 returns to step 103.

Accordingly, when dial 42 is not turned, a loop of steps 103, 104, 121, 131, 141, and possibly 142, is repeated approximately every 10 milliseconds, in that order.

When dial 42 is turned by the operator, rotary encoder 41 produces the pulse Pr, which occurrence is identified at decision step 104. If a YES is output at step 104, then the processing of the CPU 31 proceeds to step 111, where the rotational direction of dial 42 is identified by checking the phase relation of pulses Pr and Pq. If it is determined that dial 42 is rotated in a direction to increase the received frequency f_r , then the processing of CPU 31 proceeds to step 112. In

step 112, the present frequency-dividing ratio N, stored in RAM 33 of microprocessor 30, is incremented by 1 unit, and the processing of CPU 31 proceeds to the next decision step 114.

On the other hand, if it is determined in step 111 that dial 42 is rotated in the direction to decrease the present received frequency fr, the processing of CPU 31 proceeds to step 113, where the frequency-dividing ratio N is decremented by 1 unit, and the processing of CPU 31 proceeds to decision step 114.

In decision step 114, the cycle of the pulse Pr is checked, that is, the rotational speed of the dial 42 is checked. If the cycle of the pulse Pr is shorter than 100 milliseconds, for example, the processing of CPU 31 proceeds from step 114 to step 115, where the muting period Tb is increased as $T_b = T_b + 10$ milliseconds. In step 114 a maximum value for the period Tb is selected to be 500 milliseconds. After the muting period Tb has been increased, the processing of CPU 31 proceeds to step 116. On the other hand, if it is determined in step 114 that the cycle of the pulses Pr is longer than 100 milliseconds, the processing of CPU 31 proceeds directly to step 116.

At step 116, as shown at timing point t_1 in Fig. 6, the muting control signal Sm has a high level "1", whereby switching circuits 12L and 12R are opened and the muting operation is carried out. In the next step 117, AFLG = "1" is set, and the processing of CPU 31 proceeds to decision step 121, wherein it is determined whether the first flag AFLG is "0" or "1". In this case, since AFLG = "1" was established then the processing of CPU 31 proceeds to decision step 122, where it is determined whether the period Ta (Ta 10 milliseconds) has elapsed after the timing point t_1 , at which time the processing at step 116 is secured.

In this case, the processing of CPU 31 is executed in the order of step 116, step 117, step 121, and step 122, while the period Ta has not yet elapsed, as shown at timing point t_2 , so that the processing of CPU 31 proceeds from step 122 to decision step 141.

Thereafter, the processing of CPU 31 returns to step 103 and executes steps 103, 104, 111, 112, 114, 115, 116, 117, and 121 in that order. Then, when it is determined that period Ta has elapsed after timing point t_1 , the processing of CPU 31 proceeds from step 122 to step 123, where the frequency-dividing ratio N stored in RAM 33 of microcomputer 30 is supplied to, and set in, frequency-dividing circuit 22 as a new frequency-dividing ratio N at timing point t_3 . Accordingly, after the lock-up time from this timing point t_3 , the received frequency fr is based upon the new frequency-dividing ratio N.

Then, the processing of CPU 31 proceeds to step 124, where the data indicative of the new reception frequency fr is supplied to liquid crystal display (LCD) device 43, and the new reception frequency fr is digitally displayed to the operator. In the next step 125, flags AFLG = "0" and BFLG = "1" are established, and

the processing of CPU 31 proceeds to step 141.

Thereafter, the processing of the CPU 31 returns to step 103, and again proceeds through step 104 to step 121. In this case, since AFLG = "0" is established, the processing of CPU 31 proceeds from step 121 to step 131. In step 131, the flag BFLG = "1" is determined and the processing of CPU 31 proceeds to step 132, where it is determined whether the period Tb has elapsed starting from timing point t_3 . In this case, decision step 132 is executed for the first time, and the period Tb has not yet elapsed, as shown at timing point t_4 in Fig. 6. Then, the processing of CPU 31 proceeds from step 132 to step 141.

As described above, a loop formed of step 103, step 104, step 121, step 131, step 132, step 141, and possibly step 142, is repeated from the timing point t_3 . At that time, if dial 42 is further rotated, steps 111 to 117 are executed, whereby the muting time Tb is increased from 100 milliseconds in increments of 10 milliseconds each. Further, at that time, AFLG = "1" is established at step 117, so that the operations such as steps 103 to 121 to step 125 or the like during the timing points t_1 to t_5 are executed.

At timing point t_5 , the muting period Tb will have elapsed and this timing lapse is identified at step 132, at which time the processing of CPU 31 proceeds from step 132 to step 133, whereat Sm = "0" is established, resulting in switching circuits 12L and 12R being released and closed so that the muting ceases. In the next step 134, the period Tb is selected to be 100 milliseconds and the succeeding flag BFLG is reset to "0". Then, the processing of CPU 31 proceeds to step 141.

If the frequency of the newly selected channel is such that the broadcast wave signal Sr can not be received, Sm = "1" is established on the basis of the detection output from detecting circuit 7, and muting is carried out for the received frequency fr.

As described above, according to the present invention, in a synthesizer-tuned receiver performing channel selection by utilizing a dial as in a variable-capacitor tuner, the muting time Tb is varied in response to the rotational speed of the dial, so that when fine tuning is carried out by slowly turning the dial, the muting time can be reduced, which can provide the operator a fine tuning feel similar to that given by the variable-capacitor tuned radio receiver.

Further, when the dial is turned quickly, the muting time is increased, so that the lock-up time period for the phase-locked loop in the synthesizer tuner can be positively muted.

Claims

1. A frequency synthesizer tuned receiver in which a local oscillation signal (50) is generated by a phase-locked loop (22-25) and a frequency-div-



step 112, the present frequency-dividing ratio N , stored in RAM 33 of microprocessor 30, is incremented by 1 unit, and the processing of CPU 31 proceeds to the next decision step 114.

On the other hand, if it is determined in step 111 that dial 42 is rotated in the direction to decrease the present received frequency f_r , the processing of CPU 31 proceeds to step 113, where the frequency-dividing ratio N is decremented by 1 unit, and the processing of CPU 31 proceeds to decision step 114.

In decision step 114, the cycle of the pulse P_r is checked, that is, the rotational speed of the dial 42 is checked. If the cycle of the pulse P_r is shorter than 100 milliseconds, for example, the processing of CPU 31 proceeds from step 114 to step 115, where the muting period T_b is increased as $T_b = T_b + 10$ milliseconds. In step 114 a maximum value for the period T_b is selected to be 500 milliseconds. After the muting period T_b has been increased, the processing of CPU 31 proceeds to step 116. On the other hand, if it is determined in step 114 that the cycle of the pulses P_r is longer than 100 milliseconds, the processing of CPU 31 proceeds directly to step 116.

At step 116, as shown at timing point t_1 in Fig. 6, the muting control signal S_m has a high level "1", whereby switching circuits 12L and 12R are opened and the muting operation is carried out. In the next step 117, AFLG = "1" is set, and the processing of CPU 31 proceeds to decision step 121, wherein it is determined whether the first flag AFLG is "0" or "1". In this case, since AFLG = "1" was established then the processing of CPU 31 proceeds to decision step 122, where it is determined whether the period T_a (T_a 10 milliseconds) has elapsed after the timing point t_1 , at which time the processing at step 116 is secured.

In this case, the processing of CPU 31 is executed in the order of step 116, step 117, step 121, and step 122, while the period T_a has not yet elapsed, as shown at timing point t_2 , so that the processing of CPU 31 proceeds from step 122 to decision step 141.

Thereafter, the processing of CPU 31 returns to step 103 and executes steps 103, 104, 111, 112, 114, 115, 116, 117, and 121 in that order. Then, when it is determined that period T_a has elapsed after timing point t_1 , the processing of CPU 31 proceeds from step 122 to step 123, where the frequency-dividing ratio N stored in RAM 33 of microcomputer 30 is supplied to, and set in, frequency-dividing circuit 22 as a new frequency-dividing ratio N at timing point t_3 . Accordingly, after the lock-up time from this timing point t_3 , the received frequency f_r is based upon the new frequency-dividing ratio N .

Then, the processing of CPU 31 proceeds to step 124, where the data indicative of the new reception frequency f_r is supplied to liquid crystal display (LCD) device 43, and the new reception frequency f_r is digitally displayed to the operator. In the next step 125, flags AFLG = "0" and BFLG = "1" are established, and

the processing of CPU 31 proceeds to step 141.

Thereafter, the processing of the CPU 31 returns to step 103, and again proceeds through step 104 to step 121. In this case, since AFLG = "0" is established, the processing of CPU 31 proceeds from step 121 to step 131. In step 131, the flag BFLG = "1" is determined and the processing of CPU 31 proceeds to step 132, where it is determined whether the period T_b has elapsed starting from timing point t_3 . In this case, decision step 132 is executed for the first time, and the period T_b has not yet elapsed, as shown at timing point t_4 in Fig. 6. Then, the processing of CPU 31 proceeds from step 132 to step 141.

As described above, a loop formed of step 103, step 104, step 121, step 131, step 132, step 141, and possibly step 142, is repeated from the timing point t_3 . At that time, if dial 42 is further rotated, steps 111 to 117 are executed, whereby the muting time T_b is increased from 100 milliseconds in increments of 10 milliseconds each. Further, at that time, AFLG = "1" is established at step 117, so that the operations such as steps 103 to 121 to step 125 or the like during the timing points t_1 to t_5 are executed.

At timing point t_5 , the muting period T_b will have elapsed and this timing lapse is identified at step 132, at which time the processing of CPU 31 proceeds from step 132 to step 133, whereat $S_m = "0"$ is established, resulting in switching circuits 12L and 12R being released and closed so that the muting ceases. In the next step 134, the period T_b is selected to be 100 milliseconds and the succeeding flag BFLG is reset to "0". Then, the processing of CPU 31 proceeds to step 141.

If the frequency of the newly selected channel is such that the broadcast wave signal S_r can not be received, $S_m = "1"$ is established on the basis of the detection output from detecting circuit 7, and muting is carried out for the received frequency f_r .

As described above, according to the present invention, in a synthesizer-tuned receiver performing channel selection by utilizing a dial as in a variable-capacitor tuner, the muting time T_b is varied in response to the rotational speed of the dial, so that when fine tuning is carried out by slowly turning the dial, the muting time can be reduced, which can provide the operator a fine tuning feel similar to that given by the variable-capacitor tuned radio receiver.

Further, when the dial is turned quickly, the muting time is increased, so that the lock-up time period for the phase-locked loop in the synthesizer tuner can be positively muted.

Claims

1. A frequency synthesizer tuned receiver in which a local oscillation signal (50) is generated by a phase-locked loop (22-25) and a frequency-div-



iding ratio of a variable frequency divider (22) in the phase locked loop is varied so that a frequency of the local oscillation signal is changed to vary a reception frequency of the receiver, comprising:

a tuning dial (42);

a rotary encoder (41) arranged to rotate in response to rotation of said tuning dial for producing pulses (Pr) the period of which indicates a rotational speed of said tuning dial;

means (31,33) for varying the frequency-dividing ratio of the variable frequency divider in response to an output from said rotary encoder for changing the reception frequency of the receiver;

a muting circuit (22) arranged in an audio output signal line of the receiver for selectively muting an output signal of the receiver for a period of time (T_b); and

means (31) for controlling said muting circuit (22) in response to an output from said rotary encoder, characterized in that said means for controlling said muting circuit is operative for varying the said muting time (T_b) of said muting circuit in proportion to a speed of rotation of said dial (42) detected by said rotary encoder (41).

2. A frequency synthesizer tuned receiver according to claim 1, wherein said means (31) for controlling said muting circuit and for varying the muting time of said muting circuit include means for reducing the muting time (T_b) when the period of said pulses is longer than a predetermined time and said tuning dial (42) is rotated slowly.

3. A frequency synthesizer tuned receiver according to claim 1, further comprising means (43) for visually displaying the reception frequency of the receiver.

4. A frequency synthesizer tuned receiver according to claim 1, wherein said rotary encoder (41) produces two output signals in response to rotation of said tuning dial, in which a leading/lagging phase relationship between said two output signals indicates a direction of rotation of said tuning dial.

5. A frequency synthesizer tuned receiver according to claim 1, further comprising a detector circuit responsive to the reception frequency of the receiver for detecting whether a broadcast signal is received at the reception frequency and producing an output signal fed to said means (31) for controlling for causing the muting circuit to mute the output signal when the broadcast signal is not received at the reception frequency.

Patentansprüche

1. Mit Hilfe eines Frequenzsynthesizers abstimmbarer Empfänger, in dem eine Phasenregelschaltung (22-25) ein lokales Oszillatorsignal (S_0) erzeugt und das Frequenzteilverhältnis eines variablen Frequenzteilers (22) in der Phasenregelschaltung so variiert wird, daß die Frequenz des lokalen Oszillatorsignals zur Varierung der Empfangsfrequenz des Empfängers geändert wird, mit einem Abstimmdrehknopf (42), mit einem Drehkodierer (41), der so angeordnet ist, daß er sich in Abhängigkeit von der Drehbewegung des Abstimmdrehknopfs dreht und dabei Impulse (W_r) erzeugt, deren Periode für die Drehgeschwindigkeit des Abstimmdrehknopfs kennzeichnend ist, mit einer Einrichtung (31, 33) zum Variieren des Frequenzteilverhältnisses des variablen Frequenzteilers in Abhängigkeit von dem Ausgangssignal des Drehkodierers zur Änderung der Empfangsfrequenz des Empfängers, mit einer in einer Audioausgangssignalleitung des Empfängers angeordneten Stummschalteneinrichtung (22) zum selektiven Stummschalten des Empfängerenausgangssignals während einer Zeitperiode (T_b), sowie mit einer Einrichtung (31) zur Steuerung der Stummschalteneinrichtung (22) in Abhängigkeit von dem Ausgangssignal des Drehkodierers, dadurch gekennzeichnet, daß die Einrichtung (31) zur Steuerung der Stummschalteneinrichtung eine zu der von dem Drehkodierer (41) detektierten Drehgeschwindigkeit des Abstimmdrehknopfs (42) proportionale Änderung der Stummschaltzeit (T_b) der Stummschalteneinrichtung bewirkt.

2. Mit Hilfe eines Frequenzsynthesizers abstimmbarer Empfänger nach Anspruch 1, bei dem die Einrichtung (31) zur Steuerung der Stummschalteneinrichtung und zur Änderung der Stummschaltzeit der Stummschalteneinrichtung Mittel aufweist, die Mittel aufweist, die die Stummschaltzeit (T_b) verkürzen, wenn die Periode der genannten Impulse eine vorbestimmte Zeit überschreitet und der Abstimmdrehknopf (42) langsam gedreht wird.

3. Mit Hilfe eines Frequenzsynthesizers abstimmbarer Empfänger nach Anspruch 1, der ferner Mittel (43) zur visuellen Anzeige der Empfangsfrequenz des Empfängers aufweist.

4. Mit Hilfe eines Frequenzsynthesizers abstimmbarer Empfänger nach Anspruch 1, bei dem der Drehkodierer (41) in Abhängigkeit von der Dre-



hung des Abstimm-drehknopfs zwei Ausgangssignale erzeugt, wobei die vorellende/nacheillende Phasenbeziehung zwischen diesen beiden Ausgangssignalen die Drehrichtung des Abstimm-drehknopfs kennzeichnet.

5. Mit Hilfe eines Frequenzsynthesizers abstimmbarer Empfänger nach Anspruch 1, der ferner eine auf die Empfangsfrequenz des Empfängers ansprechende Detektorschaltung aufweist, die feststellt, ob auf der jeweiligen Empfangsfrequenz ein Rundfunksignal empfangen wird, und die ein der Einrichtung (31) zur Steuerung der Stummschalteneinrichtung zugeführtes Ausgangssignal erzeugt, das die Stummschalteneinrichtung zum Stummschalten des Ausgangssignal veranlaßt, wenn auf der Empfangsfrequenz kein Rundfunksignal empfangen wird.

Revendications

1. Récepteur accordé par synthétiseur de fréquence, dans lequel un signal d'oscillation locale (S_o) est produit par une boucle à phase asservie (22-25) et un rapport de division de fréquence d'un diviseur de fréquence variable (22) contenu dans la boucle à phase asservie varie de façon que la fréquence du signal d'oscillation locale varie pour faire varier la fréquence de réception du récepteur, comprenant :
 - un cadran (42) de réglage d'accord de fréquence ;
 - un codeur rotatif (41) disposé de façon à tourner en liaison avec la rotation dudit cadran de réglage d'accord de fréquence et servant à produire des impulsions (P_r) dont la période indique la vitesse de rotation dudit cadran de réglage d'accord de fréquence ;
 - un moyen (31, 33) servant à faire varier le rapport de division de fréquence du diviseur de fréquence variable en fonction du signal de sortie dudit codeur rotatif afin de modifier la fréquence de réception du récepteur ;
 - un circuit (22) d'application d'accord silencieux, disposé dans une ligne de sortie de signaux audio du récepteur, servant à rendre sélectivement muet le signal de sortie du récepteur pendant une certaine durée (T_b) ; et
 - un moyen (31) servant à commander le circuit d'application d'accord silencieux (22) en fonction du signal de sortie dudit codeur rotatif ;
 - caractérisé en ce que ledit moyen servant à commander ledit circuit d'application d'accord silencieux a pour fonction de faire varier ledit temps d'accord silencieux (T_b) dudit circuit d'application d'accord silencieux proportionnellement à la vitesse de rotation dudit cadran (42), détec-

tée par ledit codeur rotatif (41).

2. Récepteur accordé par synthétiseur de fréquence selon la revendication 1, où ledit moyen (31) servant à commander ledit circuit d'application d'accord silencieux et à faire varier le temps d'accord silencieux dudit circuit d'application d'accord silencieux comporte un moyen servant à réduire le temps d'accord silencieux (T_b) lorsque la période desdites impulsions est plus longue qu'un temps prédéterminé et que ledit cadran (42) de réglage d'accord de fréquence tourne lentement.
3. Récepteur accordé par synthétiseur de fréquence selon la revendication 1, comprenant en outre un moyen (43) servant à afficher visuellement la fréquence de réception du récepteur.
4. Récepteur accordé par synthétiseur de fréquence selon la revendication 1, où ledit codeur rotatif (41) produit deux signaux de sortie en fonction de la rotation dudit cadran de réglage d'accord de fréquence, la relation d'avance ou de retard de phase entre lesdits deux signaux de sortie indiquant le sens de rotation dudit cadran de réglage d'accord de fréquence.
5. Récepteur accordé par synthétiseur de fréquence selon la revendication 1, comprenant en outre un circuit détecteur qui répond à la fréquence de réception du récepteur en déterminant si un signal de radiodiffusion est reçu sur la fréquence de réception et qui produit un signal de sortie à destination dudit moyen (31) de commande afin d'amener le circuit d'application d'accord silencieux à rendre muet le signal de sortie lorsque le signal de radiodiffusion n'est pas reçu à la fréquence de réception.