What is claimed is:

1. A memory device, comprising:

a memory cell array including a plurality of memory cells, wherein each of the plurality of memory cells includes a switching element, and a data storage element connected to the switching element, wherein the data storage element includes a phase change material; and

a memory controller configured to perform a control operation with respect to a first memory cell of the plurality of memory cells by inputting an operating current to the first memory cell, and inputting a compensation current flowing from the data storage element to the switching element in the first memory cell before or after inputting the operating current to the first memory cell,

wherein the control operation includes a reading operation for reading data stored in the first memory cell and a programming operation for storing data in the first memory cell, and

when the control operation is a reading operation, a time for which the compensation current is input to the first memory cell is shorter than a time for which the operating current is input to the first memory cell.

2. The memory device of claim 1, wherein, when the control operation is the programming operation, the memory controller inputs the compensation current to the first memory cell after inputting the operating current to the first memory cell.

3. The memory device of claim 1 or claim 2, wherein, when the control operation is the programming operation, the operating current and the compensation current flow in different directions in the first memory cell.

4. The memory device of any one of claims 1 to 3, wherein, when the control operation is the programming operation, a magnitude of the compensation current is less

than a magnitude of the operating current.

5. The memory device of any one of claims 1 to 4, wherein, when the control operation is the programming operation, the memory controller inputs the compensation current only when the first memory cell is in a reset state.

6. The memory device of claim 1, wherein, when the control operation is the reading operation, the memory controller inputs the compensation current to the first memory cell before or after inputting the operating current to the first memory cell.

7. The memory device of claim 1, wherein, when the control operation is the reading operation, the operating current and the compensation current flow along the same direction in the first memory cell.

8. The memory device of claim 1, when the control operation is the reading operation, wherein a magnitude of the compensation current is greater than a magnitude of the operating current.

9. The memory device of claim 1, wherein, when the control operation is the reading operation, the memory controller inputs the compensation current only when the first memory cell is in a set state.

10. The memory device of any one of claims 1 to 9, wherein the compensation current is input to the first memory cell in a plurality of sequentially generated pulses.

11. The memory device of claim 1, wherein the memory controller inputs the compensation current to the first memory cell, before the operating current is input when the first memory cell is in a set state, and inputs the compensation current to the first memory

cell after the operating current is input when the first memory cell is in a reset state.

12. The memory device of any one of claims 1 to 11, wherein the switching element of the first memory cell includes an ovonic threshold switch (OTS).

13. A memory device, comprising:

a memory cell array including a plurality of memory cells, wherein each of the plurality of memory cells includes a first electrode, a switching element connected to the first electrode, a data storage element connected to the switching element, and a second electrode connected to the data storage element; and

a memory controller configured to read data stored in a first memory cell of the plurality of memory cells by inputting a reading current to the first memory cell, wherein the memory controller is further configured to input a compensation current to the second electrode of the first memory cell before or after inputting the reading current, and

wherein the memory controller inputs the compensation current to the first memory cell only when the first memory cell is in a set state, in which the data storage element of the first memory cell has a crystalline phase.

14. The memory device of claim 13, wherein the memory controller inputs the reading current to the first electrode or the second electrode of the first memory cell.

15. The memory device of claim 13 or claim 14, wherein a magnitude of the reading current is less than a magnitude of a first threshold current, wherein the first threshold current is capable of generating a phase change in a phase change material included in the data storage element of the first memory cell, and the compensation current is greater than the first threshold current.

16. The memory device of any one of claim 13 to 15, wherein a time for which

the compensation current is input to the first memory cell is shorter than a time for which the reading current is input to the first memory cell.

17. A memory device, comprising:

a memory cell array including a plurality of memory cells, wherein each of the plurality of memory cells includes a first electrode, a switching element connected to the first electrode, a data storage element connected to the switching element, and a second electrode connected to the data storage element; and

a memory controller configured to store data in a first memory cell of the plurality of memory cells by inputting a program current to the first memory cell, wherein the memory controller is further configured to input a compensation current to the second electrode of the first memory cell after storing the data in the first memory cell,

wherein the program current and the compensation current flow in different directions in the first memory cell.