This invention relates to a photosensitive line transfer device provided with negative feedback amplifiers.

Photosensitive line transfer devices of the prior art are well known. We shall refer, for example, to French patent applications FR-A-2,504,334 and FR-A-2,538,200 filed in the name of Thomson-CSF.

It will be recalled that these devices generally comprise:

- a photosensitive zone of M lines of N photosensitive points onto which the image to be read is projected and converted into electrical charges, termed signal charges;

- an interface element of M points, termed line memory, connected via conductive columns to the photosensitive points of the various lines, which receives, in a preferred method of operation, in turn, the stray charges found on the columns before the arrival of the signal charges and the signal charges stored by each line;

- a charge transfer shift register which receives the signal charges coming from the memory and delivers in series the electrical image analysis signal;

- a drain for evacuation of the stray charges coming from the memory.

French patent application FR-A-2,524,751 relates to photosensitive line transfer devices provided with negative feedback amplifiers. The input of each of these amplifiers is connected to a conductive column and to a diode termed input diode of the line memory and its output is connected to a transfer gate of the memory, adjacent to one of the input diodes.

Negative feedback amplifiers have the advantage of dividing the apparent capacity C of the conductive columns by G + 1, where G is the gain of the amplifiers, which is generally of the order of 50.

Consequently, the transfer of the charges from the columns to the memory is performed more quickly and the transfer efficiency for a given transfer time is improved. The temporal noise due to the channel situated under each gate of the memory connected to an amplifier is reduced since it is proportional to $\sqrt{C}$.

A major disadvantage of negative feedback amplifiers, and one which will be demonstrated by the Applicant in the detailed description

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of the figures, is that it is not possible, if one wishes to obtain satisfactory operation, to connect them to a gate of the memory having an embedded channel, and one for which the transfer of the charges is a volume transfer. One is therefore compelled to use gates, and therefore a memory, for which the charges are transferred by surface transfer.

We shall here give a brief reminder of the advantages which there are in using a memory where the charges are transferred by volume transfer. To achieve a maximum transfer efficiency, a read register with embedded channel is generally used. The use of a memory where the charges are transferred by volume transfer permits a bi-lateral passage of the charges between the memory and the read register, this being particularly advantageous in the case of operation with a double driver charge as was described in patent application FR-A-2,538, 200. In the case where the transfer is performed on the surface in the memory, it is not possible to tranfer the charges from the register to the memory, since, for a given voltage applied to the gates, the surface potentials are at a higher level in the case of volume tranfer than in the case of surface transfer. The use of a memory where the charges are transferred by volume transfer also permits improvement of the vertical transfer efficiency. This efficiency is inversely proportional to the capacity of the columns, which is diminished because of the volume transfer. In fact, the columns consist essentially of interconnected read diodes. These diodes are reverse-biassed. Because of the volume transfer, these diodes receive a higher biassing voltage, for identical applied voltages on the elements of the line memory, and the capacity of these diodes is reduced. Furthermore, the noise during transfers between the columns and the line memory has two sources, namely a thermal noise which is proportional to the square root of the column capacity and a noise proportional to the surface and volume traps under the transfer gate between the columns and the line memory. The change-over to volume transfer reduces these two components by reducing the capacity of the columns, as was mentioned above and by eliminating the interface traps.

Another disadvantage of negative feedback amplifiers is that they introduce noise, particularly at low frequency. This noise can in certain cases reach the same level as the read noise introduced by the channel of the transfer gate between the columns and the memory.

This invention enables the problems set out above to be solved. In particular it permits the use of a transfer gate between the columns and the memory and of a memory in which the charges are transferred by volume transfer. In one particular mode of implementation, this invention also provides a reduction in the low frequency noise due to the negative feedback amplifiers.

This invention relates to a photosensitive line transfer device, comprising a photosensitive area of M lines of N photosensitive points, the photosensitive points of the varous lines being connected in parallel by conductive columns to diodes belonging to a line memory, which performs at least the transfer to a read register of the signal charges of the same line, this photosensitive device comprising negative feedback amplifiers the input of each of which is connected to a column and to a diode of the memory and the output from each of which is connected to a transfer gate of the memory, adjacent to one of the diodes, characterised in that:

- the line memory and the read register are so constructed that transfer of the charges takes place there by volume transfer;

- means enable the threshold voltage of each amplifier to be adjusted so that the point of operation of the assembly constitued by each amplifier, the diode and the memory gate to which it is connected, is situated in the high gain area of the transfer characteristic of the amplifier.

In the following we shall describe various methods of construc--ting means for adjusting the threshold voltage of each amplifier.

To reduce the low frequency noise due to the amplifiers, this invention proposes to perform successively a double reading of the stray charges found on the conductive columns and of the signal charges, with only two driver charges. It will be shown in the detailed description of the figures that this double reading enables the low frequency noise due to the amplifiers to be filtered.

Other objects, characteristics and results of the invention will emerge from the following description, given as a non-exhaustive example and illustrated by the attached figures which show:

- figure 1, a diagram of a photosensitive line transfer device provided with negative feedback amplifiers, as known in the prior art;

- figure 2, a method of constructing amplifiers connected to the line memory;

- figures 3 and 5, graphs respectively illustrating the operation of a device according to the prior art and according to the invention;

- figures 4, 6 and 7, diagrams illustrating various means for raising the threshold voltage of the amplifiers;

- figures 8, 9 and 10a to g, graphs and diagrams illustrating the low frequency filtering achieved;

- figure 11, a diagram of a method of constructing a line transfer device provided with negative feedback amplifiers and performing a double reading.

In the various figures, the same references denote the same elements, but, for reasons of clarity, the dimensions and proportions of various elements are not respected.

Figure 1 shows the diagram of a photosensitive line transfer device provided with negative feedback amplifiers according to the above-mentioned known art.

Figure 1 shows diagrammatically the photosensitive area 1 with M lines of N photosensitive points 2. A shift register 3 enables each line in turn to be addressed. Conductive columns C_1 to C_N connect in parallel the photosensitive points of a given column to a line memory 4. Only the input diodes 5 of the memory which are connected to the columns, and the transfer gates P which are adjacent to them have been shown.

Each of some negative feedback amplifiers 6 has its input connected to a conductive column and to an input diode 5 of the memory and its output connected to a transfer gate P between the columns and the memory.

The signal charges coming from the memory are transferred into a charge transfer shift register 7 termed read register which delivers in series the electrical image analysis signal S. The amplifiers 6 are constructed in conventional manner using two MOS transistors mounted as an inverter.

Figure 2 gives the diagram of such an amplifier consisting of an enrichment MOS transistor T_1 in series with a depletion MOS transistor T_2, connected to the line memory. The gate of T_1 constitutes the amplifier input which is connected to an input diode 5 of the memory and to a conductive column C_i. One of the other electrodes of the transistor T_1 is connected to a constant biassing voltage V_{SS} and a last electrode of the transistor T_1 constitutes the output from the amplifier, which is connected to an electrode of the transistor T_2 and to a gate P for transfer of the charges from the columns to the memory.

The gate of the transistor T_2 is connected to the output from the amplifier and a last electrode of the transistor T_2 is connected to a constant biassing voltage V_{DD}.

In the case where an enrichment transistor T_2 is used its gate is connected to the constant biassing voltage V_{DD}.

In the above-mentioned known art, it is not specified whether the line memory, and therefore the gates P for transfer of the charges between the columns and the memory, operate a surface transfer or a volume transfer of the charges, but only that "the voltages of the source and of the drain must be chosen so that the inverter operates in a high gain area".

The Applicant will demonstrate in the following that this device can operate satisfactorily only with a line memory, and therefore gates P for transfer of the charges from the column to the memory, performing a surface transfer of the charges.

The point of equilibrium of the assembly of figure 2 is obtained by the intersection of the transfer characteristic V_P, V_C of the amplifier, where V_P is the output voltage from the amplifier and V_C its input voltage with the curve representing the potential ϕ_S of the channel under the gate P in terms of the voltage V_P applied to this gate.

Figure 3 shows, in the same plane, as a solid line the characteristic of the amplifier and in broken lines the curve $(\phi_S, V_P)8$ for the gate P in the case of a surface transfer and the curve $(\phi_S, V_P)9$ for the gate P in the case of a volume transfer.

The two graphs 8 and 9 of the gate P are practically straight lines of slopes k_S and k_V, positive and close to one in the case of usual techniques. The points of intersection of the straight lines 8 and 9 with the transfer characteristic of the amplifier are termed P_{OS} and P_{OV}.

These straight lines 8 and 9 cut the V_P line at the Y axis points V_{TPS} and $-V_{TPV}$ and the V_C, ϕ_S line at the X-axis points $-k_S . V_{TPS}$ and $k_V . V_{TPV}$.

On the amplifier transfer characteristic have been entered the points H and B which delimit the high gain zone of the amplifier transfer characteristic, which is the one for which the two transistors T_1 and T_2 are biassed to saturation.

The point H is the one starting from which the transistor T_2 reaches saturation; it has the Y-axis $V_{DD} - |V_{T2}|$, where V_{T2} is the threshold voltage of the transistor T_2.

The point B is the one starting from which the transistor T_1 operates as a triode. It has the Y axis $V_C - V_{T1}$, where V_{T1} is the threshold voltage of the transistor T_1.

Figure 3 shows the straight line 10 of equation $V_P = V_C - V_{T1}$ which cuts the line V_C, ϕ_S at the X axis V_{T1} and the line V_P at the Y axis $- V_{T1}$.

The point P_{OS} is always situated above the point B since the following inequality is always true: $V_{T1} > - k_S . V_{TPS}$, V_{T1}, k_S and V_{TPS} being positive and the straight lines 8 and 10 approximately parallel. For good operation, it is also necessary for the point P_{OS} not to be too close to the point H because when a charge arrives on a column to be transferred the operating point P_{OS} of X-axis V_{CO} passes into a point P of X-axis $V_C = V_{CO} - V_C$ closer to H. Adjustment of the voltages V_{DD} and V_{SS} enables the point P_{OS} to be moved away from point H. In figure 3, it has been indicated that the intersection of the amplifier characteristic with the line V_P occurs at the Y-axis point V_{DD} and that the amplifier characteristic tends

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towards a Y-axis horizontal asymptote close to V_{SS}.

The voltage V_{SS} and then the voltage V_{DD} can be regulated so that the following condition is true: $V_{DD} - V_{T2} > V_{PO} + G. \Delta V_C$ where V_{PO} is the Y axis of the point P_{OS}.

In conclusion with a surface gate P, the amplifier operates in a high gain zone.

The point P_{OV} is always situated below the point B since the following inequality is always true: $V_{T1} < K_V. V_{TPV}$ and the straight lines 9 and 10 are approximately parallel. In fact, in usual techniques, V_{T1} varies between 0.5 and 1.5 V and V_{TPV} between 3 and 10 V, with a slope K_V close to one.

Figure 3 clearly demonstrates that since the straight line 9 is positioned below the straight line 10 it is not possible to make the point P_{OV} pass between the points H and B, even by acting upon the biassing voltages V_{DD} and V_{SS}.

Consequently, since in the above-mentioned patent it is stated that it is necessary to act upon the biassing voltages V_{DD} and V_{SS} in order for the inverter to operate in a high gain zone, this means that it is necessary to use gates P and therefore a line memory where transfer of the charges takes place on the surface with all the disadvantages which this involves.

It is not possible to obtain satisfactory operation with gates P, and therefore a line memory, where transfer of the charges takes place in volume, if only the biassing voltages V_{DD} and V_{SS} are available to adjust the point of operation.

According to the invention, satisfactory operation is achieved by using gates P and a line memory with embedded channel, where the transfer of the charges is performed in volume, by displacing the straight line 10 of equation $V_P = V_C - V_{T1}$ so that the straight line 9 is situated above the straight line 10. Thus the point of operation P_{OV} is situated between the points H and B. Figure 5 shows the new arrangement of the straight lines 9 and 10 and of the points P_{OV} and B. According to the invention, means are used whereby the threshold voltage V_{T1} of each amplifier may be adjusted so that the following inequality is true: $V_{T1} > k_V. V_{TPV}$. This threshold voltage of the amplifier is that at which it starts to drive. In the case of

one method of constructing the amplifier such as that shown in figure 2, the threshold voltage of the amplifier is that of the MOS transistor T_1.

Figure 4 shows a method of constructing the means for adjusting the voltage V_{T1}.

The voltage V_{T1} is increased by effecting an enrichment 11 in its own type of impurities of the area of the substrate 12 located under the gate of the transistor T_1 so as to have: $V_{T1} > K_V \cdot V_{TPV}$.

In figure 4, it will be seen that the gate P and the transistor T_2 are constructed on a channel in volume, marked TV.

Whatever the means used to adjust V_{T1}, it is possible to make under the gate P an area 13 of a type of impurities opposite to that of the embedded channel marked TV situated under this gate. The value of T_{TPV} is thus reduced, this making it easier to satisfy the inequality: $V_{T1} > K_V \cdot V_{TPV}$.

Such doping operations are generally performed under the transfer gates of the read register operating in volume.

Figure 6 shows another method of constructing means for adjusting the threshold voltage of each amplifier.

In figure 6, the amplifier consists as in figure 1 of two transistors T_1 and T_2 but a third and afourth MOS transistor T_3 and T_4, mounted as followers, are interposed between each input diode 5 of the memory and the gate of the transistor T_1.

The threshold voltage of the device of figure 6 is equal to $V_{T3} + V_{T1}$, where V_{T3} is the threshold voltage of the MOS transistor T_3 the gate of which is connected to a diode 5 of the memory.

In the method of construction of figure 6, MOS transistors T_3 and T_4 have been used of the enrichment and depletion types respectively.

The gate of transistor T_3 is connected to the input diode 5 of the memory and to a conductive column, the other two electrodes of this transistor are connected to the voltage V_{DD} and to the gate of the transistor T_1. The transistor T_4 has its gate and one electrode connected to the biassing voltage V_{SS} and another electrode connected to the gate of the transistor T_1.

In a variant, an MOS transistor T_4 of the enrichment type may be used the gate of which is connected to the gate of the MOS transistor T_1.

Another method for adjusting the threshold voltage of each amplifier is shown in figure 7. It consists of using an amplifier comprising two transistors mounted as an inverter, as in figure 2, but in this case an MOS transistor T_2 is used of the N channel depletion type and an MOS transistor T_1 of the P channel depletion type, which enables the threshold voltage V_{T1} of the amplifier to be increased sufficiently. The use of a depletion type MOS transistor T_1 enables the noise to be reduced.

The threshold voltage of the amplifier is adjusted in this case by means of the P type implantation located under the gate of the transistor T_1.

The various means described for adjusting the threshold voltage of the amplifiers may be used simultaneously.

Furthermore, the operating point can also be set by adjusting the biassing voltages V_{DD} and V_{SS}, but this setting is not sufficient on its own for the operating point P_{OV} to be situated in the high gain zone of the amplifier characteristic. In the introduction to the description, it was explained that one disadvantage of negative feedback amplifiers is the noise which they introduce essentially at low frequency.

This noise is due to the MOS transistors. At low frequency, these transistors have an 1/f spectral response the cut-off frequency of which is between 20 and 100 KHz. At high frequency, these transistors have a much lower noise level and a spectrum level similar to that of a white noise.

In figure 8, the broken line graph 14 represents the spectral distribution of the amplifier noise.

The Applicant offers a solution which enables the low frequency noise due to the amplifiers to be reduced and which consists of effecting a double reading.

This solution will be explained with reference to figures 10a to f.

In the above-mentioned patent application FR-A-2,538,200, an analysis process of a line transfer type photosensitive device is described in which the stray charges found on the columns are evacuated before reading the signal charges. It is this double reading which is used to filter the low frequency noise due to the amplifiers whereas its initial purpose was the evacuation of the stray charges.

Figure 10a shows an input diode 5 of the memory, with its transfer gate P, the amplifier 6 which is connected between the diode and the memory, and the main two sources of temporal noise which are the noise voltage e_n of the amplifier and the noise current i_n of the channel under the gate P.

The noise current i_n engenders a noise proportional to $\sqrt{KTC}$, where K is the Boltzmann constant, T the temperature and C the capacity of the columns which is divided by G + 1 by means of the negative feedback amplifier.

The noise voltage of the amplifier introduces a fluctuation onto the potential barrier under the gate G on which depends the transfer of the charges to the memory.

Depending on the spectral distribution of the noise, this potential barrier has its level which varies during the transfer of the signal charges if it is a question of high frequency components or from one reading of the signal charges to the following reading, if it is a question of low frequency components.

The double reading enables the low frequency components to be eliminated as will be shown.

In figures 10b and 10e, solid lines represent the potential barrier under the gate P, when there is no noise and broken lines the potential barrier under the gate P when noise is present. The noise can produce an increase or a reduction in the level of the barrier, as shown respectively in figures 10b and 10e. Reading of the stray charges Q_B found on the columns causes alignment of the potential existing under the diode 5 on the temporary level of the potential barrier, as shown in figures 10c and 10f.

Consequently, when the signal charges Q_S arrive on the columns they are transmitted in their entirety as shown in figures 10d and 10g.

A reading of the signal charges effected immediately after the reading of the stray charges therefore enables the low frequency components of the noise to be filtered, provided that the level of the potential barrier under the gate P has not changed between the two readings.

The transfer function of such a filtering is expressed in terms of the frequency f of the noise by the equation:
$A = 1 - \cos 2\pi f \tau$, where τ is the time interval between two readings.

In figure 9, graph 15 represents the transfer function of the double reading operation.

In figure 8, the solid line graph 16 represents the spectral distribution of the amplifier noise with double reading which shows the low frequency filtration achieved.

The filtering of low frequency noise by means of double reading has been verified experimentally by artificially injecting noise onto the columns.

In the above-mentioned patent application FR-A-2,538,200 the double reading of the charges necessitates three driver charges as shown diagrammatically in figure 4 of that patent. A driver charge Q_O of the order of 4 to 5 times the maximum signal charge is necessary in order to transfer the charges from the columns to the memory. This very strong charge Q_O remains stored under the capacities C_1 of the memory and two driver charges Q_1 and Q_2 of lesser strength are required to transfer the signal charges Q_S and the stray charges Q_B from the memory respectively to the read register and the drain.

In the case of a photosensitive line transfer device provided with negative feedback amplifiers, two driver charges Q_1 and Q_2 are sufficient. In fact, the apparent capacity of the columns is divided by G + 1, the driver charge necessary for an effective transfer of the charges from the columns to the memory may be reduced and a driver charge of the order of one tenth of the maximum signal charge is sufficient.

Such a driver charge may without difficulty be supplied by a charge transfer shift register without its storage capacity and its dimensions being increased for this.

Consequently, in the device according to the invention two driver charges Q_1 and Q_2 are used, of the same amplitude as the charges Q_1 and Q_2 of the Prior Art which serve both for the transfer of the charges from the columns to the memory and from the memory to the read register or to the evacuation drain. These driver charges are not memory-stored but preferably injected by two charge transfer shift registers, which are the read register 7 and an auxiliary register 14 which serves only for the injection of a driver charge.

The new structure of the device according to the invention is shown in figure 11.

The line memory now comprises only a single stage with intermediate gates C_1, which no longer serve for storage of the driver charges Q_O as in patent application FR-A-2,538,200, but which serve to direct the signal charges Q_S to the read register and the stray charges Q_B towards a drain. This directing is performed through transfer gates C_2 and C_3.

Figure 11 shows symbolically that a driver charge Q_1 is obtained by permanently injecting this quantity of charge into the read register 7. This driver charge is transferred into the memory before the arrival of the charges to be read.

It is possible to obtain this driver charge Q_1 in another way for example by injection at the level of the gates C_1 of the memory from diodes associated with injection gates.

As far as the driver charge Q_2 is concerned, this can be introduced into the memory from the evacuation drain.

These various possibilities for generating the driver charges were set out in patent application FR-A-2,538,200.

The driver charge Q_2 may also be generated by means of an auxiliary charge transfer shift register, into which this quantity of charge Q_2 is injected in series. Figure 11 shows such an auxiliary register 14, which is positioned parallel with the read register and which comprises gates 15 permitting transfers of the driver charges Q_2 into the read register.

It would also be possible to arrange this auxiliary register 14 parallel with the series of input diodes 5 and to transfer the charges Q_2 from the register into the diodes 5.

In figure 11, arrows symbolise the various transfers accompanying the double reading. The transfers permitting evacuation of the stray charges and the transfers permitting reading of the signal charges have been shown on two successive stages of the device.

The driver charges Q_1 are transferred from the read register, into the memory then under the input diodes 5 of the memory. The charges $Q_1 + Q_B$ are then transferred to the memory and then towards the evacuation drain, Q_B being the stray charges found on the columns.

The driver charges Q_2 are transferred from the auxiliary register, into the read register, into the memory then under the input diodes 5 of the memory.

After arrival of the signal charges Q_S on these diodes, the charges $Q_2 + Q_S$ are transferred into the memory then into the read register.

All of these transfers take place during the line return time. During the line time, the signal charges are read and new driver charges are injected in series into the registers.

For an optimum functioning of the device, charges Q_1 and Q_2 as similar as possible are used which allows a perfect symmetry of the injection elements.

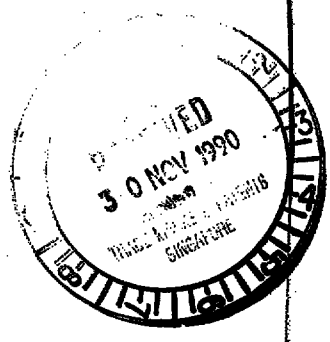
The charges Q_1 and Q_2 may be used for transfer of the signal charges and of the stray charges alike, except in the method of construction of figure 11 where it is necessary to use the driver charges Q_1 first before transferring the driver charges Q_2 into the read register, this requiring use of the charges Q_1 to transfer the stray charges and the charges Q_2 to transfer the signal charges.

Lastly, an auxiliary register 14 is used where transfer of the charges takes place in volume so as to have an optimum transfer efficiency particularly in the lateral direction.

Double reading makes it possible to eliminate stray charges as well as to reduce the low frequency noise due to the amplifiers.

The photosensitive line transfer device provided with negative feedback amplifiers may be used with an anti-dazzle device at the level of each photosensitive point.

Even in this case, the use of double reading is very advantageous for noise reduction.



CLAIMS

1. Photosensitive line transfer device, comprising a photosensitive zone (1) of M lines of N photosensitive points, the photosensitive points of the various lines being connected in parallel by conductive columns ($C_1 \ldots C_N$) to diodes (5) belonging to a line memory, which performs at least the transfer to a read register (7) of the signal charges (Q_S) of the same line, this photosensitive device comprising negative feedback amplifiers (6) the input of each of which is connected to a column and to a diode (5) of the memory and the output of each of which is connected to a transfer gate (P) of the memory, adjacent to one of the diodes, characterised in that:

- the line memory (4) and the read register (7) are so constructed that transfer of the charges is a volume transfer;

- means for adjusting the threshold voltage (V_{T1}) of each amplifier (6) so that the operation point (P_{OV}) of the assembly constituted by each amplifier (6), the diode (5) and the gate (P) of the memory (4) to which it is connected, is situated in the high gain zone (HB) of the transfer characteristic of the amplifier.

2. Device according to claim 1, characterised in that each amplifier (6) consists of a first and a second MOS transistor (T_1, T_2), mounted as an inverter.

3. Device according to claim 2, characterised in that it comprises a first enrichment-type MOS transistor (T_1) the gate of which constitutes the input of the amplifier, one of the other electrodes of which is connected to a constant biassing voltage (V_{SS}) and the last electrode of which constitutes the output of the amplifier and is connected to an electrode of the second MOS transistor (T_2).

4. Device according to claim 3, characterised in that it comprises a second depletion-type MOS transistor (T_2) the gate of which is connected to the output from the amplifier and one other electrode of which is connected to a constant biassing voltage (V_{DD}).

5. Device according to claim 3, characterised in that it comprises a second enrichment-type MOS transistor (T_2), the gate of which is connected to one of its electrodes which receives a constant biassing voltage (V_{DD}).

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6. Device according to one of claims 2 to 5, characterised in that the means for adjusting the threshold of each amplifier (6) consist of an enrichment (11) in its own type of impurities of the area of the substrate (12) situated under the gate of the first MOS transistor (T_1).

7. Device according to one of claims 2 to 6, characterised in that the means for adjusting the threshold voltage of each amplifier (6) consist of a follower stage comprising a third and a fourth MOS transistor (T_3, T_4), interposed between each diode (5) of the memory (4) and the input of an amplifier (6). The threshold voltage of each amplifier being adjusted by means of the threshold voltage (V_{T3}) of the third MOS transistor the gate of which is connected to a diode of the memory.

8. Device according to one of claims 2 to 7, characterised in that the means for adjusting the threshold voltage of each amplifier (6) consist of the realisation of a first P channel depletion-type MOS transistor (T_1) and of a second N channel depletion-type MOS transistor (T_2).

9. Device according to one of claims 1 to 8, characterised in that under each transfer gate (P) of the memory (4), adjacent to an input diode (5), there exists a zone (13) of a type of impurities opposite to that of the embedded channel (TV) situated under this gate.

10. Device according to one of claims 1 to 9, characterised in that the line memory (4) consists of a series of storage gates (C_1), adjacent to the transfer gates (P) of the memory connected to the amplifiers (6) each storage gate (C_1) being connected to two transfer gates (C_2, C_3) one leading to a drain for evacuation of the charges (D) and the other to the read register (7).

11. Device according to claim 10, characterised in that the read register (7) is a charge transfer shift register which is positioned parallel with the line memory (4) and which comprises means for injecting into all of its stages a first driver charge (Q_1).

12. Device according to one of claims 10 or 11, characterised in that it comprises an auxiliary charge transfer shift register (14) performing volume transfer of the charges, which is positioned parallel

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with the read register (4) and which comprises means of injecting into all of its stages a second driver charge (Q_2) and gates (15) performing transfer of these second driver charges into the read register.

13. Device according to one of claims 10 or 11, characterised in that it comprises an auxiliary charge transfer shift register (14), performing volume transfer of the charges, which comprises means for injecting into all of its stages a second driver charge (Q_2) and means permitting transfer of these second driver charges into the input diodes (5) of the memory (4).

14. Device according to one of claims 12 or 13, characterised in that the first (Q_1) and the second (Q_2) driver charges are equal.

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