

Description

Title of Invention: TIME SYNCHRONIZATION DEVICE, TIME
SYNCHRONIZATION SYSTEM, AND TIME SYNCHRONIZATION METHOD

5 Technical Field

[0001] The present invention relates to a time synchronization device, a time
synchronization system, and a time synchronization method.

Background Art

10 [0002] In the field of process automation (PA), achievement of wide area smart
communication by shifting from a closed network configuration to an open network
configuration, applying new information technologies, and the like have been promoted.
Smart grids are taken for example. For measurement and control of numerous devices,
there have been demands for time synchronization with high accuracy to simplify event
15 synchronization and data correlation.

[0003] In a closed network configuration, times of a relatively small number, such as
several tens, of devices are synchronized by a unique time synchronization scheme.
The time synchronization accuracy is in microseconds. To improve the time
synchronization accuracy, a time synchronization scheme is implemented mainly on a
20 hardware basis.

[0004] The IEEE (Institute of Electrical and Electronics Engineers) has established
the time synchronization standard IEEE 1588 using Ethernet (registered trademark) as a
time synchronization scheme that can be used in an open network configuration. IEEE
1588 defines a method of synchronizing time by transmitting and receiving
25 synchronization frames containing time recorded therein via a network.

Implementation of IEEE 1588 is classified into two types, which are hardware-based implementation and software-based implementation.

[0005] In hardware-based implementation, a hardware timestamping function of a PHY, which performs processing on a physical layer in the Open Systems

5 Interconnection (OSI) reference model, is used for recording time (refer to Patent Literature 1, for example). Thus, a time transmitting side records a timestamp, as transmission time, when a PHY transmits a synchronization frame, and transmits the recorded transmission time. Similarly, a time receiving side records a timestamp, as reception time, when a PHY receives a synchronization frame, and uses the recorded
10 reception time in an application program. The time synchronization accuracy is one nanosecond in theory, but is actually up to about 100 nanoseconds.

[0006] In software-based implementation, a software timestamping function of an application program, which performs processing on an application layer of the OSI reference model, is used to record time. Thus, a time transmitting side records a

15 timestamp, as transmission time, when the application program instructs a lower process to transmit a synchronization frame, and transmits the recorded transmission time. Similarly, a time receiving side records a timestamp, as reception time, when the application program is informed of reception of a synchronization frame by a lower process, and uses the recorded reception time in the application program. The time
20 synchronization accuracy is degraded to about 100 milliseconds in the worst case. Note that the time synchronization accuracy in the software-based implementation varies widely depending on the operating system (OS) on which the application program runs and the hierarchical structure of communication functions.

Patent Literature

[0007] Patent Literature 1: JP 2012-256965 A

Summary of Invention

5 Technical Problem

[0008] For changing a system from a closed network configuration to an open network configuration, the system is connected to another system. In terms of resource diversion, an existing time synchronization scheme may continue to be used for time synchronization in the system, and IEEE 1588 may be used for time
10 synchronization with the outside of the system. In this case, however, a terminal supporting both the existing time synchronization scheme and IEEE 1588 is required. In a case where IEEE 1588 is newly introduced, use of the hardware-based implementation will provide a high time synchronization accuracy but will cost enormously. Thus, in terms of cost saving, use of software-based implementation is
15 desirable.

[0009] An object of the present invention is to improve the time synchronization accuracy of a time synchronization scheme in software-based implementation.

Solution to Problem

[0010] A time synchronization device according to one aspect of the present
20 invention includes:
a reception unit to receive first data from a master device having a master clock;
a transmission unit to transmit second data to the master device after the first data are received by the reception unit;
25 a recording unit to record reception time of the first data at the reception unit

and transmission time of the second data at the transmission unit by using a slave clock that is a software clock;

a correction unit to correct the reception time of the first data and the transmission time of the second data recorded by the recording unit; and

5 a synchronization unit to calculate an offset from at least transmission time of the first data at the master device reported from the master device, reception time of the first data corrected by the correction unit, transmission time of the second data corrected by the correction unit, and reception time of the second data at the master device reported from the master device, the offset being a time lag between the master clock
10 and the slave clock.

Advantageous Effects of Invention

[0011] In the present invention, since time recorded with use of a software clock is corrected, the time synchronization accuracy of the time synchronization scheme in software-based implementation is improved.

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Brief Description of Drawings

[0012] Fig. 1 is a diagram illustrating an example configuration of a time synchronization system according to a first embodiment.

Fig. 2 is a block diagram illustrating configurations of a master device and a
20 time synchronization device according to the first embodiment.

Fig. 3 is a flowchart illustrating operation of the time synchronization system according to the first embodiment.

Fig. 4 is a flowchart illustrating operation of the time synchronization system according to the first embodiment.

25 Fig. 5 is a flowchart illustrating operation of the time synchronization system

according to the first embodiment.

Fig. 6 is a block diagram illustrating example implementation of the master device and the time synchronization device according to the first embodiment.

Fig. 7 is a sequence diagram illustrating a communication procedure between the master device and the time synchronization device according to the first embodiment.

Fig. 8 is a diagram illustrating an example configuration of a time synchronization system according to a second embodiment.

Fig. 9 is a diagram illustrating an example configuration of a time synchronization system according to a third embodiment.

Fig. 10 is a diagram illustrating an example hardware configuration of a time synchronization device according to the embodiments of the present invention.

Description of Embodiments

[0013] Embodiments of the present invention will now be described with reference to the drawings. Note that, in the drawings, the same or corresponding parts or components are represented by the same reference numerals. In the description of the embodiments, explanation of the same or corresponding parts will not be repeated or will be provided in a simplified manner as appropriate.

[0014] First Embodiment

A time synchronization scheme in conventional software-based implementation has a problem of degradation in the time synchronization accuracy as described above. Factors of this problem are variation in software timestamps and asymmetry of delay in internal processes of a terminal on which time synchronization is implemented. In the present embodiment, recorded values of time are corrected, so

that at least one or some of these factors are removed or inhibited.

[0015] The present embodiment achieves time synchronization in a distributed system in which a plurality of devices are present by software-based implementation.

In a time synchronization scheme in the software-based implementation according to
 5 the present embodiment, the principle of IEEE 1588 is used. This time synchronization scheme can be implemented in any terminal present in the distributed system. An OS installed in a terminal is a real-time OS. A terminal on a time transmitting side is a master. A terminal on a time receiving side is a slave, which performs time synchronization.

10 [0016] A configuration of a system according to the present embodiment, operation of the system according to the present embodiment, and effects of the present embodiment will now be described in this order.

[0017] *** Description of configuration ***

An example configuration of a time synchronization system 100 that is the
 15 system according to the present embodiment will be described with reference to Fig. 1.

[0018] The time synchronization system 100 is a distributed system. The time synchronization system 100 includes one grand master (GM) 110, a plurality of programmable logic controllers (PLCs) 120, and a plurality of field devices 130.

[0019] In this example, a tree network topology is used. The GM 110 is the root,
 20 and at least three PLCs 120 are connected to the GM 110 as nodes subordinate to the root. At least one PLC 120 or at least three field devices 130 are connected as further subordinate nodes, which constitute a subnetwork.

[0020] The GM 110 provides a time reference. A first time synchronization scheme
 101 is applied to time synchronization between the GM 110 and the PLCs 120
 25 connected to the GM 110. The first time synchronization scheme 101 is a time

synchronization scheme in the software-based implementation according to the present embodiment using the principle of IEEE 1588. A procedure of the time synchronization by the first time synchronization scheme 101 will be described below.

[0021] A second time synchronization scheme 102 is applied to time synchronization
 5 in each subnetwork. The second time synchronization scheme 102 is a time synchronization scheme unique to each subnetwork. Since any procedure may be applied to the procedure of the time synchronization by the second time synchronization scheme 102, description of the procedure will not be provided.

[0022] The PLCs 120 connected to the GM 110 support the second time
 10 synchronization scheme 102 of the respective subnetworks, and support the first time synchronization scheme 101.

[0023] Note that the number of PLCs 120 connected to the GM 110 and the configuration of each subnetwork can be changed where appropriate. The PLCs 120 may be replaced by another type of devices such as numeric controllers (NCs).

15 [0024] Configurations of a master device 200 and a time synchronization device 300 according to the present embodiment will be described with reference to Fig. 2.

[0025] The master device 200 has a master clock 201. The master clock 201 is not a hardware clock but is a software clock. A hardware clock is a clock mounted on hardware. A hardware clock is used for a hardware timestamping function. A
 20 software clock is a clock managed by software. A software clock is used for a software timestamping function.

[0026] The master device 200 includes a transmission unit 210, a reception unit 220, a recording unit 230, and a correction unit 240.

[0027] The GM 110 illustrated in Fig. 1 is a terminal on a time transmitting side in
 25 the first time synchronization scheme 101, and corresponds to the master device 200.

[0028] The time synchronization device 300 has a slave clock 301. Similarly to the master clock 201, the slave clock 301 is not a hardware clock but is a software clock.

[0029] The time synchronization device 300 includes a reception unit 310, a transmission unit 320, a recording unit 330, a correction unit 340, and a synchronization
5 unit 350.

[0030] The PLCs 120 connected to the GM 110 as illustrated in Fig. 1 are terminals on a time receiving side in the first time synchronization scheme 101, and each correspond to the time synchronization device 300.

[0031] The master device 200 and the time synchronization device 300 transmit and
10 receive data to/from each other via a network 400 according to a communication procedure of the first time synchronization scheme 101, which will now be described. This allows the time synchronization device 300 to set the time of the slave clock 301 to the time of the master clock 201.

[0032] The transmission unit 210 of the master device 200 transmits first data 401 to
15 the time synchronization device 300.

[0033] The reception unit 310 of the time synchronization device 300 receives the first data 401 from the master device 200.

[0034] The transmission unit 320 of the time synchronization device 300 transmits second data 402 to the master device 200 after the first data 401 are received by the
20 reception unit 310.

[0035] The reception unit 220 of the master device 200 receives the second data 402 from the time synchronization device 300.

[0036] The recording unit 230 of the master device 200 records transmission time of the first data 401 at the transmission unit 210 and reception time of the second data 402
25 at the reception unit 220 by using the master clock 201.

[0037] The correction unit 240 of the master device 200 corrects the transmission time of the first data 401 and the reception time of the second data 402 recorded by the recording unit 230.

[0038] The transmission unit 210 of the master device 200 transmits, to the time synchronization device 300, third data 403 for reporting at least the transmission time of the first data 401 corrected by the correction unit 240 and fourth data 404 for reporting at least the reception time of the second data 402 corrected by the correction unit 240. In this manner, the transmission unit 210 reports at least the transmission time of the first data 401 and the reception time of the second data 402 corrected by the correction unit 240 to the time synchronization device 300.

[0039] The reception unit 310 of the time synchronization device 300 receives the third data 403 and the fourth data 404 from the master device 200.

[0040] The recording unit 330 of the time synchronization device 300 records reception time of the first data 401 at the reception unit 310 and transmission time of the second data 402 at the transmission unit 320 by using the slave clock 301.

[0041] The correction unit 340 of the time synchronization device 300 corrects the reception time of the first data 401 and the transmission time of the second data 402 recorded by the recording unit 330.

[0042] The synchronization unit 350 of the time synchronization device 300 calculates an offset 405 from at least the transmission time of the first data 401 at the master device 200 reported from the master device 200, reception time of the first data 401 corrected by the correction unit 340, transmission time of the second data 402 corrected by the correction unit 340, and the reception time of the second data 402 at the master device 200 reported from the master device 200. The offset 405 is a time lag between the master clock 201 and the slave clock 301. For calculation of the offset

405, the synchronization unit 350 refers to the third data 403 and the fourth data 404 received by the reception unit 310. That is, the synchronization unit 350 obtains the transmission time of the first data 401 at the master device 200 from the third data 403 received by the reception unit 310. The synchronization unit 350 obtains the reception
5 time of the second data 402 at the master device 200 from the fourth data 404 received by the reception unit 310.

[0043] In the present embodiment, the third data 403 are data for reporting not only the transmission time of the first data 401 corrected by the correction unit 240 of the master device 200 but also the transmission time of the first data 401 recorded by the
10 recording unit 230 of the master device 200. The fourth data 404 are data for reporting not only the reception time of the second data 402 corrected by the correction unit 240 but also the reception time of the second data 402 recorded by the recording unit 230. That is, in the present embodiment, the transmission unit 210 of the master device 200 further reports the transmission time of the first data 401 and the reception time of the
15 second data 402 recorded by the recording unit 230 to the time synchronization device 300. Thus, for calculation of the offset 405, the synchronization unit 350 of the time synchronization device 300 uses both of the transmission time of the first data 401 recorded by the recording unit 230 of the master device 200 and the transmission time of the first data 401 corrected by the correction unit 240 of the master device 200 as the
20 transmission time of the first data 401 at the master device 200 reported from the master device 200. Furthermore, for calculation of the offset 405, the synchronization unit 350 of the time synchronization device 300 uses both of the reception time of the second data 402 recorded by the recording unit 230 of the master device 200 and the reception time of the second data 402 corrected by the correction unit 240 of the master
25 device 200 as the reception time of the second data 402 at the master device 200

reported from the master device 200.

[0044] In the present embodiment, for calculation of the offset 405, the synchronization unit 350 uses not only the reception time of the first data 401 corrected by the correction unit 340 but also the reception time of the first data 401 recorded by the recording unit 330. Furthermore, for calculation of the offset 405, the synchronization unit 350 uses not only the transmission time of the second data 402 corrected by the correction unit 340 but also the transmission time of the second data 402 recorded by the recording unit 330.

[0045] That is, in the present embodiment, the synchronization unit 350 calculates the offset 405 from the transmission time of the first data 401 recorded at the master device 200, the transmission time of the first data 401 corrected at the master device 200, the reception time of the first data 401 recorded by the recording unit 330, the reception time of the first data 401 corrected by the correction unit 340, the transmission time of the second data 402 recorded by the recording unit 330, the transmission time of the second data 402 corrected by the correction unit 340, the reception time of the second data 402 recorded at the master device 200, and the reception time of the second data 402 corrected at the master device 200.

[0046] Specifically, the synchronization unit 350 calculates the offset 405 from the difference between the sum of the transmission time of the first data 401 recorded at the master device 200 and the transmission time of the first data 401 corrected at the master device 200 and the sum of the reception time of the first data 401 recorded by the recording unit 330 and the reception time of the first data 401 corrected by the correction unit 340, and the difference between the sum of the transmission time of the second data 402 recorded by the recording unit 330 and the transmission time of the second data 402 corrected by the correction unit 340 and the sum of the reception time

of the second data 402 recorded at the master device 200 and the reception time of the second data 402 corrected at the master device 200.

[0047] Note that the third data 403 may be data for reporting only the transmission time of the first data 401 recorded by the recording unit 230 of the master device 200.

- 5 The fourth data 404 may be data for reporting only the reception time of the second data 402 recorded by the recording unit 230. Thus, the master device 200 may not include the correction unit 240.

- [0048] In a case where the master device 200 does not include the correction unit 240 or in a case where the correction unit 240 does not correct the transmission time of the
10 first data 401 recorded by the recording unit 230, the correction unit 340 of the time synchronization device 300 may correct the transmission time of the first data 401 at the master device 200 reported from the master device 200. In this case, the synchronization unit 350 of the time synchronization device 300 can use transmission time of the first data 401 corrected by the correction unit 340 together with the
15 transmission time of the first data 401 at the master device 200 reported from the master device 200, for calculation of the offset 405.

- [0049] In the case where the master device 200 does not include the correction unit 240 or in a case where the correction unit 240 does not correct the reception time of the second data 402 recorded by the recording unit 230, the correction unit 340 of the time
20 synchronization device 300 may correct the reception time of the second data 402 at the master device 200 reported from the master device 200. In this case, the synchronization unit 350 of the time synchronization device 300 can use reception time of the second data 402 corrected by the correction unit 340 together with the reception time of the second data 402 at the master device 200 reported from the master device
25 200, for calculation of the offset 405.

[0050] *** Description of operation ***

Operation of the time synchronization system 100 will be described with reference to Figs. 3, 4 and 5. The operation of the time synchronization system 100 corresponds to a time synchronization method according to the present embodiment.

5 [0051] Fig. 3 illustrates operation relating to transmission and reception of the first data 401. In the present embodiment, the transmission and reception of the first data 401 are repeated.

[0052] In step S11, the transmission unit 210 of the master device 200 repeatedly transmits the first data 401 to the time synchronization device 300.

10 [0053] In step S12, the reception unit 310 of the time synchronization device 300 repeatedly receives the first data 401 from the master device 200.

[0054] In step S13, each time the first data 401 are transmitted by the transmission unit 210, the recording unit 230 of the master device 200 records the transmission time of the first data 401 at the transmission unit 210 by using the master clock 201.

15 [0055] In step S14, each time the transmission time of the first data 401 is recorded by the recording unit 230, the correction unit 240 of the master device 200 generates a random number, and uses the generated random number to calculate a corrected value of the transmission time of the first data 401 recorded by the recording unit 230.

20 [0056] In step S15, the transmission unit 210 of the master device 200 transmits, as the third data 403, data for reporting the corrected value of the transmission time of the first data 401 calculated by the correction unit 240 to the time synchronization device 300.

[0057] In step S16, the reception unit 310 of the time synchronization device 300 repeatedly receives the third data 403 from the master device 200.

25 [0058] In step S17, each time the first data 401 are received by the reception unit 310,

the recording unit 330 of the time synchronization device 300 records the reception time of the first data 401 at the reception unit 310 by using the slave clock 301.

[0059] In step S18, each time the reception time of the first data 401 is recorded by the recording unit 330, the correction unit 340 of the time synchronization device 300
5 generates a random number, and uses the generated random number to calculate a corrected value of the reception time of the first data 401 recorded by the recording unit 330.

[0060] As will be described below, for calculation of the offset 405, the synchronization unit 350 of the time synchronization device 300 uses the corrected
10 value of the reception time of the first data 401 calculated by the correction unit 340 as the reception time of the first data 401.

[0061] Fig. 4 illustrates operation relating to transmission and reception of the second data 402. In the present embodiment, the transmission and reception of the second data 402 are also repeated.

15 [0062] In step S21, each time the first data 401 are received by the reception unit 310, the transmission unit 320 of the time synchronization device 300 transmits the second data 402 to the master device 200.

[0063] In step S22, the reception unit 220 of the master device 200 repeatedly receives the second data 402 from the time synchronization device 300.

20 [0064] In step S23, each time the second data 402 are received by the reception unit 220, the recording unit 230 of the master device 200 records the reception time of the second data 402 at the reception unit 220 by using the master clock 201.

[0065] In step S24, each time the reception time of the second data 402 is recorded by the recording unit 230, the correction unit 240 of the master device 200 generates a
25 random number, and uses the generated random number to calculate a corrected value

of the reception time of the second data 402 recorded by the recording unit 230.

[0066] In step S25, the transmission unit 210 of the master device 200 transmits, as the fourth data 404, data for reporting the corrected value of the reception time of the second data 402 calculated by the correction unit 240 to the time synchronization device
5 300.

[0067] In step S26, the reception unit 310 of the time synchronization device 300 repeatedly receives the fourth data 404 from the master device 200.

[0068] In step S27, each time the second data 402 are transmitted by the transmission unit 320, the recording unit 330 of the time synchronization device 300 records the
10 transmission time of the second data 402 at the transmission unit 320 by using the slave clock 301.

[0069] In step S28, each time the transmission time of the second data 402 is recorded by the recording unit 330, the correction unit 340 of the time synchronization device 300 generates a random number, and uses the generated random number to
15 calculate a corrected value of the transmission time of the second data 402 recorded by the recording unit 330.

[0070] As will be described below, for calculation of the offset 405, the synchronization unit 350 of the time synchronization device 300 uses the corrected value of the transmission time of the second data 402 calculated by the correction unit
20 340 as the transmission time of the second data 402.

[0071] In the present embodiment, a communication procedure of sequentially transmitting and receiving the first data 401, the second data 402, the third data 403 and the fourth data 404 one by one is repeated as described above.

[0072] Fig. 5 illustrates operation of calculating the offset 405.

25 [0073] In step S31, each time the first data 401 are received by the reception unit 310,

the synchronization unit 350 of the time synchronization device 300 calculates the offset 405. That is, the synchronization unit 350 calculates one offset 405 in each communication procedure.

[0074] In step S32, the synchronization unit 350 of the time synchronization device 300 accumulates calculated values of the offset 405. That is, the synchronization unit 350 accumulates two or more offsets 405 associated with two or more respective communication procedures.

[0075] In step S33, the synchronization unit 350 of the time synchronization device 300 performs statistical processing on the accumulated calculated values. The synchronization unit 350 adjusts the time of the slave clock 301 according to a result of the statistical processing. Specifically, the synchronization unit 350 uses an average of the accumulated calculated values as the result of the statistical processing to adjust the time of the slave clock 301. Consequently, the time of the master clock 201 and the time of the slave clock 301 are synchronized with each other.

[0076] In the present embodiment, the principle of IEEE 1588 is used as described above. That is, the first data 401, the second data 402, the third data 403, and the fourth data 404 are transmitted and received as synchronization frames. Specifically, the first data 401 are transmitted and received as a Sync message, the second data 402 are transmitted and received as a Follow_Up message, the third data 403 are transmitted and received as a Delay_Req message, and the fourth data 404 are transmitted and received as a Delay_Resp message.

[0077] If the one-way delay between the master device 200 and the time synchronization device 300 is assumed to be a half of the two-way delay, a value obtained by the following corresponds to the one-way delay: subtracting the sum of the transmission time of the first data 401 recorded at the master device 200 and the

transmission time of the first data 401 corrected at the master device 200, which are both reported by the third data 403, from the sum of the reception time of the first data 401 recorded by the recording unit 330 and the reception time of the first data 401 corrected by the correction unit 340; subtracting the sum of the transmission time of the second data 402 recorded by the recording unit 330 and the transmission time of the second data 402 corrected by the correction unit 340 from the sum of the reception time of the second data 402 recorded at the master device 200 and the reception time of the second data 402 corrected at the master device 200, which are both reported by the fourth data 404; and dividing the sum of the subtraction results by four. Then, a value obtained by the following corresponds to the offset 405: subtracting the sum of the transmission time of the first data 401 recorded at the master device 200 and the transmission time of the first data 401 corrected at the master device 200 from the sum of the reception time of the first data 401 recorded by the recording unit 330 and the reception time of the first data 401 corrected by the correction unit 340, and dividing the subtraction result by two; subtracting the sum of the transmission time of the second data 402 recorded by the recording unit 330 and the transmission time of the second data 402 corrected by the correction unit 340 from the sum of the reception time of the second data 402 recorded at the master device 200 and the reception time of the second data 402 corrected at the master device 200, and dividing the subtraction result by two; and subtracting the one-way delay from either one of the division results.

[0078] That is, when the offset 405 is represented by T_{offset} , the transmission time of the first data 401 recorded by the recording unit 230 of the master device 200 is represented by T_{m1} , the corrected value of T_{m1} is represented by T_{m1} ', the reception time of the first data 401 recorded by the recording unit 330 of the time synchronization device 300 is represented by T_{s1} , the corrected value of T_{s1} is

represented by T_{s1}' , the transmission time of the second data 402 recorded by the recording unit 330 of the time synchronization device 300 is represented by T_{s2} , the corrected value of T_{s2} is represented by T_{s2}' , the reception time of the second data 402 recorded by the recording unit 230 of the master device 200 is represented by T_{m2} , and the corrected value of T_{m2} is represented by T_{m2}' , $T_{offset} = ((T_{s1} + T_{s1}') - (T_{m1} + T_{m1'}))/2 - (((T_{s1} + T_{s1}') - (T_{m1} + T_{m1'})) + ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2'})))/4 = (((T_{s1} + T_{s1}') - (T_{m1} + T_{m1'})) - ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2'})))/4$, or $T_{offset} = ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2'}))/2 - (((T_{s1} + T_{s1}') - (T_{m1} + T_{m1'})) + ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2'})))/4 = -(((T_{s1} + T_{s1}') - (T_{m1} + T_{m1'})) - ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2'})))/4$. In step S31, such a calculation formula can be used to obtain the offset 405.

[0079] Note that a value obtained by the following may be regarded as the one-way delay: subtracting the transmission time of the first data 401 reported by the third data 403 from the reception time of the first data 401 corrected by the correction unit 340; subtracting the transmission time of the second data 402 corrected by the correction unit 340 from the reception time of the second data 402 reported by the fourth data 404; and dividing the sum of the subtraction results by two. In this case, a value obtained by the following corresponds to the offset 405: subtracting the transmission time of the first data 401 reported by the third data 403 from the reception time of the first data 401 corrected by the correction unit 340; subtracting the transmission time of the second data 402 corrected by the correction unit 340 from the reception time of the second data 402 reported by the fourth data 404; and subtracting the one-way delay from either one of the subtraction results.

[0080] That is, in step S31, the following calculation formula may be used to obtain the offset 405: $T_{offset} = (T_{s1}' - T_{m1'}) - ((T_{s1}' - T_{m1'}) + (T_{m2}' - T_{s2'}))/2 =$

$$((T_{s1}' - T_{m1}') - (T_{m2}' - T_{s2'}))/2, \text{ or } T_{\text{offset}} = (T_{m2}' - T_{s2'}) - ((T_{s1}' - T_{m1}') + (T_{m2}' - T_{s2'}))/2 = -((T_{s1}' - T_{m1}') - (T_{m2}' - T_{s2'}))/2.$$

[0081] Example implementation of the master device 200 and the time synchronization device 300 will be described with reference to Fig. 6.

5 [0082] The functions of the reception unit 310 and the transmission unit 320 of the time synchronization device 300 are implemented by a PHY 302 and a media access control (MAC) 303. The PHY 302 and the MAC 303 are hardware included in the time synchronization device 300. Specifically, the PHY 302 is a chip to perform processing on a physical layer in the OSI reference model, and the MAC 303 is a chip
10 to perform processing on a data link layer the OSI reference model. Note that the PHY 302 and the MAC 303 may be integrated on one chip.

[0083] Similarly, the functions of the transmission unit 210 and the reception unit 220 of the master device 200 are implemented by a PHY 202 and a MAC 203. The PHY 202 is a chip to perform processing on a physical layer, and the MAC 203 is a chip
15 to perform processing on a data link layer.

[0084] The functions of the recording unit 330 of the time synchronization device 300 are implemented by a MAC driver 304. The MAC driver 304 is software mounted on the time synchronization device 300. Specifically, the MAC driver 304 is middleware used by an OS 305 to control and operate the MAC 303. The MAC driver
20 304 has a software timestamping function of generating a timestamp by using the slave clock 301.

[0085] Similarly, the functions of the recording unit 230 of the master device 200 are implemented by a MAC driver 204. The MAC driver 204 is middleware used by an OS 205 to control and operate the MAC 203. The MAC driver 204 has a software
25 timestamping function of generating a timestamp by using the master clock 201.

[0086] The functions of the correction unit 340 and the synchronization unit 350 of the time synchronization device 300 are implemented by a time synchronization application 306. The time synchronization application 306 is software mounted on the time synchronization device 300. Specifically, the time synchronization application
 5 306 is an application program that runs on the OS 305 together with other applications 307. The time synchronization application 306 manages a correction table 308 to correct variation in timestamps generated by the MAC driver 304.

[0087] Similarly, the functions of the correction unit 240 of the master device 200 are implemented by the time synchronization application 206. The time synchronization
 10 application 206 is an application program that runs on the OS 205 together with other applications 207. The time synchronization application 206 manages a correction table 208 to correct variation in timestamps generated by the MAC driver 204.

[0088] The master device 200 that transmits time and the time synchronization device 300 that synchronizes time have the same hierarchical structure for time
 15 synchronization. The hierarchical structure is a three-layer structure including an application layer corresponding to the OSs 205 and 305 and the time synchronization applications 206 and 306, a data link layer corresponding to the MAC drivers 204 and 304 and the MACs 203 and 303, and a physical layer corresponding to the PHYs 202 and 302. Thus, in a time synchronization protocol according to the present
 20 embodiment, the data link layer is directly accessed from the application layer without a transport layer and a network layer in the OSI reference model.

[0089] Operation of the master device 200 and the time synchronization device 300 in the example illustrated in Fig. 6 will be explained with reference to Fig. 7.

[0090] In step S41 in which the master device 200 transmits a Sync message as a
 25 synchronization frame, the time synchronization application 206 generates a

synchronization frame that is a Sync message. The time synchronization application 206 does not store time in the synchronization frame. Upon detecting that the synchronization frame is generated by the time synchronization application 206, the OS 205 activates prioritized interruption to input the synchronization frame prior to other

5 frames to the MAC driver 204. The MAC driver 204 generates a software timestamp at the point when the synchronization frame is input, to record a transmission time T_{m1} of the synchronization frame. Thereafter, the MAC driver 204 inputs the synchronization frame to the MAC 203. The MAC 203 transmits the synchronization frame from the PHY 202. The MAC driver 204 feeds back the recorded transmission

10 time T_{m1} to the time synchronization application 206. The time synchronization application 206 stores the transmission time T_{m1} fed back from the MAC driver 204 in the first column among empty columns in the first row of the correction table 208. The time synchronization application 206 generates a random number following normal distribution, and stores the generated random number in the same column in the second

15 row of the correction table 208. The time synchronization application 206 corrects variation in the transmission time T_{m1} by subtracting the random number stored in the second row of the correction table 208 from the transmission time T_{m1} stored in the first row of the correction table 208. The time synchronization application 206 stores a corrected transmission time T_{m1}' in the same column in the third row of the correction

20 table 208. Note that the transmission time T_{m1} may be corrected in other manners such as adding the random number to the transmission time T_{m1} instead of subtracting the random number from the transmission time T_{m1} . Furthermore, the rows and the columns of the correction table 208 in which the transmission time T_{m1} , the random number, and the corrected transmission time T_{m1}' are to be stored can be changed as

25 appropriate.

[0091] In step S51 in which the time synchronization device 300 receives a Sync message as a synchronization frame, the PHY 302 receives the synchronization frame from the master device 200. The PHY 302 inputs the received synchronization frame to the MAC 303. The MAC driver 304 generates a software timestamp at the point
5 when it detects that the synchronization frame is input to the MAC 303, to record a reception time T_{s1} of the synchronization frame. Thereafter, the MAC driver 304 immediately inputs the recorded reception time T_{s1} to the time synchronization application 306. The time synchronization application 306 stores the reception time T_{s1} input from the MAC driver 304 in the first column among empty columns in the
10 first row of the correction table 308. The time synchronization application 306 generates a random number following normal distribution, and stores the generated random number in the same column in the second row of the correction table 308. The time synchronization application 306 corrects variation in the reception time T_{s1} by subtracting the random number stored in the second row of the correction table 308
15 from the reception time T_{s1} stored in the first row of the correction table 308. The time synchronization application 306 stores a corrected reception time T_{s1}' in the same column in the third row of the correction table 308. Note that the reception time T_{s1} may be corrected in other manners such as adding the random number to the reception time T_{s1} instead of subtracting the random number from the reception time T_{s1} .
20 Furthermore, the rows and the columns of the correction table 308 in which the reception time T_{s1} , the random number, and the corrected reception time T_{s1}' are to be stored can be changed as appropriate.

[0092] In step S42 in which the master device 200 transmits a Follow_Up message as a synchronization frame, the time synchronization application 206 generates a
25 synchronization frame that is a Follow_Up message. The time synchronization

application 206 stores, in the synchronization frame, a pair of uncorrected and corrected transmission times T_{m1} and T_{m1}' stored in the last column among the pairs of uncorrected and corrected transmission times T_{m1} and T_{m1}' stored in the first row and the third row, respectively, of the correction table 208, that is, the uncorrected and corrected transmission times T_{m1} and T_{m1}' of the last Sync message. Upon detecting that the synchronization frame is generated by the time synchronization application 206, the OS 205 activates prioritized interruption to input the synchronization frame prior to other frames to the MAC driver 204. The MAC driver 204 generates a software timestamp at the point when the synchronization frame is input.

10 The MAC driver 204, however, only detects that the synchronization frame is a Follow_Up message and temporarily holds the generated timestamp in a buffer or the like, and does not feed back the generated timestamp to the time synchronization application 206. Thereafter, the MAC driver 204 inputs the synchronization frame to the MAC 203. The MAC 203 transmits the synchronization frame from the PHY 202.

15 [0093] In step S52 in which the time synchronization device 300 receives a Follow_Up message as a synchronization frame, the PHY 302 receives a synchronization frame from the master device 200. The PHY 302 inputs the received synchronization frame to the MAC 303. The MAC driver 304 generates a software timestamp at the point when it detects that the synchronization frame is input to the

20 MAC 303. The MAC driver 304, however, only detects that the synchronization frame is a Follow_Up message and temporarily holds the generated timestamp in a buffer or the like, and does not input the generated timestamp to the time synchronization application 306. Thereafter, the MAC driver 304 inputs the synchronization frame to the time synchronization application 306 via the OS 305. The time synchronization

25 application 306 detects that the synchronization frame input from the MAC driver 304

is a Follow_Up message, and extracts the uncorrected and corrected transmission times T_{m1} and T_{m1}' stored in the synchronization frame.

[0094] In step S53 in which the time synchronization device 300 transmits a

Delay_Req message as a synchronization frame, the time synchronization application

5 306 generates a synchronization frame that is a Delay_Req message. The time synchronization application 306 does not store time in the synchronization frame.

Upon detecting that the synchronization frame is generated by the time synchronization application 306, the OS 305 activates prioritized interruption to input the

synchronization frame prior to other frames to the MAC driver 304. The MAC driver

10 304 generates a software timestamp at the point when the synchronization frame is input,

to record a transmission time T_{s2} of the synchronization frame. Thereafter, the MAC

driver 304 inputs the synchronization frame to the MAC 303. The MAC 303 transmits

the synchronization frame from the PHY 302. The MAC driver 304 feeds back the

recorded transmission time T_{s2} to the time synchronization application 306. The

15 time synchronization application 306 stores the transmission time T_{s2} fed back from the MAC driver 304 in the first column among empty columns in the fourth row of the correction table 308. The time synchronization application 306 generates a random

number following normal distribution, and stores the generated random number in the same column in the fifth row of the correction table 308. The time synchronization

20 application 306 corrects variation in the transmission time T_{s2} by subtracting the random number stored in the fifth row of the correction table 308 from the transmission time T_{s2} stored in the fourth row of the correction table 308. The time

synchronization application 306 stores a corrected transmission time T_{s2}' in the same column in the sixth row of the correction table 308. Note that the transmission time

25 T_{s2} may be corrected in other manners such as adding the random number to the

transmission time T_{s2} instead of subtracting the random number from the transmission time T_{s2} . Furthermore, the rows and the columns of the correction table 308 in which the transmission time T_{s2} , the random number, and the corrected transmission time T_{s2}' are to be stored can be changed as appropriate.

- 5 [0095] In step S43 in which the master device 200 receives a Delay_Req message as a synchronization frame, the PHY 202 receives a synchronization frame from the time synchronization device 300. The PHY 202 inputs the received synchronization frame to the MAC 203. The MAC driver 204 generates a software timestamp at the point when it detects that the synchronization frame is input to the MAC 203, to record a
- 10 reception time T_{m2} of the synchronization frame. Thereafter, the MAC driver 204 immediately inputs the recorded reception time T_{m2} to the time synchronization application 206. The time synchronization application 206 stores the reception time T_{m2} input from the MAC driver 204 in the first column among empty columns in the fourth row of the correction table 208. The time synchronization application 206
- 15 generates a random number following normal distribution, and stores the generated random number in the same column in the fifth row of the correction table 208. The time synchronization application 206 corrects variation in the reception time T_{m2} by subtracting the random number stored in the fifth row of the correction table 208 from the reception time T_{m2} stored in the fourth row of the correction table 208. The time
- 20 synchronization application 206 stores a corrected reception time T_{m2}' in the same column in the sixth row of the correction table 208. Note that the reception time T_{m2} may be corrected in other manners such as adding the random number to the reception time T_{m2} instead of subtracting the random number from the reception time T_{m2} . Furthermore, the rows and the columns of the correction table 208 in which the
- 25 reception time T_{m2} , the random number, and the corrected reception time T_{m2}' are to

be stored can be changed as appropriate.

- [0096] In step S44 in which the master device 200 transmits a Delay_Resp message as a synchronization frame, the time synchronization application 206 generates a synchronization frame that is a Delay_Resp message. The time synchronization
- 5 application 206 stores, in the synchronization frame, a pair of uncorrected and corrected reception times T_{m2} and T_{m2}' stored in the last column among the pairs of uncorrected and corrected reception times T_{m2} and T_{m2}' stored in the fourth row and the sixth row, respectively, of the correction table 208, that is, the uncorrected and corrected reception times T_{m2} and T_{m2}' of the last Delay_Req message. Upon
- 10 detecting that the synchronization frame is generated by the time synchronization application 206, the OS 205 activates prioritized interruption to input the synchronization frame prior to other frames to the MAC driver 204. The MAC driver 204 generates a software timestamp at the point when the synchronization frame is input. The MAC driver 204, however, only detects that the synchronization frame is a
- 15 Delay_Resp message and temporarily holds the generated timestamp in a buffer or the like, and does not feed back the generated timestamp to the time synchronization application 206. Thereafter, the MAC driver 204 inputs the synchronization frame to the MAC 203. The MAC 203 transmits the synchronization frame from the PHY 202.
- [0097] In step S54 in which the time synchronization device 300 receives a
- 20 Delay_Resp message as a synchronization frame, the PHY 302 receives a synchronization frame from the master device 200. The PHY 302 inputs the received synchronization frame to the MAC 303. The MAC driver 304 generates a software timestamp at the point when it detects that the synchronization frame is input to the MAC 303. The MAC driver 304, however, only detects that the synchronization frame
- 25 is a Delay_Resp message and temporarily holds the generated timestamp in a buffer or

the like, and does not input the generated timestamp to the time synchronization application 306. Thereafter, the MAC driver 304 inputs the synchronization frame to the time synchronization application 306 via the OS 305. The time synchronization application 306 detects that the synchronization frame input from the MAC driver 304 is a Delay_Resp message, and extracts the uncorrected and corrected reception times T_{m2} and T_{m2}' stored in the synchronization frame.

[0098] After step S54, the time synchronization application 306 calculates the offset 405 by using the uncorrected and corrected reception times T_{s1} and T_{s1}' stored in the first row and the third row of the correction table 308 in step S51, the uncorrected and corrected transmission times T_{m1} and T_{m1}' extracted in step S52, the uncorrected and corrected transmission times T_{s2} and T_{s2}' stored in the fourth row and the sixth row of the correction table 308 in step S53, and the uncorrected and corrected reception times T_{m2} and T_{m2}' extracted in step S54. The following calculation formula as described above can be used, but another formula may alternatively be used: $T_{offset} = (((T_{s1} + T_{s1}') - (T_{m1} + T_{m1}')) - ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2}')))/4$, or $T_{offset} = -(((T_{s1} + T_{s1}') - (T_{m1} + T_{m1}')) - ((T_{m2} + T_{m2}') - (T_{s2} + T_{s2}')))/4$.

[0099] Subsequently, the procedure from step S41 to step S44 and the procedure from step S51 to step S54 are repeated.

20 [0100] *** Description of effects ***

In the present embodiment, since time recorded with use of a software clock is corrected, the time synchronization accuracy of the time synchronization scheme in software-based implementation is improved.

[0101] Second Embodiment

25 The description of the present embodiment will focus on differences from the

first embodiment.

[0102] An example configuration of a time synchronization system 100 according to the present embodiment will be described with reference to Fig. 8.

[0103] In this example, the same tree network topology as that in the example
5 illustrated in Fig. 1 is used.

[0104] While the second time synchronization scheme 102 is applied to the time synchronization in all the subnetworks in the first embodiment, a first time synchronization scheme 101 is applied to time synchronization in one or some subnetworks in the present embodiment.

10 [0105] Thus, one or some PLCs 120 out of PLCs 120 connected to the GM 110 are also terminals on a time transmitting side in the first time synchronization scheme 101, and each correspond to both of a master device 200 and a time synchronization device 300. In addition, field devices 130 connected to the one or some PLCs 120 are terminals on a time receiving side in the first time synchronization scheme 101, and
15 each correspond to the time synchronization device 300.

[0106] Configurations and operation of the master device 200 and the time synchronization device 300 according to the present embodiment are the same as those in the first embodiment.

[0107] Third Embodiment

20 The description of the present embodiment will focus on differences from the first embodiment.

[0108] An example configuration of a time synchronization system 100 according to the present embodiment will be described with reference to Fig. 9.

[0109] In this example, a line network topology is partially used. Three PLCs 120
25 are connected in series with the GM 110. At least one PLC 120 or at least two field

devices 130 are subordinately connected to each of these three PLCs 120, which constitute tree subnetworks.

[0110] A first time synchronization scheme 101 is applied to time synchronization between the GM 110 and the PLCs 120 connected in series with the GM 110. The first
5 time synchronization scheme 101 is also applied to time synchronization between the PLCs 120 connected in series with the GM 110.

[0111] Thus, the two PLCs 120 in the middle among the PLCs 120 connected in series with the GM 110 are also terminals on a time transmitting side in the first time synchronization scheme 101, and each correspond to both of a master device 200 and a
10 time synchronization device 300. In this manner, the present embodiment is an embodiment in which the master functions are distributed to the GM 110 and the two PLCs 120.

[0112] Note that the two PLCs 120 in the middle among the PLCs 120 connected in series with the GM 110 may simply transfer synchronization frames transmitted and
15 received between the GM 110 and the other PLC 120 without serving as the terminals on the time transmitting side in the first time synchronization scheme 101. In this case, the two PLCs 120 in the middle each correspond only to the time synchronization device 300. In this manner, the present embodiment may be changed to an embodiment in which the master functions are integrated in the GM 110.

20 [0113] Configurations and operation of the master device 200 and the time synchronization device 300 according to the present embodiment are the same as those in the first embodiment.

[0114] An example hardware configuration of the time synchronization device 300 according to the embodiments of the present invention will now be described with
25 reference to Fig. 10.

[0115] The time synchronization device 300 is a computer. The time synchronization device 300 includes hardware components such as a processor 901, an auxiliary storage device 902, a memory 903, a communication device 904, an input interface 905, and a display interface 906. The processor 901 is connected to other
 5 hardware components via a signal line 910, and controls these hardware components. The input interface 905 is connected to an input device 907. The display interface 906 is connected to a display 908.

[0116] The processor 901 is an integrated circuit (IC) to perform processing. The processor 901 is a central processing unit (CPU), a digital signal processor (DSP), or a
 10 graphics processing unit (GPU), for example.

[0117] The auxiliary storage device 902 is a recording medium such as a read only memory (ROM), a flash memory, or a hard disk drive (HDD).

[0118] The memory 903 is a random access memory (RAM), for example.

[0119] The communication device 904 includes a receiver 921 to receive data and a
 15 transmitter 922 to transmit data. The communication device 904 is a communication chip or a network interface card (NIC), for example.

[0120] The input interface 905 is a port to which a cable 911 of the input device 907 is connected. The input interface 905 is a universal serial bus (USB) terminal, for example.

20 [0121] The display interface 906 is a port to which a cable 912 of the display 908 is connected. The display interface 906 is an USB terminal or a high definition multimedia interface (HDMI (registered trademark)) terminal, for example.

[0122] The input device 907 is a mouse, a stylus, a keyboard, or a touch panel, for example.

25 [0123] The display 908 is a liquid crystal display (LCD), for example.

[0124] The auxiliary storage device 902 stores programs to implement the functions of the “units” such as the reception unit 310, the transmission unit 320, the recording unit 330, the correction unit 340, and the synchronization unit 350. The programs are loaded into the memory 903, read by the processor 901, and executed by the processor 901. The auxiliary storage device 902 also stores the OS. At least part of the OS is loaded into the memory 903, and the processor 901 executes the programs to implement the functions of the “units” while executing the OS.

[0125] While one processor 901 is illustrated in Fig. 10, the time synchronization device 300 may include a plurality of processors 901. The plurality of processors 901 may then execute the programs to implement the functions of the “units” in cooperation with one another.

[0126] Information, data, signal values, and variable values representing results of processing performed by the “units” are stored in the auxiliary storage device 902, the memory 903, or a register or a cache memory in the processor 901.

[0127] The “units” may alternatively be provided in the form of “circuitry”. Alternatively, a “unit” may be replaced by a “circuit”, a “step”, a “procedure”, or a “process”. The “circuit” and “circuitry” are concepts including not only the processor 901 but also other types of processing circuits such as a logic IC, a gate array (GA), an application specific integrated circuit (ASIC), and a field-programmable gate array (FPGA).

[0128] Note that the hardware configuration illustrated in Fig. 10 is also applicable to the master device 200 according to the embodiments of the present invention.

[0129] Embodiments of the present invention have been described above; some of the embodiments may be combined to be carried out. Alternatively, any one or more of the embodiments may be partially carried out. For example, any one of the “units”

described in the embodiments may be used, or any combination of some of the “units” may be used. Note that the present invention is not limited to the embodiments, but various modifications may be made thereto where necessary.

5 Reference Signs List

- [0130] 100: time synchronization system, 101: first time synchronization scheme, 102: second time synchronization scheme, 110: GM, 120: PLC, 130: field device, 200: master device, 201: master clock, 202: PHY, 203: MAC, 204: MAC driver, 205: OS, 206: time synchronization application, 207: other application, 208: correction table, 210: transmission unit, 220: reception unit, 230: recording unit, 240: correction unit, 300: time synchronization device, 301: slave clock, 302: PHY, 303: MAC, 304: MAC driver, 305: OS, 306: time synchronization application, 307: other application, 308: correction table, 310: reception unit, 320: transmission unit, 330: recording unit, 340: correction unit, 350: synchronization unit, 400: network, 401: first data, 402: second data, 403: third data, 404: fourth data, 405: offset, 901: processor, 902: auxiliary storage device, 903: memory, 904: communication device, 905: input interface, 906: display interface, 907: input device, 908: display, 910: signal line, 911: cable, 912: cable, 921: receiver, 922: transmitter

Claims

[Claim 1] A time synchronization device comprising:

a reception unit to receive first data from a master device having a master clock;

5 a transmission unit to transmit second data to the master device after the first data are received by the reception unit;

a recording unit to record reception time of the first data at the reception unit and transmission time of the second data at the transmission unit by using a slave clock that is a software clock;

10 a correction unit to correct the reception time of the first data and the transmission time of the second data recorded by the recording unit; and

a synchronization unit to calculate an offset from a difference between a sum of transmission time of the first data recorded at the master device and transmission time of the first data corrected at the master device, which are both reported from the master device, and a sum of the reception time of the first data recorded by the
15 recording unit and reception time of the first data corrected by the correction unit, and a difference between a sum of the transmission time of the second data recorded by the recording unit and transmission time of the second data corrected by the correction unit and a sum of reception time of the second data recorded at the master device and
20 reception time of the second data corrected at the master device, which are both reported from the master device, the offset being a time lag between the master clock and the slave clock.

[Claim 2] The time synchronization device according to claim 1, wherein

the reception unit repeatedly receives the first data from the master device,
25 each time the first data are received by the reception unit, the recording unit

records the reception time of the first data at the reception unit,

each time the reception time of the first data is recorded by the recording unit, the correction unit generates a random number, and uses the generated random number to calculate a corrected value of the reception time of the first data recorded by the

5 recording unit, and

the synchronization unit uses the corrected value of the reception time of the first data calculated by the correction unit as the reception time of the first data for calculation of the offset.

[Claim 3] The time synchronization device according to claim 2, wherein

10 each time the first data are received by the reception unit, the transmission unit transmits the second data to the master device,

each time the second data are transmitted by the transmission unit, the recording unit records the transmission time of the second data at the transmission unit,

each time the transmission time of the second data is recorded by the
15 recording unit, the correction unit generates a random number, and uses the generated random number to calculate a corrected value of the transmission time of the second data recorded by the recording unit, and

the synchronization unit uses the corrected value of the transmission time of the second data calculated by the correction unit as the transmission time of the second
20 data for calculation of the offset.

[Claim 4] The time synchronization device according to claim 2 or 3, wherein each time the first data are received by the reception unit, the synchronization unit calculates the offset, accumulates calculated values of the offset, performs statistical processing on the accumulated calculated values, and adjusts time of the slave clock according to a result
25 of the statistical processing.

[Claim 5] The time synchronization device according to claim 4, wherein the synchronization unit uses an average of the accumulated calculated values as the result of the statistical processing to adjust the time of the slave clock.

[Claim 6] The time synchronization device according to any one of claims 1 to 5,

5 wherein

the reception unit receives third data for reporting the transmission time of the first data at the master device and fourth data for reporting the reception time of the second data at the master device from the master device, and

10 the synchronization unit refers to the third data and the fourth data received by the reception unit for calculation of the offset.

[Claim 7] A time synchronization system comprising:

the time synchronization device according to any one of claims 1 to 6; and
the master device to record transmission time of the first data and reception time of the second data by using the master clock that is a software clock, correct the
15 recorded transmission time of the first data and the recorded reception time of the second data, and report the recorded transmission time of the first data, the recorded reception time of the second data, corrected transmission time of the first data, and corrected reception time of the second data to the time synchronization device.

[Claim 8] A time synchronization method comprising:

20 transmitting first data from a master device having a master clock;
receiving the first data at a time synchronization device having a slave clock that is a software clock;
transmitting second data from the time synchronization device after receiving the first data;
25 receiving the second data at the master device;

recording transmission time of the first data and reception time of the second data by using the master clock, correcting the recorded transmission time of the first data and the recorded reception time of the second data, by the master device, and reporting the recorded transmission time of the first data, the recorded reception time of the second data, corrected transmission time of the first data, and corrected reception time of the second data from the master device; and

recording reception time of the first data and transmission time of the second data by using the slave clock, correcting the recorded reception time of the first data and the recorded transmission time of the second data, by the time synchronization device, and calculating an offset from a difference between a sum of the transmission time of the first data recorded at the master device and the transmission time of the first data corrected at the master device, which are reported from the master device, and a sum of the reception time of the first data recorded by the time synchronization device and reception time of the first data corrected by the time synchronization device, and a difference between a sum of the transmission time of the second data recorded by the time synchronization device and transmission time of the second data corrected by the time synchronization device and a sum of the reception time of the second data recorded at the master device and the reception time of the second data corrected at the master device, which are both reported from the master device, by the time synchronization device, the offset being a time lag between the master clock and the slave clock.