bonded surfaces between the divided wafers 81 and 82 and the monocrystalline SiC wafers 83 and 84. Thus, in consideration of the thickness of each of the device structures 88 and 91, each of the bonded surfaces between the divided wafers 81 and 82 and the monocrystalline SiC wafers 83 and 84 in the bonded wafers 85 and 86 is desirably located at a depth of 50 μm or more from the front surface of each of the bonded wafers 85 and 86, more desirably located at a position 80 μm deep therefrom, and most desirably located at a depth of 100 μm or more therefrom. In other words, the thickness of each of the divided wafers 81 and 82 is desirably 50 μm or more, more desirably 80 μm or more, and most desirably 100 μm or more. In this manner, the bonded surface is not included in each of the device-included wafers 93 and 94, and influence given to the device by the bonded surface can be removed.

[0108] According to the method described above, by using the monocrystalline SiC wafers 83 and 84 as support substrates, the device structures 88 and 91 can be formed on the plurality of divided wafers 81 and 82 divided from the SiC wafer. Further, the monocrystalline SiC wafers 83 and 84 divided from the bonded wafers 89 and 92 can be reused as support substrates for other divided wafers.

[0109] Note that the board thickness of each of the monocrystalline SiC wafers 83 and 84 divided from the bonded wafers 89 and 92 may be changed from the original board thickness of each of the monocrystalline SiC wafers 83 and 84. In other words, when each of the monocrystalline SiC wafers 83 and 84 is divided from the bonded wafers 89 and 92, each of the monocrystalline SiC wafers 83 and 84 need not be divided at each of the bonded surfaces between the divided wafers 81 and 82 and the monocrystalline SiC wafers 83 and 84. Further, each of the bonded surfaces may be removed by removing a damaged layer of each of the divided monocrystalline SiC wafers 83 and 84. Further, each of the bonded surfaces may remain in each of the divided monocrystalline SiC

CLAIMS

[Claim 1] A manufacturing method for a semiconductor device, the manufacturing method comprising the steps of:

(a) dividing each of a plurality of first wafers in a thickness direction to thereby obtain at least one first divided wafer not including a device structure from each of the plurality of first wafers;

(b) bonding a plurality of first divided wafers obtained from different first wafers among the plurality of first wafers to obtain a first bonded wafer being a bonded wafer; and

(c) forming the device structure on a front surface of the first bonded wafer.

[Claim 2] The manufacturing method for the semiconductor device according to claim 1, wherein

the step (a) is a step of dividing each of the first wafers on which the device structure is formed on the front surface into a first device-included wafer being a device-included wafer including the device structure and the at least one first divided wafer.

[Claim 3] The manufacturing method for the semiconductor device according to claim 1, further comprising the step of

(d) dividing the first bonded wafer on which the device structure is formed into a second device-included wafer being a device-included wafer including the device structure and at least one second divided wafer not including the device structure.

[Claim 4] The manufacturing method for the semiconductor device according to claim 3,

further comprising the step of

(e) after the step (d), repeating the step (b) to the step (d) at least once, with the second divided wafer being used as a new first divided wafer.

[Claim 5] The manufacturing method for the semiconductor device according to claim 1, wherein

at least one of the first wafers is a bonded wafer formed by bonding a plurality of wafers.

[Claim 6] The manufacturing method for the semiconductor device according to claim 3, wherein

when an original pre-divided wafer of the device-included wafer is the bonded wafer formed by bonding a plurality of wafers, the device-included wafer does not include a bonded surface included in an original pre-divided bonded wafer.

[Claim 7] The manufacturing method for the semiconductor device according to claim 6, wherein

a material of each of the first wafers is monocrystalline SiC.

[Claim 8] The manufacturing method for the semiconductor device according to claim 1, wherein

a thickness of the first divided wafer is 50 μm or more.

[Claim 9] The manufacturing method for the semiconductor device according to claim 1, wherein

the device structure is a SiC power device structure.

[Claim 10] A bonded wafer obtained by bonding a plurality of divided wafers that are divided from different wafers and do not include a device structure, wherein

a bonded surface of the plurality of divided wafers is present at a depth of 50 μm or more from a front surface.

[Claim 11] The bonded wafer according to claim 10, wherein

a material of each of the different wafers is monocrystalline SiC.

[Claim 12] A manufacturing method for a semiconductor device, the manufacturing method comprising the steps of:

(a) dividing a wafer not being a bonded wafer in a thickness direction to thereby obtain a divided wafer;

(b) after the step (a), bonding the divided wafer to a support substrate to obtain a bonded wafer; and

(c) after the step (b), forming a device structure on the bonded wafer.

[Claim 13] The manufacturing method for the semiconductor device according to claim 12, wherein

a bonded surface between the divided wafer and the support substrate in the bonded wafer is located at a depth of 50 μm or more from a front surface of the bonded wafer.

[Claim 14] The manufacturing method for the semiconductor device according to

claim 12 or 13, wherein

the support substrate is monocrystalline SiC, monocrystalline GaN or a polycrystalline substrate.

[Claim 15] A bonded wafer obtained by bonding a divided wafer that is divided from a wafer not being a bonded wafer and does not include a device structure to a support substrate, wherein

a bonded surface between the divided wafer and the support substrate is present at a depth of 50 μm or more from a front surface, and

a material of each of the wafer and the support substrate is monocrystalline SiC or monocrystalline GaN.