

ABSTRACT

A semiconductor device includes a substrate comprising a logic cell region and a peripheral region extending around the logic cell region, a logic device in the logic cell region and comprising a plurality of source/drain patterns, an upper active contact on and electrically connected to one of the source/drain patterns, a lower active contact below and electrically connected to another of the source/drain patterns, a conductive structure that penetrates the peripheral region of the substrate, a plurality of peripheral upper wiring lines in the peripheral region and connected to the conductive structure, and a plurality of peripheral lower wiring lines in the peripheral region and connected to the conductive structure opposite the peripheral upper wiring lines. A bottom surface of the conductive structure is lower than a bottom surface of the lower active contact, relative to a bottom surface of the substrate.

FIG. 5E