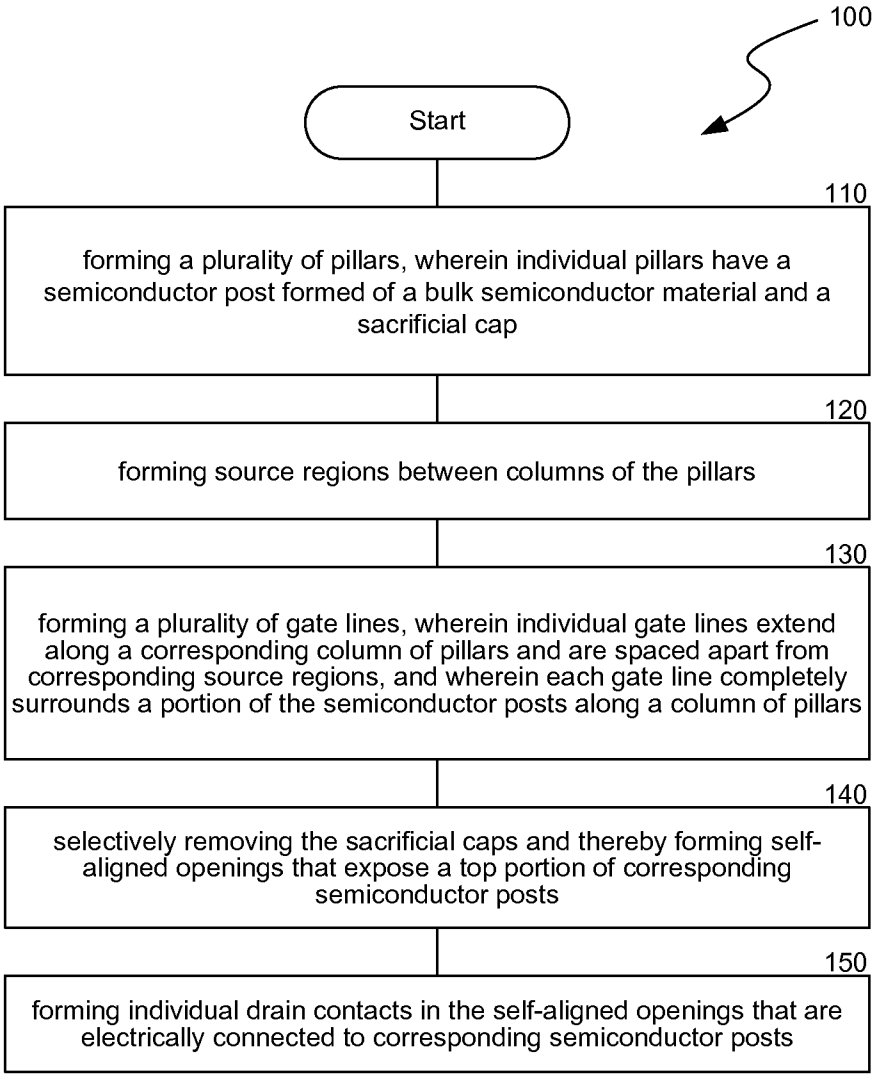

100
Start
110
forming a plurality of pillars, wherein individual pillars have a semiconductor post formed of a bulk semiconductor material and a sacrificial cap
120
forming source regions between columns of the pillars
130
forming a plurality of gate lines, wherein individual gate lines extend along a corresponding column of pillars and are spaced apart from corresponding source regions, and wherein each gate line completely surrounds a portion of the semiconductor posts along a column of pillars
140
selectively removing the sacrificial caps and thereby forming self-aligned openings that expose a top portion of corresponding semiconductor posts
150
forming individual drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts

FIG. 1

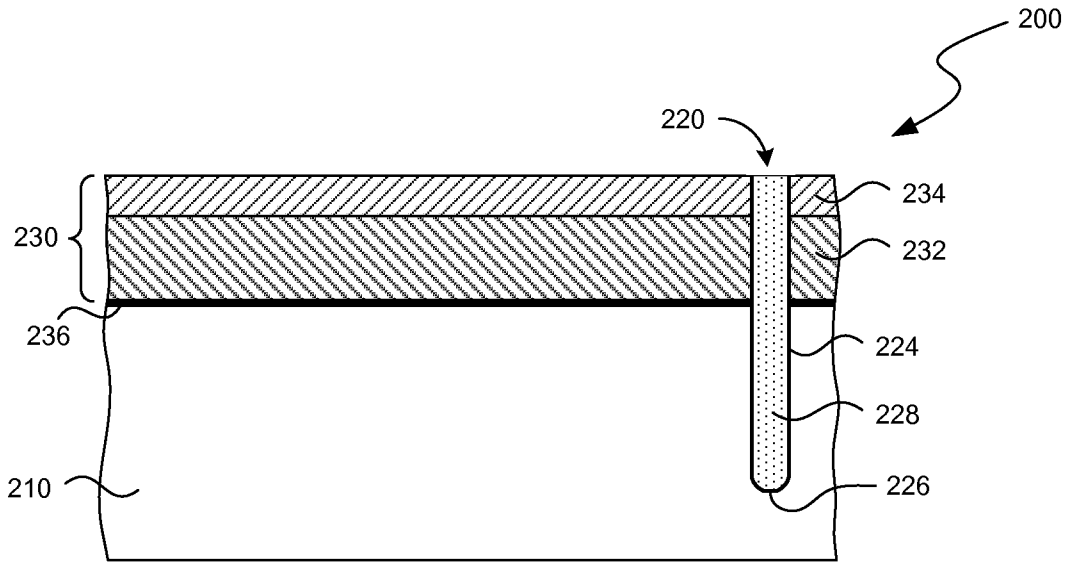

200
220
234
230
232
236
224
228
210
226

FIG. 2A

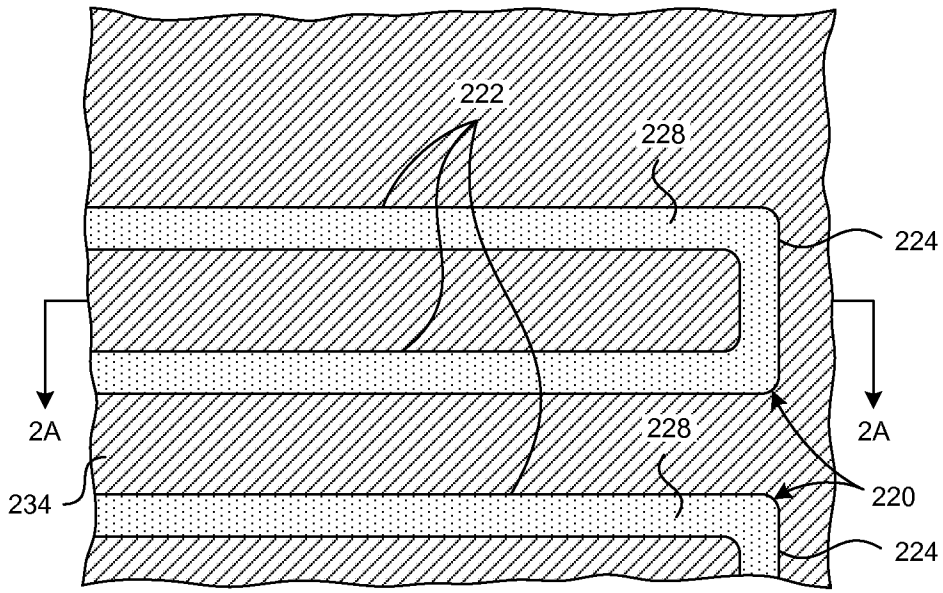

222
228
224
2A
2A
228
234
220
224

FIG. 2B

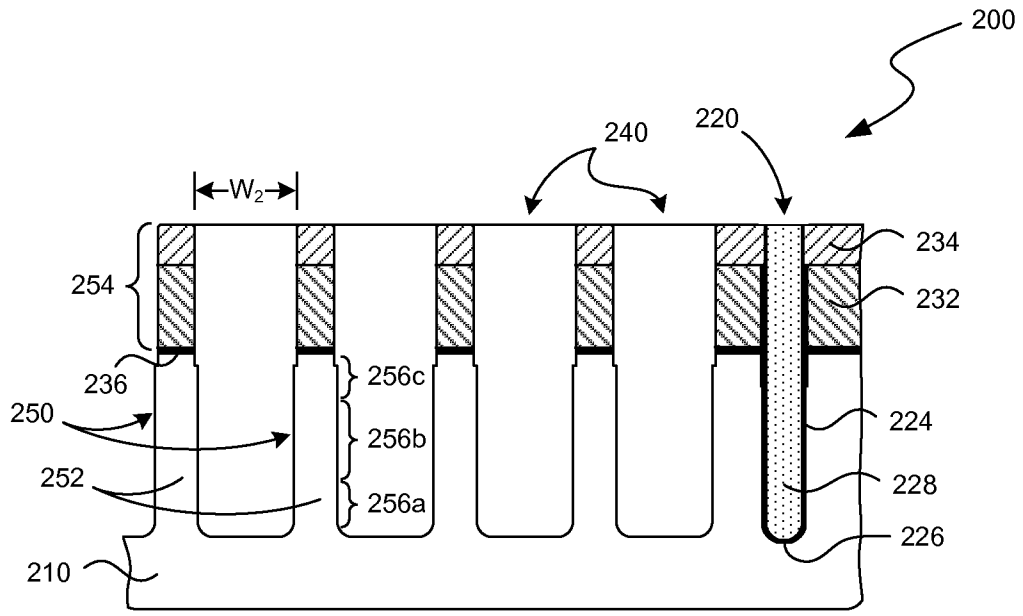

200
240
220
W_2
234
254
232
236
256c
250
256b
224
252
256a
228
226
210

FIG. 3A

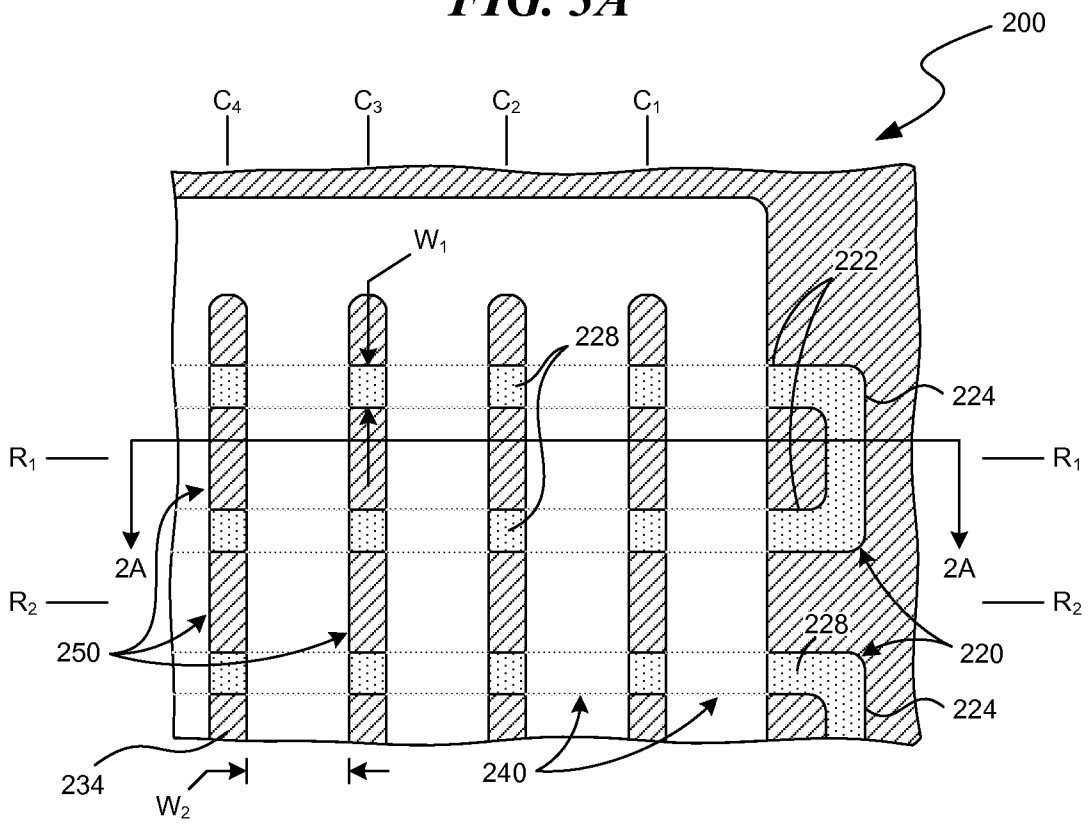

200
C_4
C_3
C_2
C_1
W_1
222
228
224
R_1
R_1
2A
2A
R_2
R_2
228
250
220
224
234
240
W_2

FIG. 3B

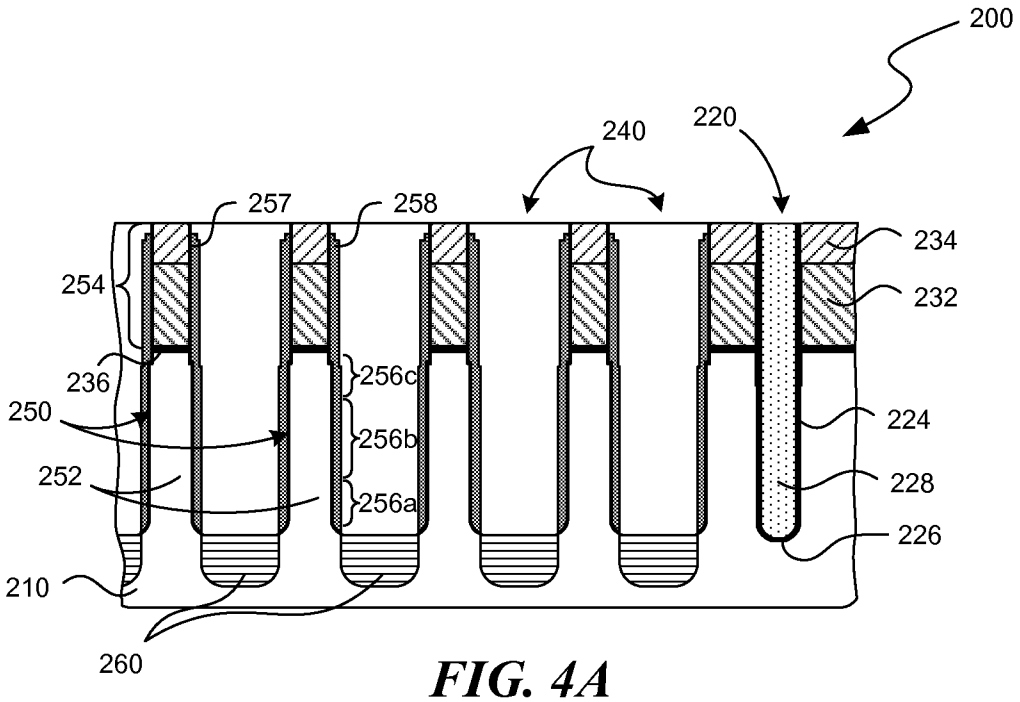

200
240
220
257
258
234
254
232
236
256c
250
256b
224
252
228
256a
226
210
260

FIG. 4A

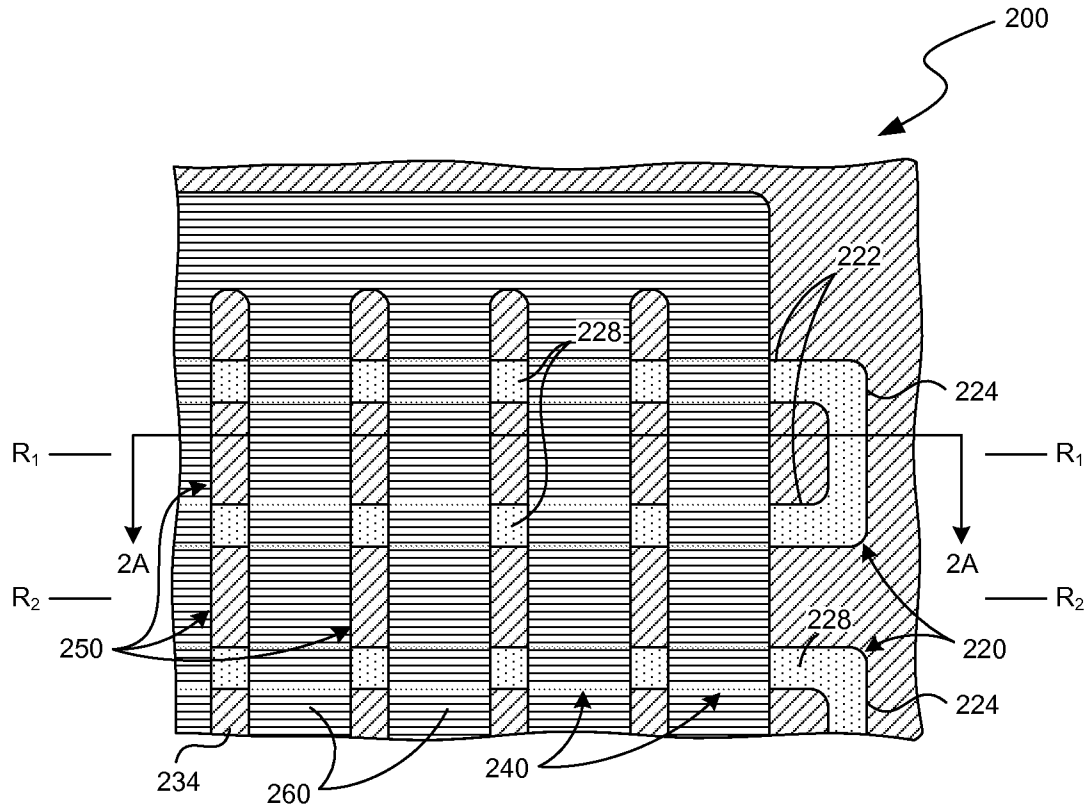

200
222
228
224
R_1
R_1
2A
2A
R_2
R_2
250
228
220
224
234
260
240

FIG. 4B

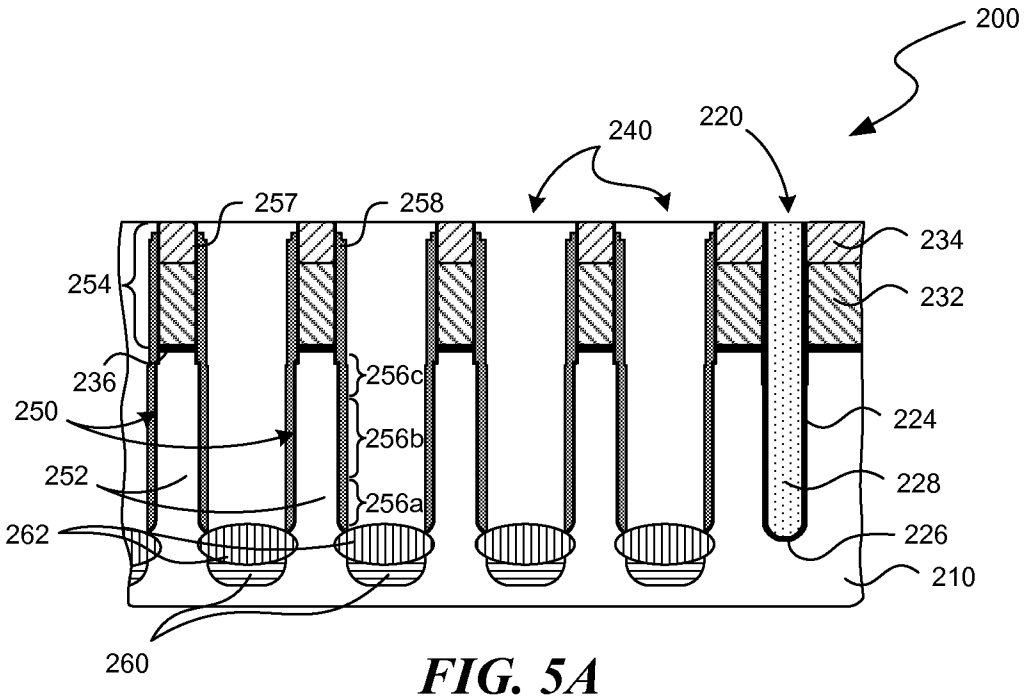

200
240
220
257
258
254
234
232
236
256c
250
256b
224
252
256a
228
262
226
210
260

FIG. 5A

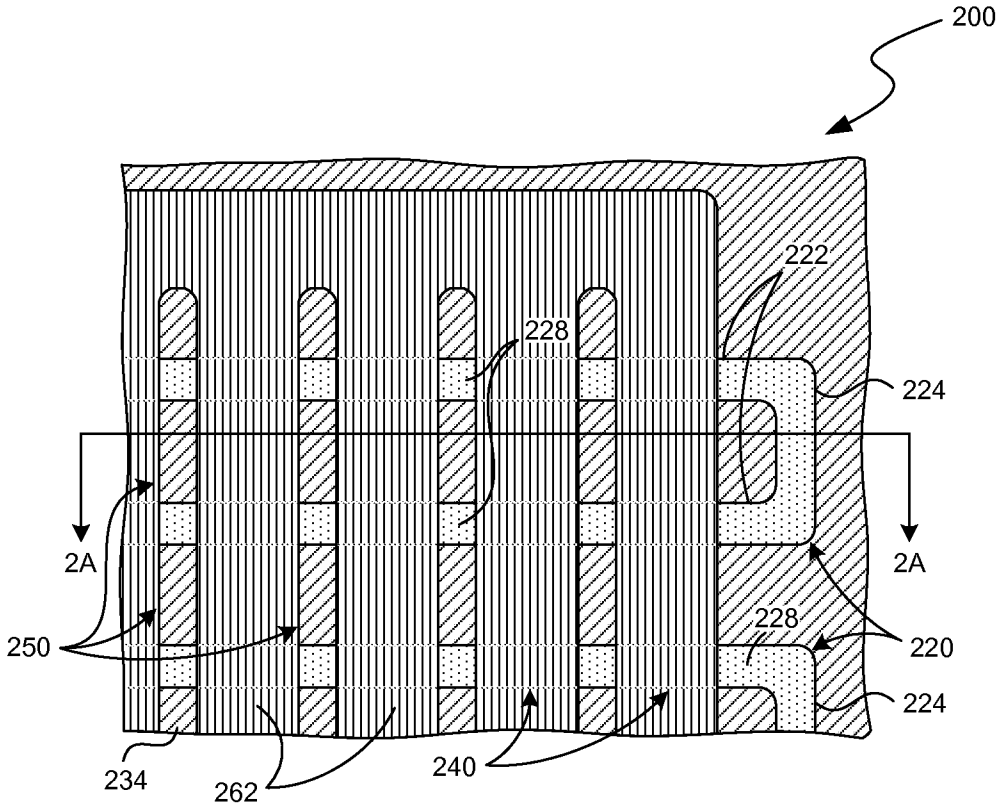

200
222
228
224
2A
2A
250
228
220
224
234
262
240

FIG. 5B

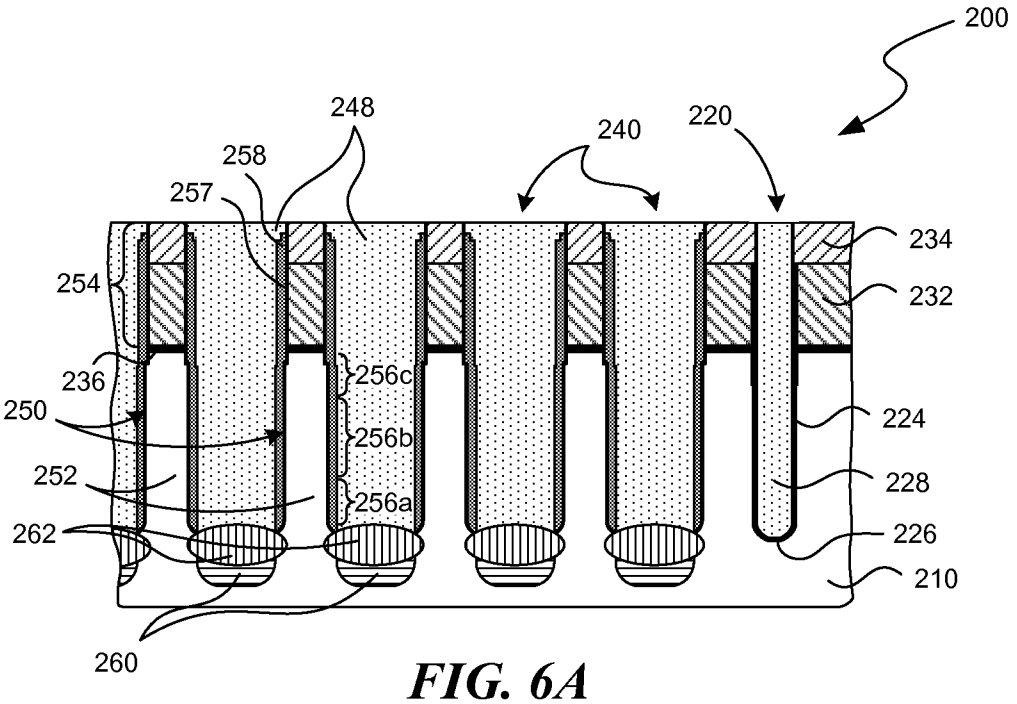

200
248
240
220
258
257
234
254
232
236
256c
250
256b
224
252
228
256a
262
226
210
260

FIG. 6A

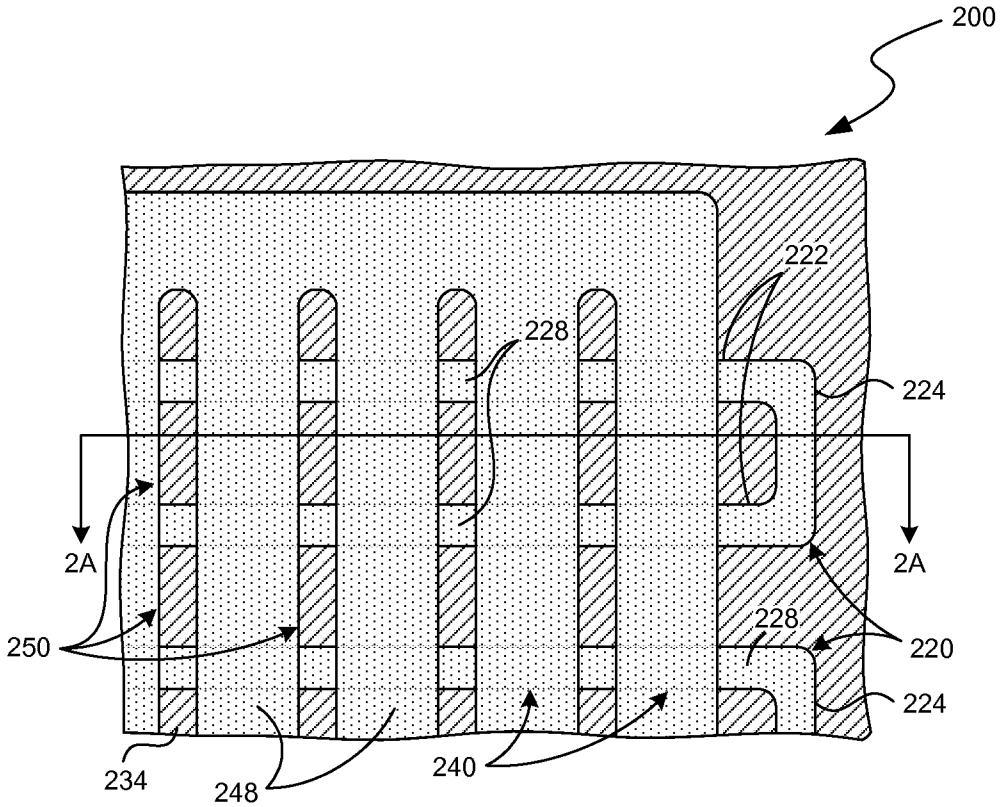

200
222
228
224
2A
2A
250
228
220
224
234
248
240

FIG. 6B

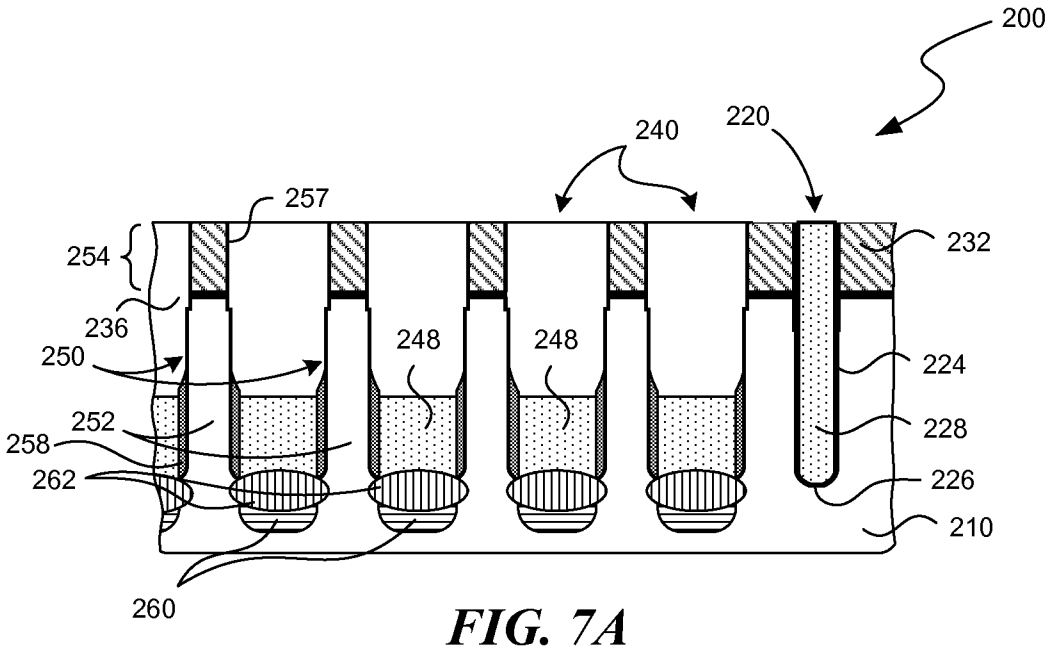

200
240
220
257
254
232
236
248
248
250
224
252
228
258
262
226
210
260

FIG. 7A

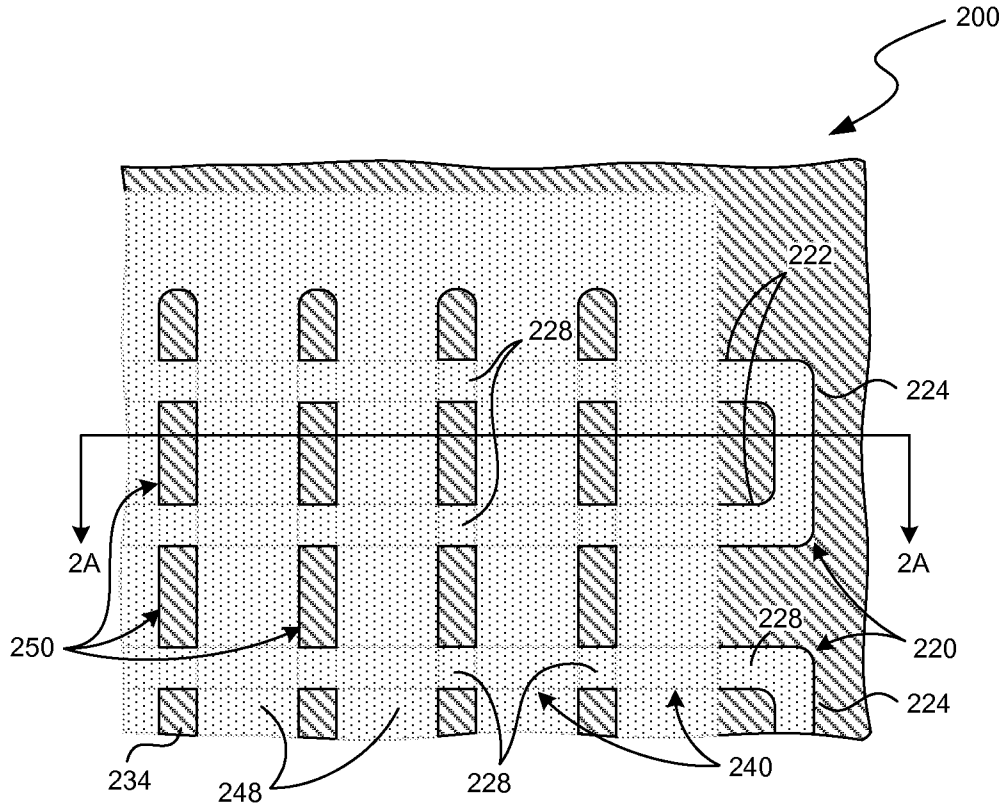

200
222
228
224
2A
2A
250
228
220
224
234
248
228
240

FIG. 7B

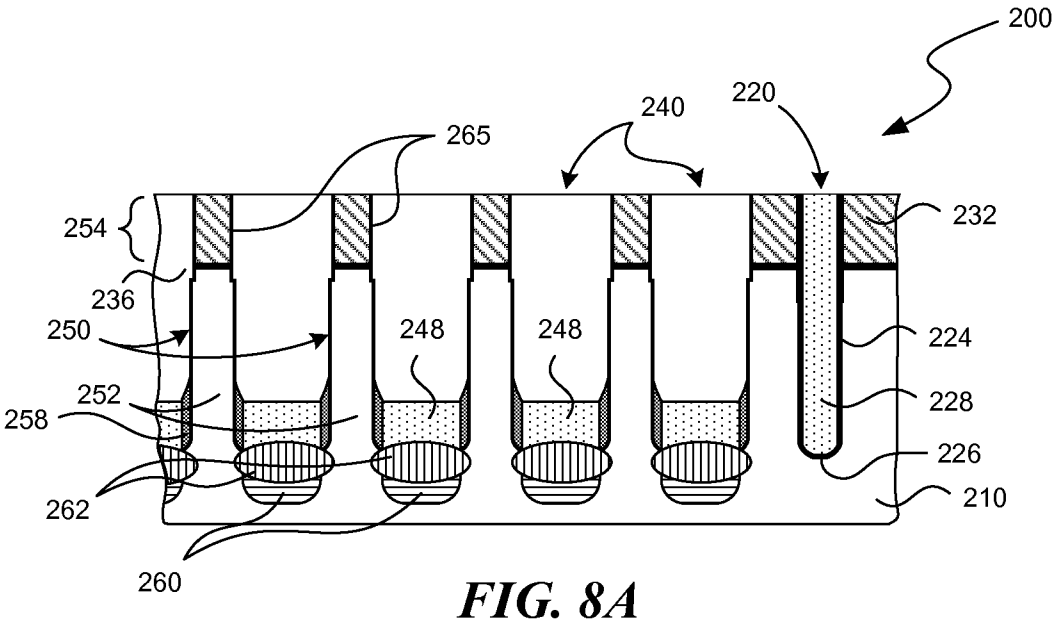

200
240
220
265
254
232
236
250
248
248
224
252
228
258
226
262
210
260

FIG. 8A

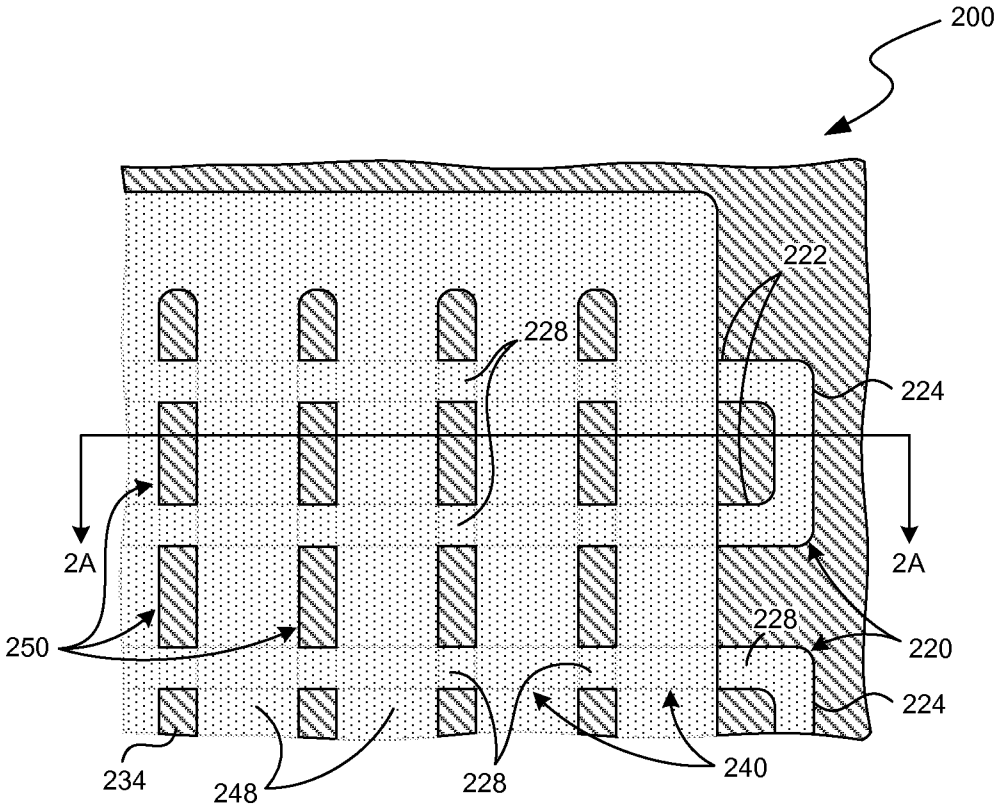

200
222
228
224
2A
2A
250
228
220
224
234
248
228
240

FIG. 8B

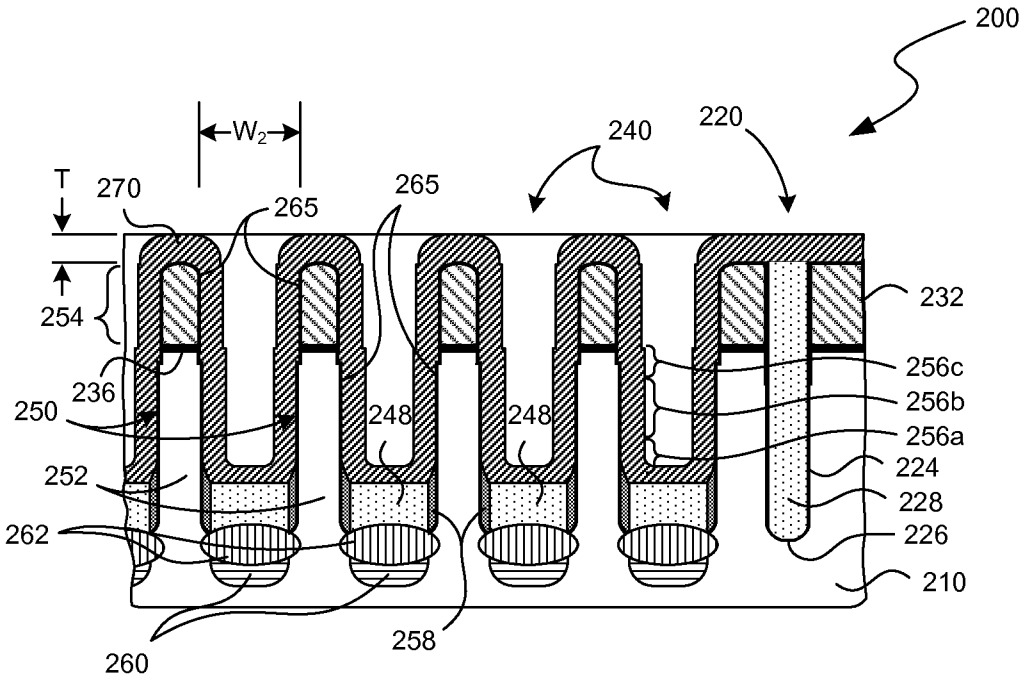

200
W_2
240
220
T
270
265
265
254
232
256c
236
256b
250
248
248
256a
224
252
228
262
226
210
260
258

FIG. 9A

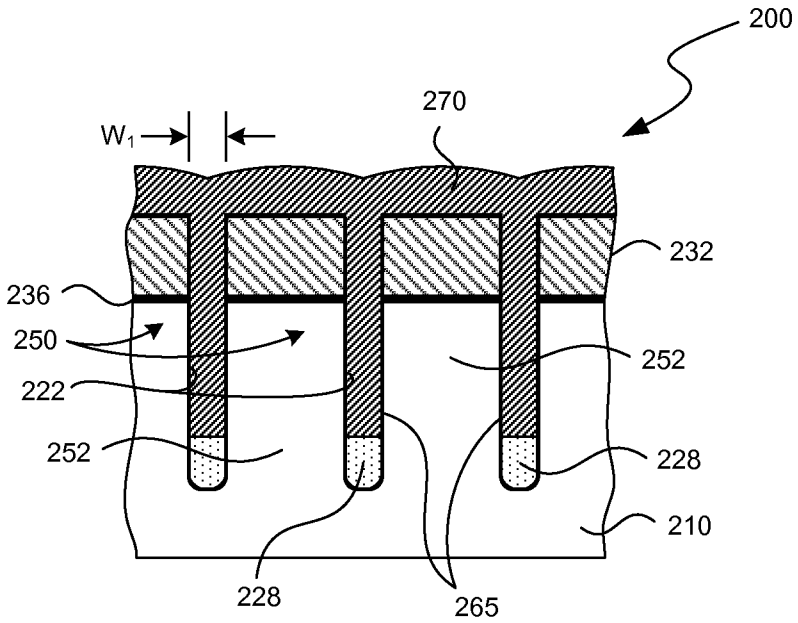

200
W_1
270
232
236
250
252
222
252
228
210
228
265

FIG. 9B

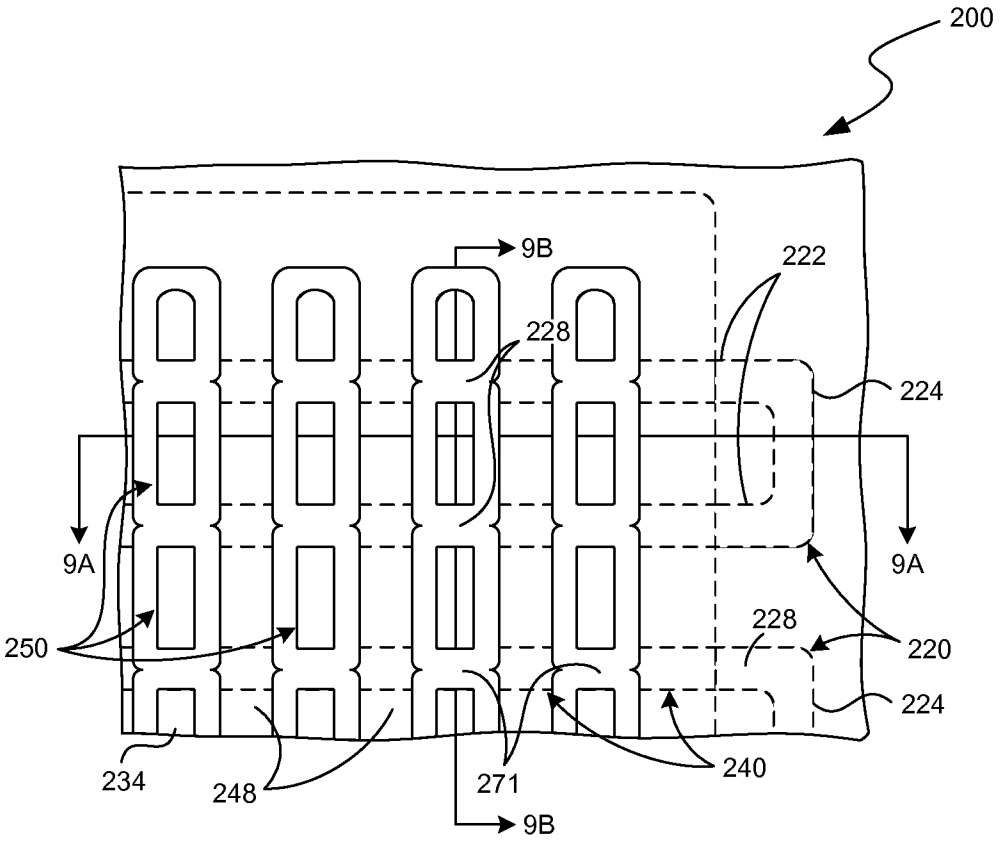


FIG. 9C

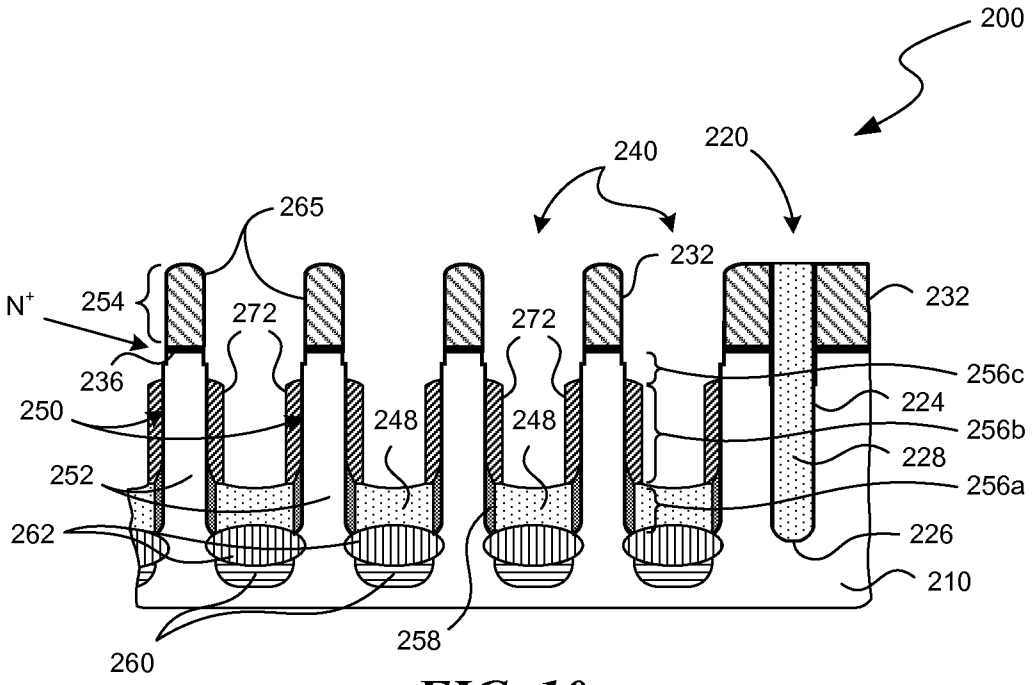

200
240
220
265
232
N+
254
272
272
232
236
256c
250
248
248
224
256b
252
228
256a
262
226
210
260
258

FIG. 10

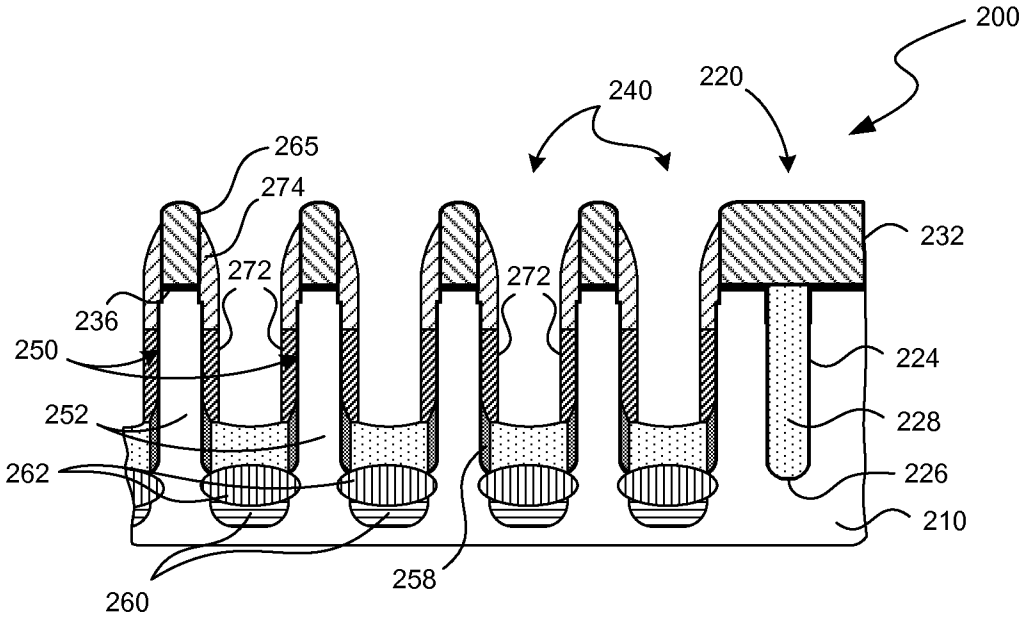

200
240
220
265
274
232
272
272
236
250
224
252
228
262
226
210
260
258

FIG. 11

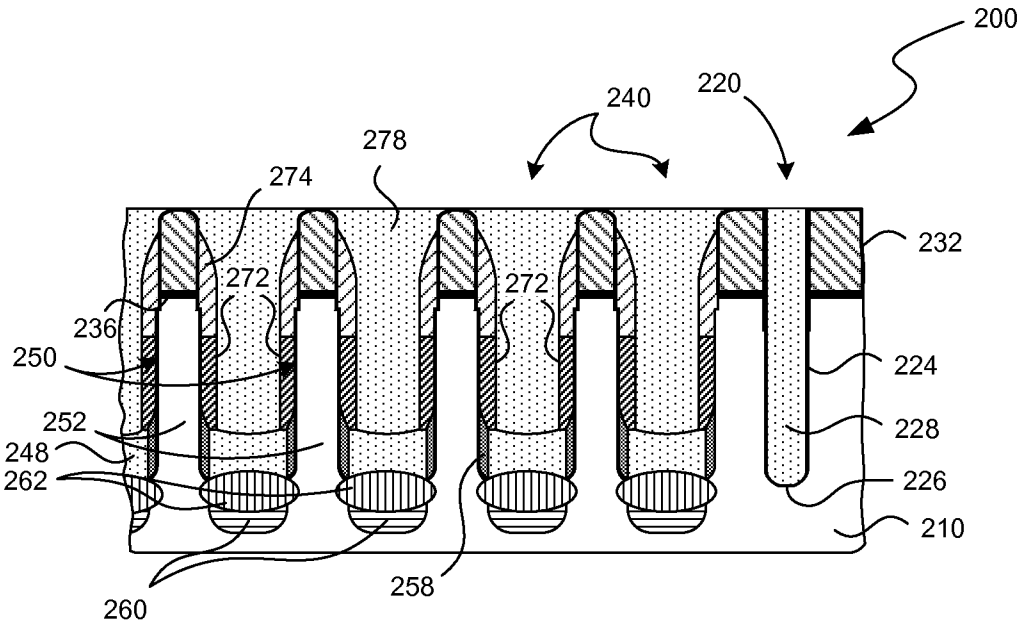

200
240
220
278
274
232
272
272
236
250
224
252
228
248
262
226
210
258
260

FIG. 12

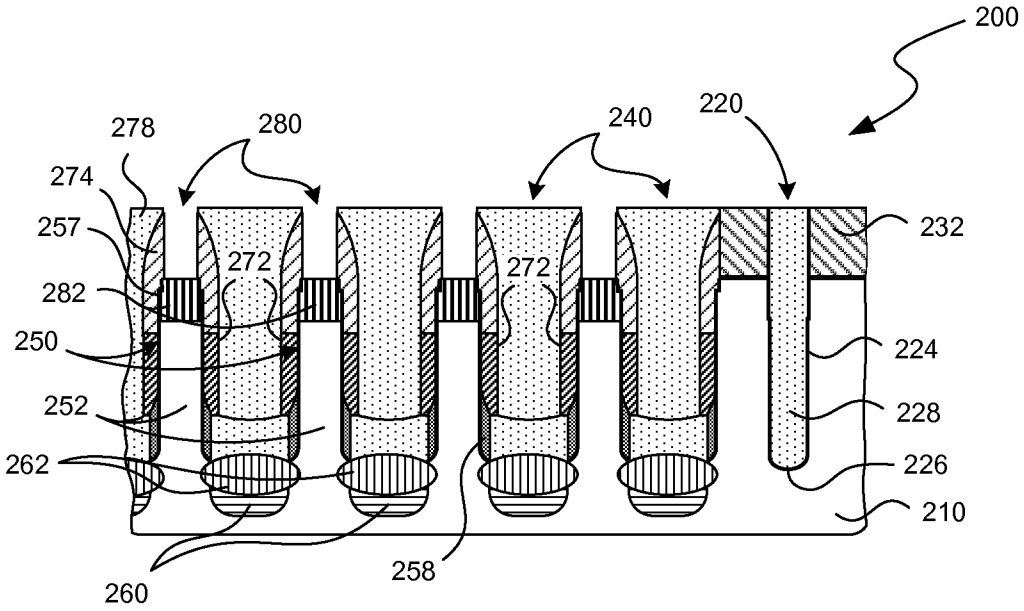

200
278
280
240
220
274
257
232
272
272
282
250
224
252
228
262
226
210
258
260

FIG. 13

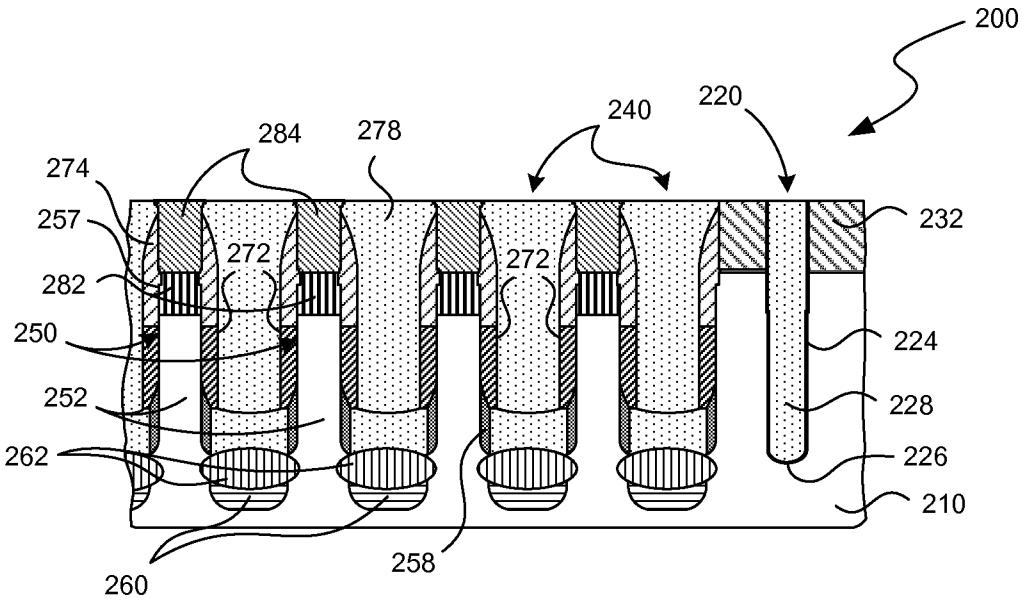

200
220
240
284
278
274
257
232
272
272
282
224
250
252
228
262
226
210
260
258

FIG. 14

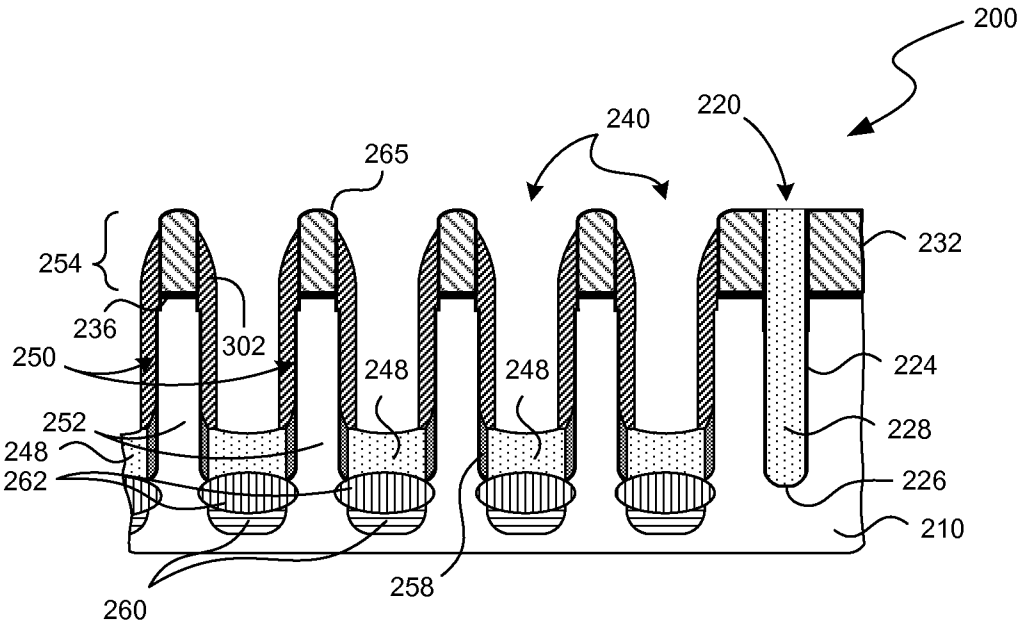

200
220
240
265
254
232
236
302
250
248
248
224
252
228
248
262
226
210
260
258

FIG. 15

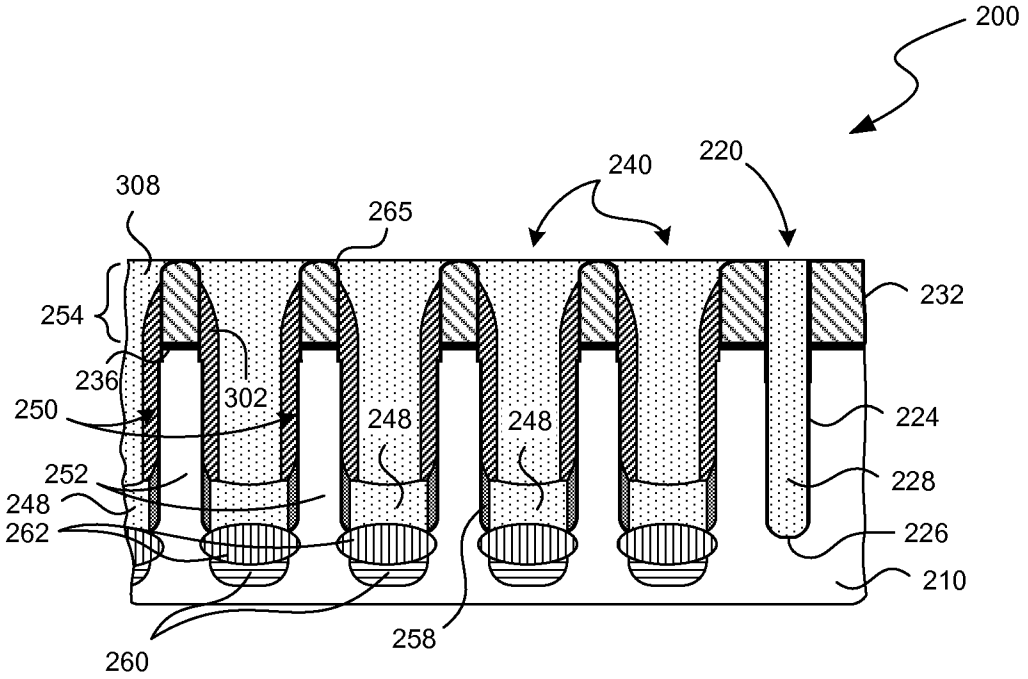

200
220
240
308
265
254
232
236
302
250
248
248
224
252
228
248
262
226
210
258
260

FIG. 16

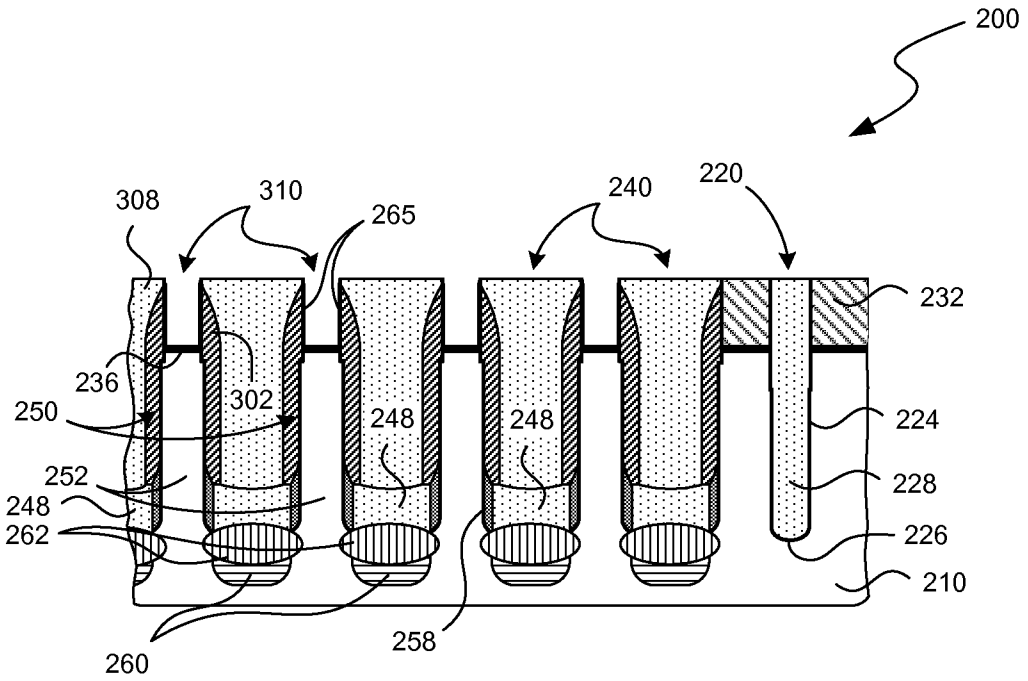

200
220
240
308
310
265
232
236
302
250
248
248
224
252
228
248
262
226
210
258
260

FIG. 17

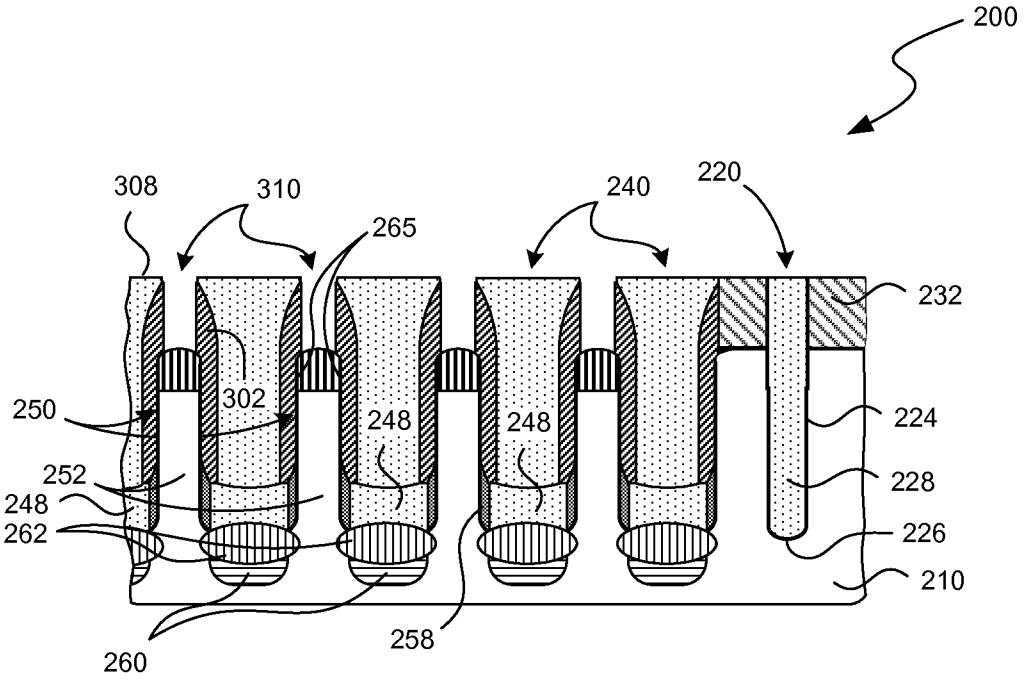

200
308
310
265
240
220
232
302
250
248
248
224
252
228
248
262
226
210
260
258

FIG. 18

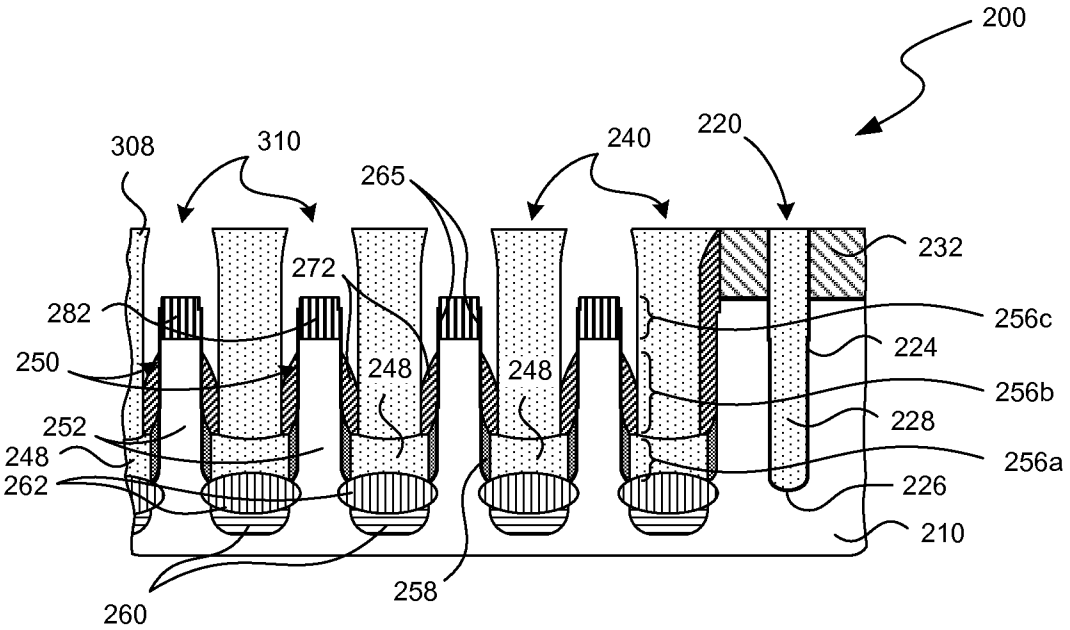

200
308
310
265
240
220
232
272
282
256c
250
248
248
224
256b
252
228
248
256a
262
226
210
260
258

FIG. 19

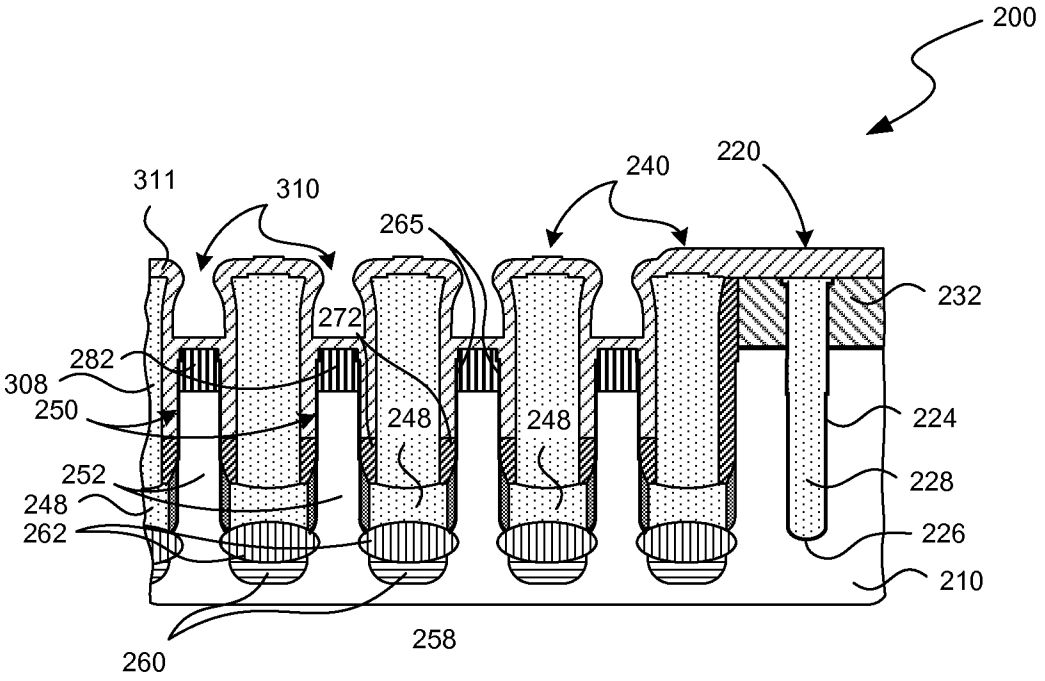

200
220
240
311
310
265
232
272
282
308
250
248
248
224
252
228
248
262
226
210
258
260

FIG. 20

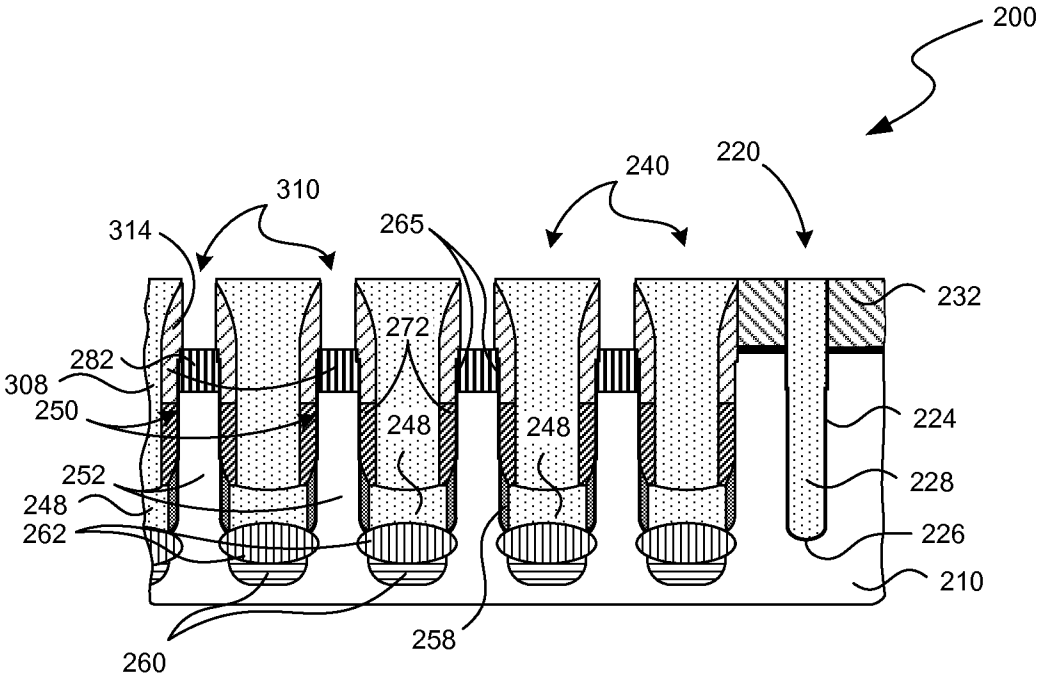

200
220
240
310
314
265
232
272
282
308
250
248
248
224
252
228
248
262
226
210
258
260

FIG. 21

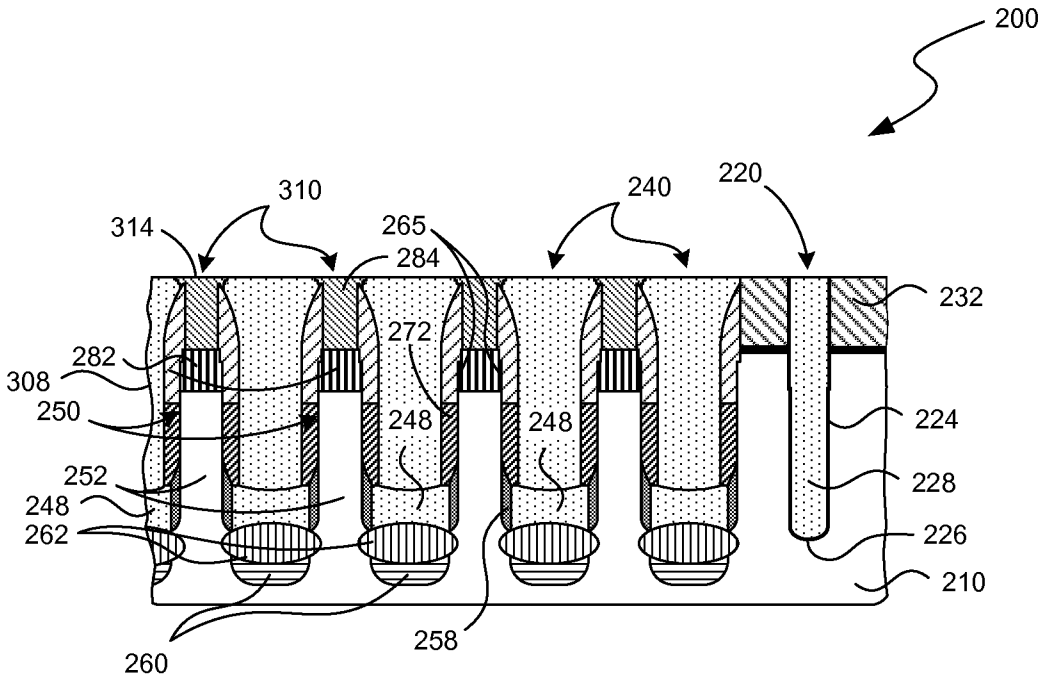

200
310
240
220
314
265
284
232
272
282
308
250
248
248
224
252
228
248
262
226
210
260
258

FIG. 22

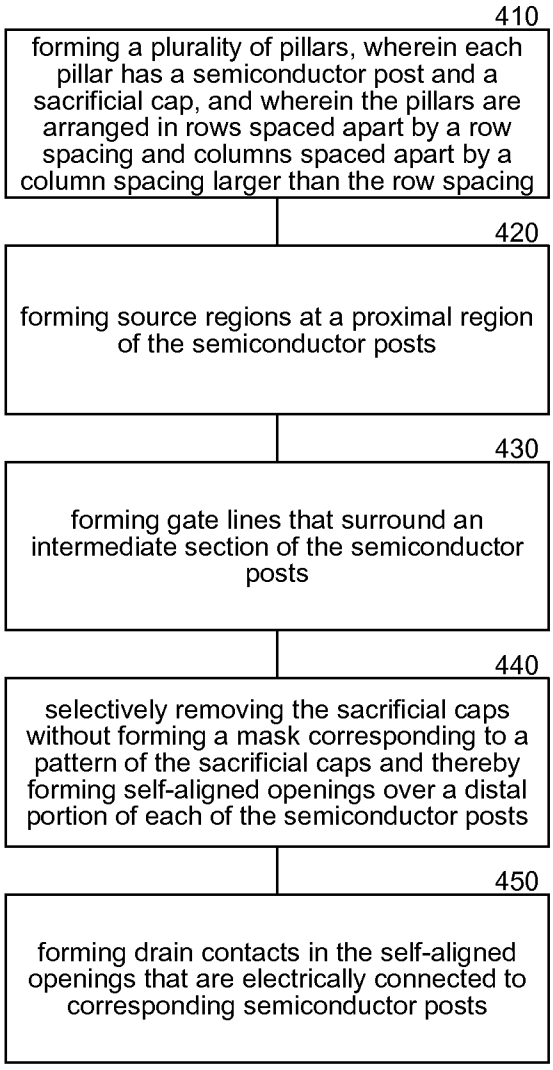

410
forming a plurality of pillars, wherein each pillar has a semiconductor post and a sacrificial cap, and wherein the pillars are arranged in rows spaced apart by a row spacing and columns spaced apart by a column spacing larger than the row spacing
420
forming source regions at a proximal region of the semiconductor posts
430
forming gate lines that surround an intermediate section of the semiconductor posts
440
selectively removing the sacrificial caps without forming a mask corresponding to a pattern of the sacrificial caps and thereby forming self-aligned openings over a distal portion of each of the semiconductor posts
450
forming drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts

FIG. 23