DATA LINE DRIVERS WITH COMMON REFERENCE RAMP DISPLAY

This invention relates generally to drive circuits for display devices and particularly to a system for applying brightness signals to pixels of a display device, such as a liquid crystal display (LCD).

Display devices, such as liquid crystal displays, are composed of a matrix or an array of pixels arranged horizontally in rows and vertically in columns. The video information to be displayed is applied as brightness (gray scale) signals to data lines which are individually associated with each column of pixels. The row of pixels are sequentially scanned and the capacitances of the pixels within the activated row are charged to the various brightness levels in accordance with the levels of the brightness signals applied to the individual columns.

In an active matrix display each pixel element includes a switching device which applies the video signal to the pixel. Typically, the switching device is a thin film transistor (TFT), which receives the brightness information from solid state circuitry. Because both the TFT's and the circuitry are composed of solid state devices it is preferable to simultaneously fabricate the TFT's and the drive circuitry utilizing either amorphous silicon or polysilicon technology.

Liquid crystal displays are composed of a liquid crystal material which is sandwiched between two substrates. At least one, and typically both of the substrates, is transparent to light and the surfaces of the substrates which are adjacent to the liquid crystal material support patterns of transparent conductive electrodes arranged in a pattern to form the individual pixel elements. It may be desirable to fabricate the drive circuitry on the substrates and around the perimeter of the display together with the TFT's.

Amorphous silicon has been the preferable technology for fabricating liquid crystal displays because this material can be fabricated at low temperatures. Low fabrication temperature is

important because it permits the use of standard, readily available and inexpensive substrate materials. However, the use of amorphous silicon thin film transistors (a-Si TFTs) in integrated peripheral pixel drivers has been limited because of, low mobility, threshold voltage drift and the availability of only N-MOS enhancement transistors.

U.S. Patent No. 5,170,155 in the names of Plus et al., entitled "System for Applying Brightness Signals To A Display Device And Comparator Therefore", describes a data line or column driver of an LCD. The data line driver of Plus et al., operates as a chopped ramp amplifier and utilizes TFT's. In the data line driver of Plus et al., an analog signal containing picture information is sampled and stored in an input sampling capacitor of the driver. A reference ramp produced in a reference ramp generator is applied to the input capacitor of the driver via a TFT switch.

It may be desirable to apply the reference ramp in common to each input capacitor without interposing a TFT switch between the reference ramp generator and the input capacitor. Advantageously, by eliminating such TFT switch, the data line driver is less susceptible to threshold voltage drift variations.

A data line driver, embodying an aspect of the invention, for developing a signal containing picture information in pixels of a display device that are arranged in columns includes a first transistor and a first capacitance coupled to the first transistor to form a comparator. A first switching arrangement is coupled to the first capacitance for storing a charge in the first capacitance that automatically adjusts a triggering level of the comparator. A reference ramp generator generates a reference ramp signal. A second capacitance couples the reference ramp signal to an input terminal of the capacitor. A second switching arrangement is coupled to the second capacitance for storing a video signal in the second capacitance. A second transistor is responsive to an output signal of the comparator for applying the data ramp signal to a data line during a period of the data ramp signal controlled by a signal that is developed at the input terminal of the comparator.

FIGURE 1 illustrates a block diagram of a liquid crystal display arrangement that includes demultiplexer and data line drivers, embodying an aspect of the invention;

FIGURE 2 illustrates the demultiplexer and data line driver of FIGURE 1 in more detail; and

FIGURES 3a-3g illustrate waveforms useful for explaining the operation of the circuit of FIGURE 2.

FIGURE 1 illustrates a block diagram of a liquid crystal display arrangement that includes demultiplexer and data line drivers, embodying an aspect of the invention;

FIGURE 2 illustrates the demultiplexer and data line driver of FIGURE 1 in more detail; and

FIGURES 3a-3g illustrate waveforms useful for explaining the operation of the circuit of FIGURE 2.

In FIGURE 1, that includes multiplexer and data line drivers 100, embodying an aspect of the invention, an analog circuitry 11 receives a video signal representative of picture information to be displayed from, for example, an antenna 12. The analog circuitry 11 provides a video signal on a line 13 as an input signal to an analog-to-digital converter (A/D) 14.

The television signal from the analog circuitry 11 is to be displayed on a liquid crystal array 16 which is composed of a large number of pixel elements, such as a liquid crystal cell 16a, arranged horizontally in m = 560 rows and vertically in n = 960 columns. Liquid crystal array 16 includes n = 960 columns of data lines 17, one for each of the vertical columns of liquid crystal cells 16a, and m = 560 select lines 18, one for each of the horizontal rows of liquid crystal cells 16a.

A/D converter 14 includes an output bus bar 19 to provide brightness levels, or gray scale codes, to a memory 21 having 40 groups of output lines 22. Each group of output lines 22 of memory 21 applies the stored digital information to a corresponding digital-to-analog (D/A) converter 23. There are 40 D/A converters 23 that correspond to the 40 groups of lines 22, respectively. An output signal IN of a given D/A converter 23 is coupled via a corresponding line 31 to corresponding multiplexer

and data line driver 100 that drives corresponding data line 17. A select line scanner 60 produces row select signals in lines 18 for selecting, in a conventional manner, a given row of array 16. The voltages developed in 960 data lines 17 are applied during a 32 microsecond line time, to pixels 16a of the selected row.

A given demultiplexer and data line driver 100 uses chopped ramp amplifiers, not shown in detail in FIGURE 1, with a low input capacitance that is, for example, smaller than 1pf to store corresponding signal IN and to transfer stored input signal IN to corresponding data line 17. Each data line 17 is applied to 560 rows of pixel cells 16a that form a capacitance load of, for example, 20pf.

FIGURE 2 illustrates in detail a given one of demultiplexer and data line drivers 100. FIGURES 3a-3g illustrate waveforms useful for explaining the operation of the circuit of FIGURE 2. Similar symbols and numerals in FIGURES 1, 2 and 3a-3g indicate similar items or functions. All the transistors of demultiplexer and line driver 100 of FIGURE 2 are TFT's of the N-MOS type. Therefore, advantageously, they can be formed together with array 16 of FIGURE 1 as one integrated circuit.

Prior to sampling the video signal in signal line 31 of FIGURE 2, a voltage developed at a terminal D of a capacitor C43 is initialized. To initialize the voltage in capacitor C43, D/A converter 23 develops a predetermined voltage in line 31 such as the maximum, or full scale voltage of video signal IN. A transistor MN1 applies the initializing voltage in line 31 to capacitor C43 when a control pulse PRE-DCTRL of FIGURE 3a is developed at the gate of transistor MN1. In this way, the voltage in capacitor C43 is the same prior to each pixel updating cycle. Following pulse PRE-DCTRL, signal IN changes to contain video information that is used for the current pixel updating cycle.

Demultiplexer transistor MN1 of a demultiplexer 32 of FIGURE 2 samples analog signal IN developed in signal line 31 that contains video information. The sampled signal is stored in sampling capacitor C43 of demultiplexer 32. The sampling of a group of 40 signals IN of FIGURE 1 developed in lines 31 occurs

simultaneously under the control of a corresponding pulse signal DCTRL(i). As shown in FIGURE 3a, 24 pulse signals DCTRL(i) occur successively, during an interval following t5a-t20. Each pulse signal DCTRL(i) of FIGURE 2 controls the demultiplexing operation in a corresponding group of 40 demultiplexers 32. The entire demultiplexing operation of 960 pixels occurs in interval t5a-t20 of FIGURE 3a.

To provide an efficient time utilization, a two-stage pipeline cycle is used. Signals IN are demultiplexed and stored in 960 capacitors C43 of FIGURE 2 during interval t5a-t20, as explained before. During an interval t3-t4 of FIGURE 3d, prior to the occurrence of any of pulse PRE-DCTRL and the 24 pulse signals DCTRL of FIGURE 3a, each capacitors C43 of FIGURE 2 is coupled to a capacitor C2 via a transistor MN7 when a pulse signal DXFER of FIGURE 3d occurs. Thus, a portion of signal IN that is stored in capacitor C43 is transferred to capacitor C2 of FIGURE 2 and develops a voltage VC2. During interval t5a-t20, when pulse signals DCTRL of FIGURE 3a occur, voltage VC2 of FIGURE 2 in capacitor C2 is applied to array 16 via corresponding data line 17, as explained below. Thus, signals IN are applied to array 16 via the two-stage pipeline.

A reference ramp generator 33 provides a reference ramp signal REF-RAMP on an output conductor 27. Conductor 27 is coupled, for example, in common to a terminal E of each capacitor C2 of FIGURE 2 of each demultiplexer and data line driver 100. A terminal A of capacitor C2 forms an input terminal of a comparator 24. A data ramp generator 34 of FIGURE 1 provides a data ramp voltage DATA-RAMP via an output line 28. In demultiplexer and data line driver 100 of FIGURE 2, a transistor MN6 applies voltage DATA-RAMP to data line 17 to develop a voltage VCOLUMN. The row to which voltage VCOLUMN is applied is determined in accordance with row select signals developed in row select lines 18. A display device using a shift register for generating select signals such as developed in lines 18 is described in, for example, U.S. Patent Nos. 4,766,430 and 4,742,346. Transistor MN6 is a TFT having a gate electrode that is

coupled to an output terminal C of comparator 24 by a conductor 29. An output voltage VC from the comparator 24 controls the conduction interval of transistor MN6.

In each pixel updating period, prior to applying voltage VC of comparator 24 to transistor MN6 to control the conduction interval of transistor MN6, comparator 24 is automatically calibrated or adjusted. During interval t0-t1 (FIGURE 3b) transistor MN10 is conditioned to conduct by a signal PRE-AUTOZ causing imposition of a voltage VPRAZ onto the drain electrode of a transistor MN5 and the gate electrode of transistor MN6. This voltage, designated VC, stored on stray capacitances such as, for example, a source-gate capacitance C24, shown in broken lines, of transistor MN6 causes transistor MN6 to conduct. Transistor MN5 is non-conductive when transistor MN10 pre-charges capacitance C24.

At a time t1 of FIGURE 3b, pulse signal PRE-AUTOZ terminates and transistor MN10 is turned off. At time t1, a pulse signal AUTOZERO is applied to a gate electrode of a transistor MN3 that is coupled between the gate and drain terminals of transistor MN5 to turn on transistor MN3. Simultaneously, a pulse signal AZ of FIGURE 3g is applied to a gate electrode of a transistor MN2 to turn on transistor MN2. When transistor MN2 is turned on, a voltage Va is coupled through transistor MN2 to terminal A of a coupling capacitor C1. Transistor MN2 develops a voltage VAA at terminal A at a level of voltage Va for establishing a triggering level of comparator 24 at terminal A. The triggering level of comparator 24 is equal to voltage Va. A second terminal B of capacitor C1 is coupled to transistor MN3 and the gate of transistor MN5.

Conductive transistor MN3 equilabrates the charge at terminal C, between the gate and drain electrodes of transistor MN5, and develops a gate voltage VG on the gate electrode of transistor MN5 at terminal B. Initially, voltage VG exceeds a threshold level VTH of transistor MN5 and causes transistor MN5 to conduct. The conduction of transistor MN5 causes the voltages at each of terminals B and C to decrease until each becomes equal

to the threshold level VTH of transistor MN5, during the pulse of signal AUTOZERO. Gate electrode voltage VG of transistor MN5 at terminal B is at its threshold level VTH when voltage VAA at terminal A is equal to voltage Va. At time t2 of FIGURES 3c and 3f, transistors MN3 and MN2 of FIGURE 2 are turned off and comparator 24 is calibrated or adjusted. Therefore, the triggering level of comparator 24 of FIGURE 2 with respect to input terminal A is equal to voltage Va.

As explained above, pulse signal DXFER developed, beginning at time t3, at the gate of transistor MN7 couples capacitor C43 of demultiplexer 32 to capacitor C2 via terminal A. Consequently, voltage VC2 that is developed in capacitor C2 is proportional to the level of sampled signal IN in capacitor C43. The magnitude of signal IN is such that voltage VAA developed at terminal A, during pulse signal DXFER, is smaller than triggering level Va of comparator 24. Therefore, comparator transistor MN5 remains non-conductive immediately after time t3. A voltage difference between voltage VAA and the triggering level of comparator 24 that is equal to voltage Va is determined by the magnitude of signal IN.

When voltage VAA at terminal A exceeds voltage Va, transistor MN5 becomes conductive. On the other hand, when voltage VAA at terminal A does not exceed voltage Va, transistor MN5 is nonconductive. The automatic calibration or adjustment of comparator 24 compensates for threshold voltage drift, for example, in transistor MN5.

Pulse signal PRE-AUTOZ, following time t2 of FIGURE 3b, is coupled to the gate electrode of transistor MN10 of FIGURE 1. Transistor MN10 applies voltage VPRAZ to the gate of transistor MN6, to turn on transistor MN6. Because transistor MN5 is nonconductive following time t3 of FIGURE 3d, the charge that is applied by transistor MN10 remains stored in the inter-electrode capacitance of transistor MN6. Therefore, transistor MN6 remains conductive after transistor MN10 is turned off.

When transistor MN6 is conductive, it establishes a predetermined initial condition of voltage VCOLUMN on line 17 and in pixel cell 16a of FIGURE 1 of the selected row. Transistor MN6 establishes voltage VCOLUMN at an inactive level VIAD of signal DATA-RAMP, prior to time t6. Thus, capacitance C4 associated with the data line 17 is charged/discharged toward inactive level VIAD of signal DATA-RAMP. Advantageously, establishing the initial condition in pixel cell 16a prevents previous stored picture information contained in the capacitance of pixel cell 16a from affecting pixel voltage VCOLUMN at the current update period of FIGURES 3b-3g.

At time t4 of FIGURE 3e, reference ramp signal REF-RAMP begins up-ramping. Signal REF-RAMP is coupled to terminal E of capacitor C2 of FIGURE 2 that is remote from input terminal A of comparator 24. As a result, voltage VAA at input terminal A of comparator 24 is equal to a sum voltage of ramping signal REF-RAMP and voltage VC2 developed in capacitor C2.

In accordance with an inventive feature, during interval t1-t2 of FIGURE 3c, when the automatic triggering voltage adjustment or calibration of comparator 24 occurs, transistor MN2 couples voltage Va to capacitor C2 via terminal A, that is remote from reference ramp generator 33. Similarly, during interval t3-t4, when the charge is transferred to capacitor C2, transistor MN7 is coupled to capacitor C2 via terminal A that is remote from ramp generator 33. Thus, terminal E of capacitor C2, advantageously, need not be decoupled from conductor 27 of reference ramp generator 33. Because terminal E need not be decoupled from reference ramp generator 33, signal REF-RAMP is coupled to terminal A of comparator 24 without interposing any TFT switch between conductor 27 of reference ramp generator 33 and terminal A. A TFT in the signal path might have suffered from threshold voltage drift. Advantageously, conductor 27 may be common to several units of multiplexer and data drivers 100.

Following time t6, data ramp voltage DATA-RAMP coupled to the drain electrode of transistor MN6 begins upramping. With feedback coupling to terminal C from the stray gate-source and

gate driven capacitance of transistor MN6, the voltage at terminal C will be sufficient to condition transistor MN6 to conduct for all values of the data ramp signal DATA-RAMP. Following time t4, and as long as ramping voltage VAA at terminal A has not reached the triggering level that is equal to voltage Va of comparator 24, transistor MN5 remains non-conductive and transistor MN6 remains conductive. As long as transistor MN6 is conductive, upramping voltage DATA-RAMP is coupled through transistor MN6 to column data line 17 for increasing the potential VCOLUMN of data line 17 and, therefore, the potential applied to pixel capacitance CPIXEL of the selected row. The capacitive feedback of ramp voltage VCOLUMN via, for example, capacitance 24, sustains transistor MN6 in conduction, as long as transistor MN5 exhibits a high impedance at terminal C, as indicated before.

At some time during the upramping portion 500 of signal REF-RAMP of FIGURE 3e, the sum voltage VAA at terminal A will exceed the triggering level Va of comparator 24, and transistor MN5 will become conductive. The instant that transistor MN5 becomes conductive is determined by the magnitude of signal IN.

When transistor MN5 becomes conductive, gate voltage VC of transistor MN6 decreases and causes transistor MN6 to turn off. As a result, the last value of voltage DATA-RAMP that occurs prior to the turn-off of transistor MN6 is held unchanged or stored in pixel capacitance CPIXEL until the next updating cycle. In this way, the current updating cycle is completed.

In order to prevent polarization of liquid crystal array 16 of FIGURE 1, a so-called backplane or common plane of the array, not shown, is maintained at a constant voltage VBACKPLANE. Multiplexer and data line driver 100 produces, in one updating cycle, voltage VCOLUMN that is at one polarity with respect to voltage VBACKPLANE and at the opposite polarity and the same magnitude, in an alternate updating cycle. To attain the alternate polarities, voltage DATA-RAMP is generated in the range of 1V-8.8V in one updating cycle and in the range of 9V-16.8V in the alternate update cycle. Whereas, voltage VBACKPLANE is established at an intermediate level between the two ranges.

Because of the need to generate voltage DATA-RAMP in two different voltage ranges, signals or voltages AUTOZERO, PRE-AUTOZ and Vss have two different peak levels that change in alternate updating cycles in accordance with the established range of voltage DATA-RAMP.

WHAT IS CLAIMED IS:

1. Apparatus for applying video signal to column electrodes of a display device, comprising:

a source of a video signal;

a reference ramp generator for generating a reference ramp signal;

a plurality of data line drivers responsive to said video signal for applying said video signal to said column electrodes, each said data line driver including:

a comparator;

a first capacitance for coupling said reference ramp generator to an input of said comparator;

a first switching arrangement coupled to said video signal source and to said first capacitance for selectively applying said video signal to said first capacitance that applies said video to said input of said comparator, such that, when said video signal indicative signal is being stored in said first capacitance, an output terminal of said reference ramp generator is coupled in a common current path of the first capacitances of said data line drivers;

a source of a data ramp signal; and

a switching transistor responsive to an output signal of said comparator for applying said data ramp signal to said column electrode during a controllable portion of a period of said data ramp signal that varies in accordance with a signal that is developed at said input of said comparator.

2. An apparatus according to claim 1, wherein said comparator comprises a second capacitance and a second switching arrangement coupled to said second capacitance and to a source of an adjustment signal for generating a voltage in said second capacitance that automatically adjusts a triggering level of said comparator in accordance with said adjustment signal.

3. An apparatus according to claim 2 wherein said adjustment signal is coupled to an interconnection of said second and first capacitances.

4. An apparatus according to claim 2 wherein said first capacitance is coupled between said reference ramp generator and said second switching arrangement.

5. An apparatus according to claim 2 wherein said comparator comprises a second transistor coupled to a control terminal of said first switching transistor and wherein a third transistor is coupled between a control terminal of said second transistor and a main current conducting terminal of said second transistor for adjusting said triggering level of said comparator in accordance with said adjustment signal.

6. An apparatus according to claim 1 wherein said comparator comprises a second transistor and a second capacitance coupled between said first capacitance and a control terminal of said second transistor and wherein said first switching arrangement is coupled to a junction terminal between said capacitances.

7. An apparatus according to claim 1 wherein said output terminal of said reference ramp generator is coupled to said input of said comparator via a signal path that excludes any switching arrangement.

* C L M S *

8. . A data line driver for developing a signal containing picture information in pixels of a display device that are arranged in columns, comprising:

a first transistor;

a first capacitance coupled to said first transistor to form a comparator;

a first switching arrangement coupled to said first capacitance for storing a charge in said first capacitance that automatically adjusts a triggering level of said comparator;

a reference ramp generator for generating a reference ramp signal;

a second capacitance for coupling said reference ramp signal to an input terminal of said capacitor;

a source of a video signal;

a second switching arrangement coupled to said second capacitance for storing said video signal in said second capacitance;

a source of a data ramp signal; and

a second transistor responsive to an output signal of said comparator for applying said data ramp signal to a data line during a period of said data ramp signal controlled by a signal that is developed at said input terminal of said comparator.

9. A data line driver according to claim 8 further comprising, a third transistor coupled between a main current conducting terminal of said first transistor and a control terminal of said first transistor and wherein said third transistor and said first switching arrangement are coupled to different terminals of said first capacitance to develop a voltage in said first capacitance that automatically adjusts said triggering level of said comparator.

10. A data line driver according to claim 8 wherein said second capacitance is coupled between said reference ramp generator and said first capacitance.

11. A video apparatus for developing a signal containing picture information in pixels of a display device that are arranged in columns, comprising:

a reference ramp generator for generating a reference ramp signal;

a plurality of data line drivers responsive to said video signal for applying said video signal to said pixels, a given data line driver of said plurality of line drivers being coupled to pixels arranged in a corresponding column that is associated with said given data line driver, said given data line driver including:

a comparator;

a capacitance for coupling said reference ramp generator to an input of said comparator;

a source of a video signal coupled to said input of said comparator;

a first switching arrangement responsive to said video signal and coupled to said capacitance via a terminal of said first capacitance that is remote from said reference ramp generator for storing said video signal in said capacitance;

a source of a data ramp signal;

a switching transistor responsive to an output signal of said comparator for applying said data ramp signal to said pixels of said column that is associated with said given data line driver, during a controllable portion of a period of said data ramp signal that varies in accordance with a signal that is developed at said input of said comparator.

12. Apparatus for applying video signal to a column electrode of a display device, comprising:

a source of a video signal;

a reference ramp generator for generating a reference ramp signal;

a data line driver responsive to said video signal for applying said video signal to said column electrode, said data line driver including:

a comparator;

a first capacitance having a first terminal coupled to said reference ramp generator and a second terminal coupled to an input of said comparator;

a first switching arrangement coupled to said video signal source and to said said second terminal of first capacitance for selectively applying said video signal to said first capacitance that applies said video to said input of said comparator;

a source of a data ramp signal; and

a switching transistor responsive to an output signal of said comparator for applying said data ramp signal to said column electrode during a controllable portion of a period of said data ramp signal that varies in accordance with a signal that is developed at said input of said comparator.