

ABSTRACT

A clock recovery circuit receives an input signal having an eye pattern and takes differences at certain intervals to generate a differential signal. A set of comparators detect timings at which the differential signal matches different levels, and generate pulse signals at these timings. A classifying circuit classifies trajectories of the differential signal by detecting certain sequences of these pulse signals, and activates a gate signal when these sequences are detected. A delay circuit delays one of the pulse signals to create a delayed signal. A gate circuit outputs the delayed signal as a timing signal when the gate signal is active. A phase-locked loop generates a clock signal synchronized to the timing signal.