FIG. 1

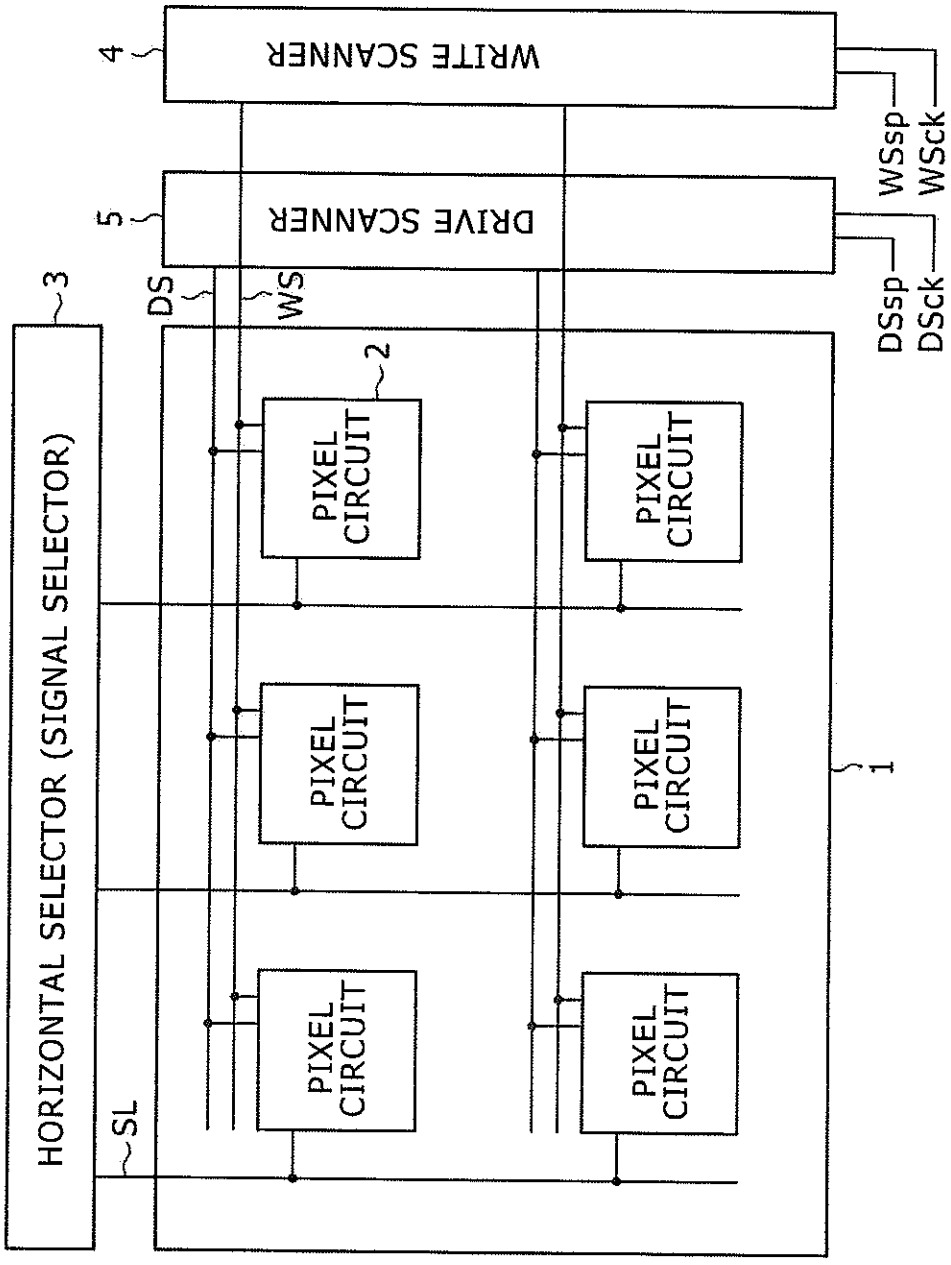

WRITE SCANNER
4
DRIVE SCANNER
5
WSsp
WSck
DSsp
DSck
DS
WS
3
HORIZONTAL SELECTOR (SIGNAL SELECTOR)
SL
2
PIXEL CIRCUIT
PIXEL CIRCUIT
PIXEL CIRCUIT
PIXEL CIRCUIT
PIXEL CIRCUIT
PIXEL CIRCUIT
1

FIG. 2

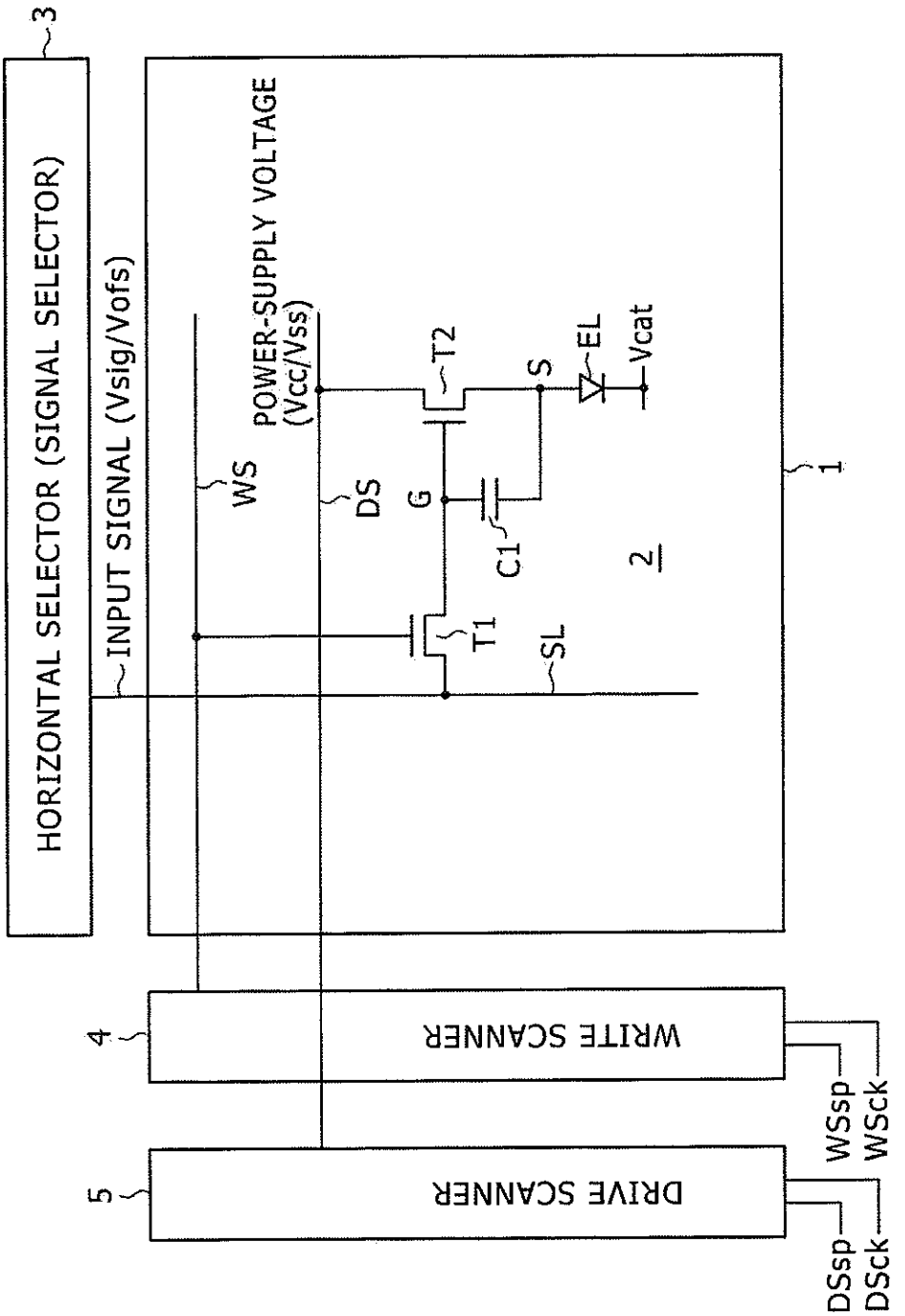

3
HORIZONTAL SELECTOR (SIGNAL SELECTOR)
INPUT SIGNAL (Vsig/Vofs)
POWER-SUPPLY VOLTAGE (Vcc/Vss)
WS
DS
G
T2
S
EL
Vcat
C1
T1
SL
2
1
4
WRITE SCANNER
5
DRIVE SCANNER
WSsp
WSck
DSsp
DSck

FIG. 3

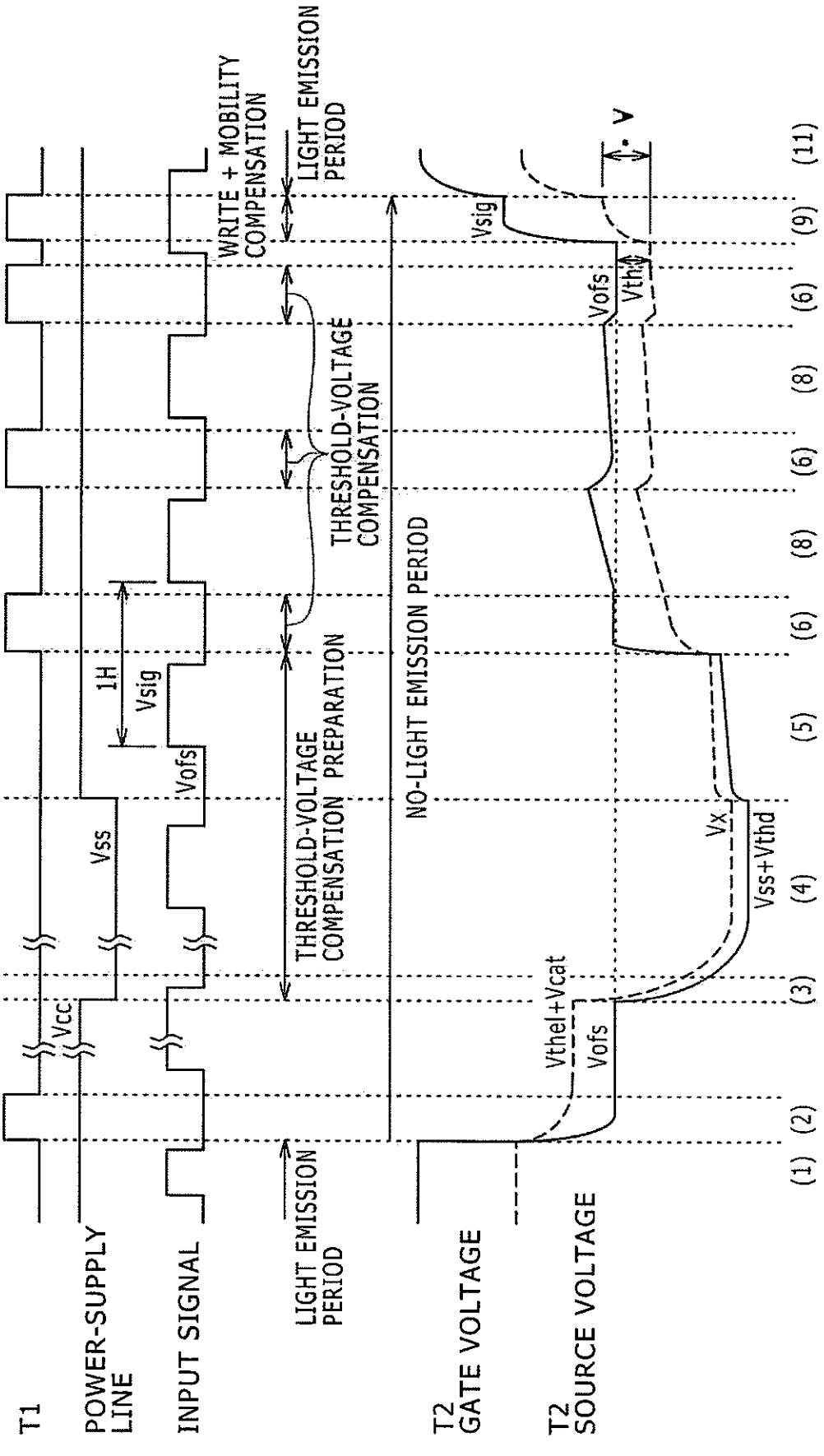

T1
POWER-SUPPLY LINE
INPUT SIGNAL
LIGHT EMISSION PERIOD
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
Vcc
Vss
1H
Vsig
Vofs
THRESHOLD-VOLTAGE COMPENSATION PREPARATION
THRESHOLD-VOLTAGE COMPENSATION
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
NO-LIGHT EMISSION PERIOD
Vthel+Vcat
Vofs
Vx
Vss+Vthd
Vsig
Vofs
Vth
ΔV
(1) (2) (3) (4) (5) (6) (8) (6) (8) (6) (9) (11)

FIG.4A

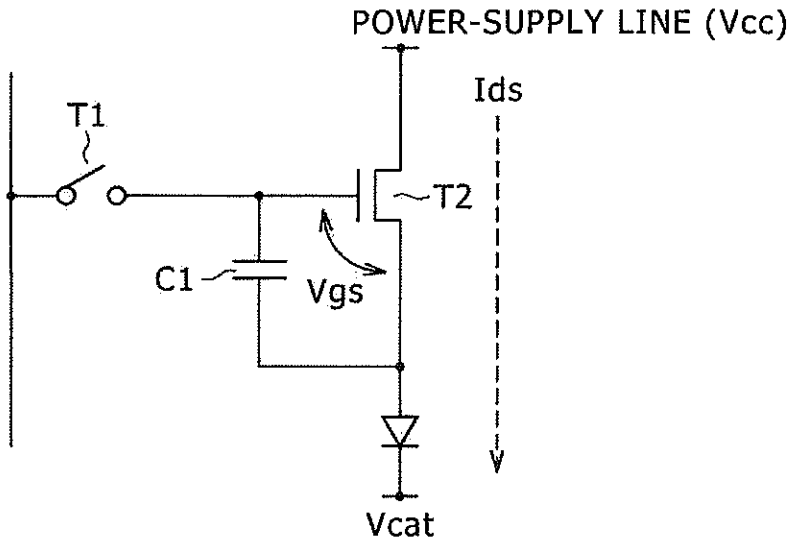

POWER-SUPPLY LINE (Vcc)
Ids
T1
T2
C1
Vgs
Vcat

FIG.4B

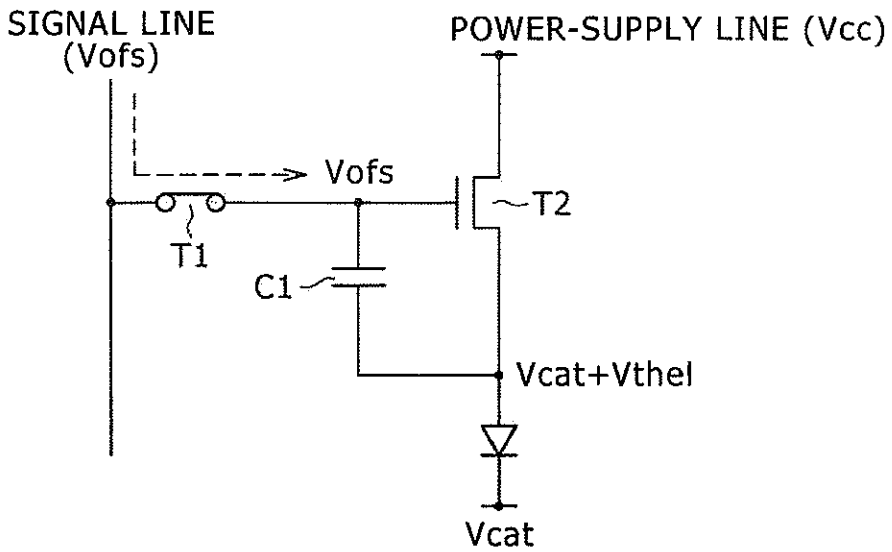

SIGNAL LINE
(Vofs)
POWER-SUPPLY LINE (Vcc)
Vofs
T2
T1
C1
Vcat+Vthel
Vcat

FIG.4C

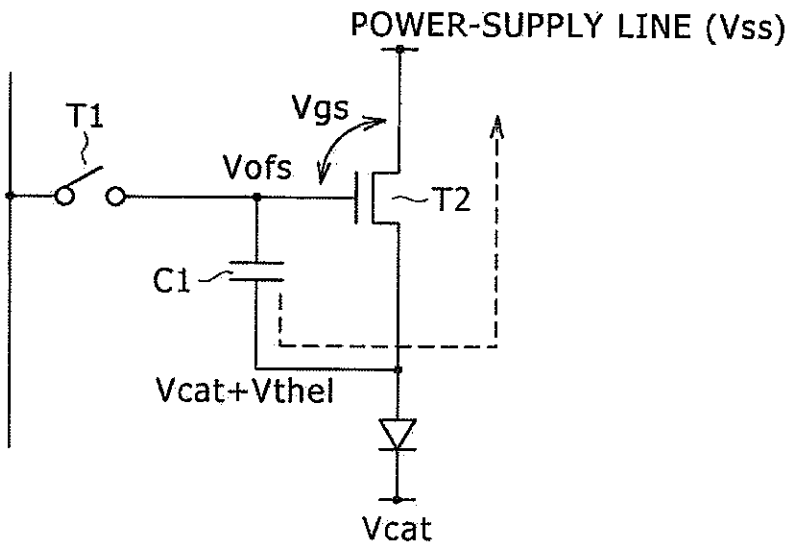

POWER-SUPPLY LINE (Vss)
T1
Vgs
Vofs
T2
C1
Vcat+Vthel
Vcat

FIG.4D

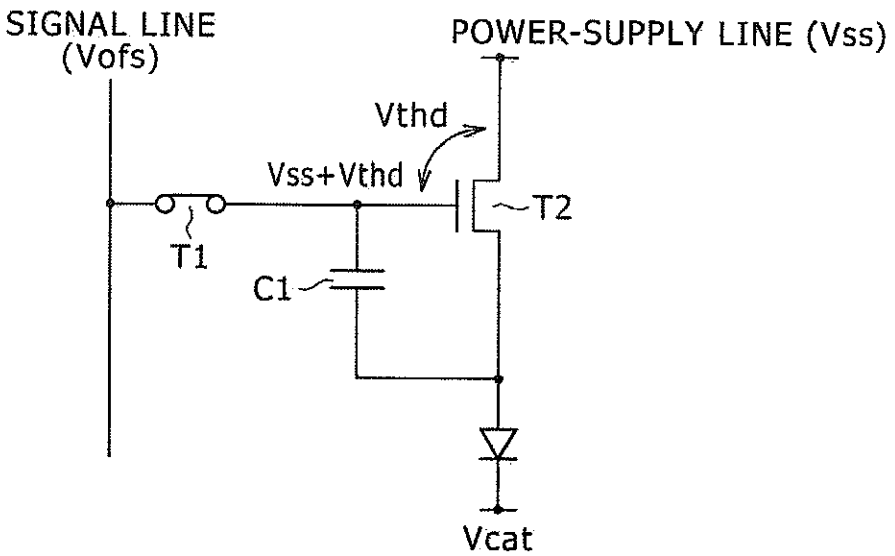

SIGNAL LINE
(Vofs)
POWER-SUPPLY LINE (Vss)
Vthd
Vss+Vthd
T2
T1
C1
Vcat

FIG.4E

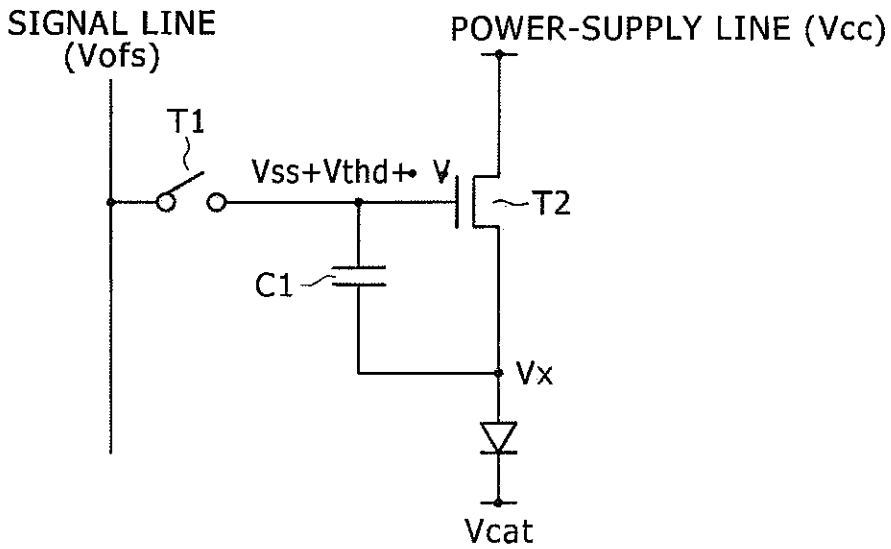

SIGNAL LINE
(Vofs)
POWER-SUPPLY LINE (Vcc)
T1
Vss+Vthd+α V
T2
C1
Vx
Vcat

FIG.4F

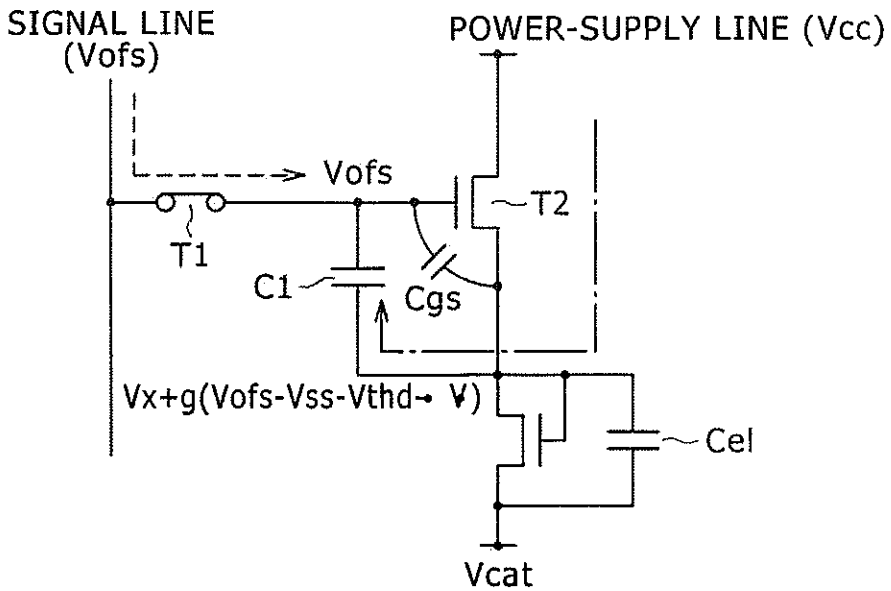

SIGNAL LINE
(Vofs)
POWER-SUPPLY LINE (Vcc)
Vofs
T2
T1
C1
Cgs
Vx+g(Vofs-Vss-Vthd-α V)
Cel
Vcat

FIG.4G

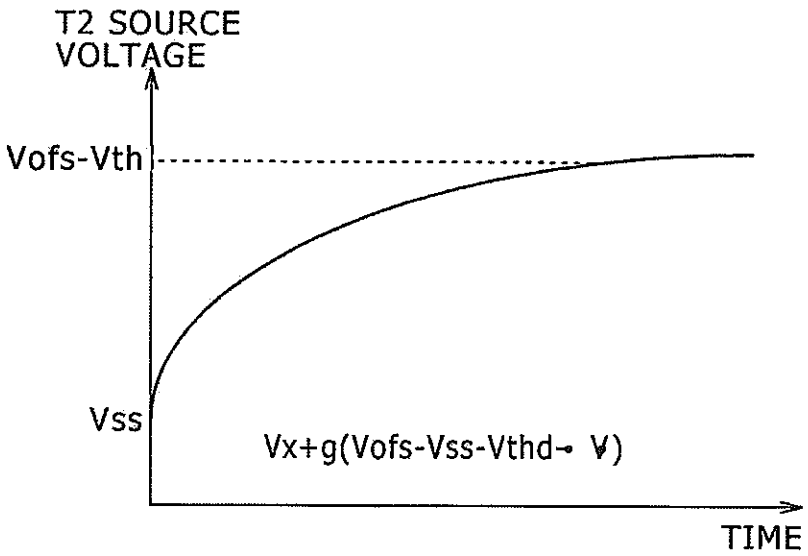

T2 SOURCE VOLTAGE
Vofs-Vth
Vss
Vx+g(Vofs-Vss-Vthd-ΔV)
TIME

FIG.4H

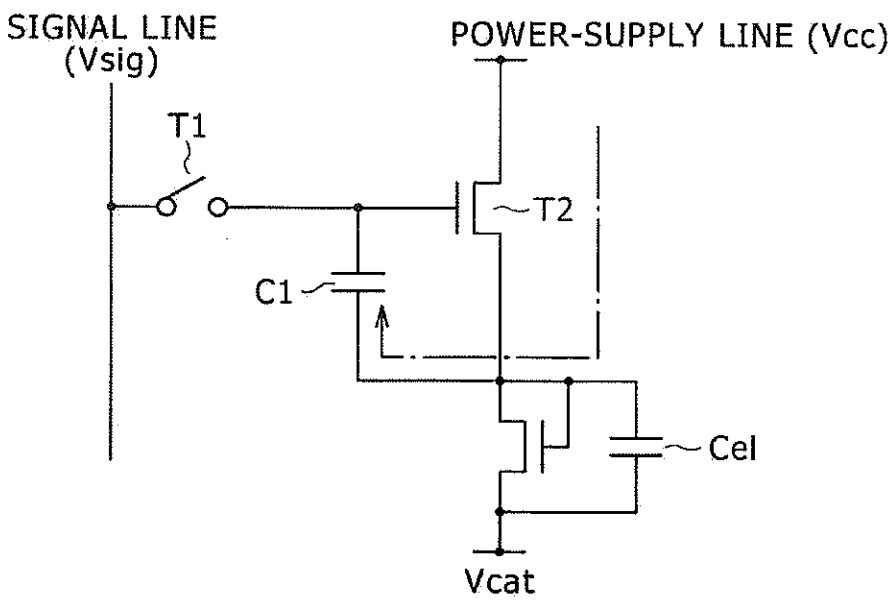

SIGNAL LINE (Vsig)
POWER-SUPPLY LINE (Vcc)
T1
T2
C1
Cel
Vcat

FIG.4I

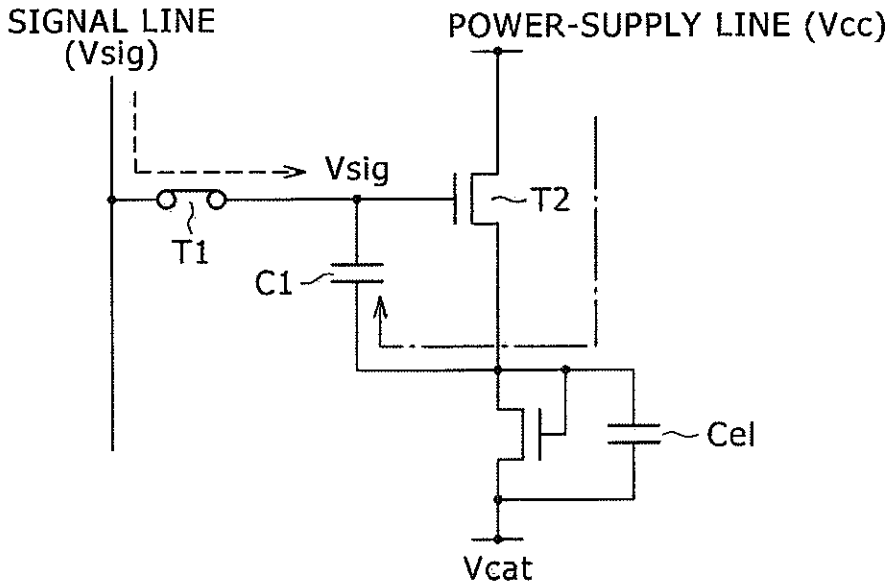

SIGNAL LINE
(Vsig)
POWER-SUPPLY LINE (Vcc)
Vsig
T1
T2
C1
Cel
Vcat

FIG.4J

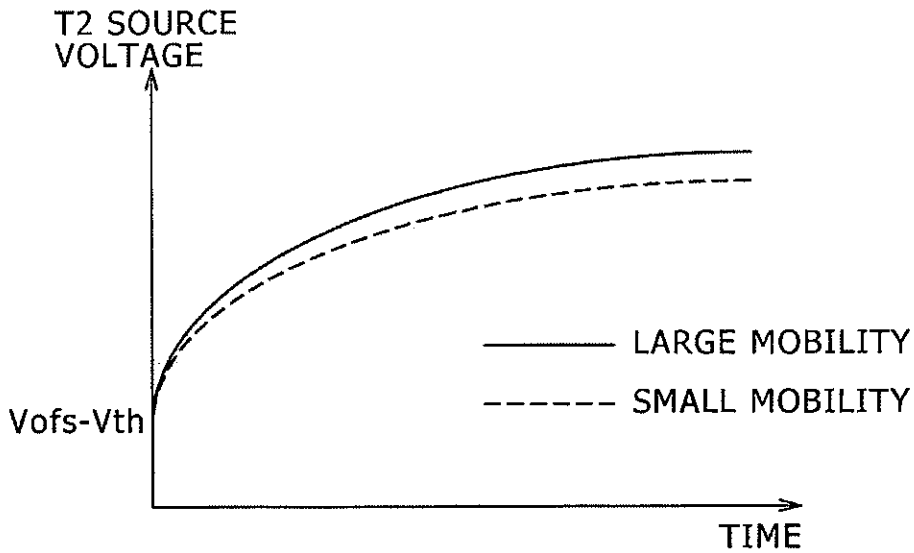

T2 SOURCE
VOLTAGE
Vofs-Vth
LARGE MOBILITY
SMALL MOBILITY
TIME

FIG. 4K

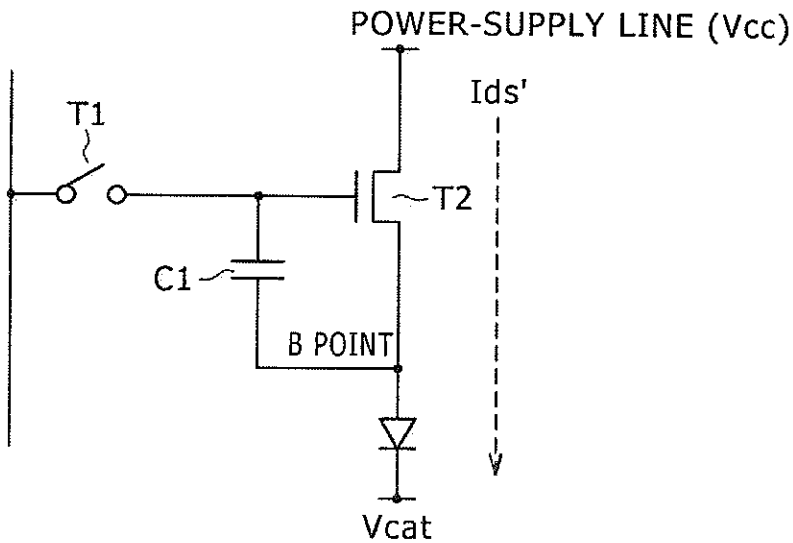


FIG. 5

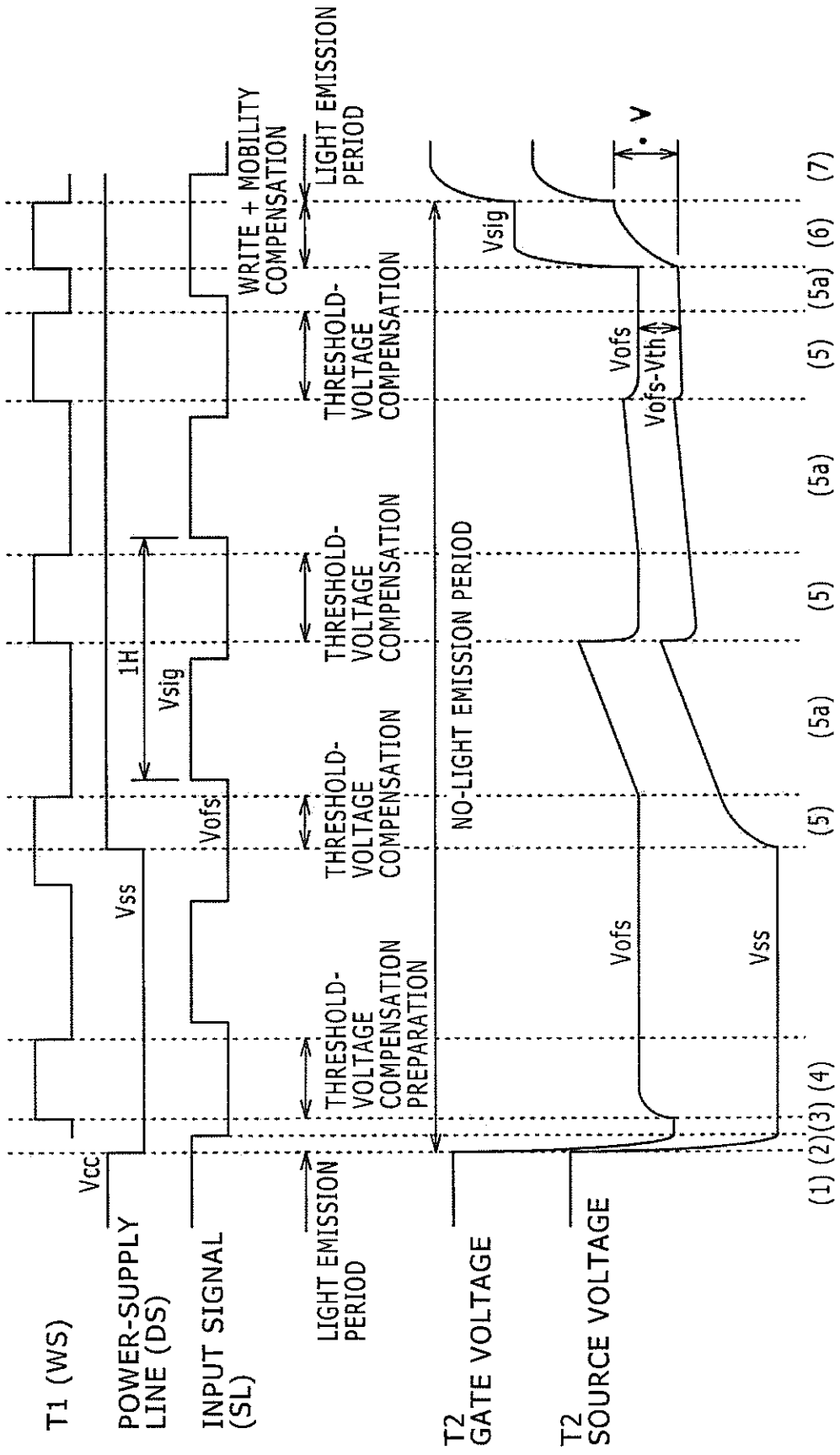

T1 (WS)
POWER-SUPPLY LINE (DS)
INPUT SIGNAL (SL)
LIGHT EMISSION PERIOD
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
Vcc
Vss
Vofs
1H
Vsig
THRESHOLD-VOLTAGE COMPENSATION PREPARATION
THRESHOLD-VOLTAGE COMPENSATION
THRESHOLD-VOLTAGE COMPENSATION
NO-LIGHT EMISSION PERIOD
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
Vsig
Vofs
Vofs-Vth
ΔV
(1) (2)(3) (4)
(5)
(5a)
(5)
(5a)
(5)
(5a)
(6)
(7)

FIG. 6A

(1)

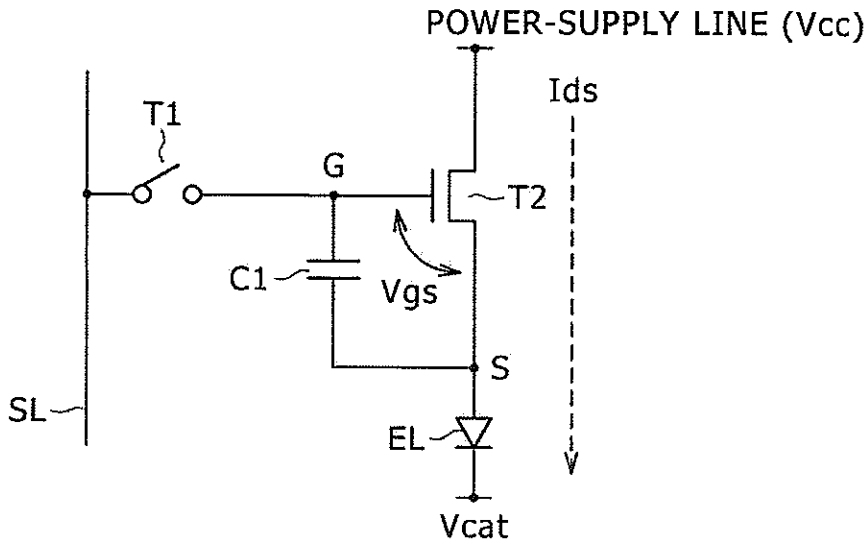


FIG. 6B

(2), (3)

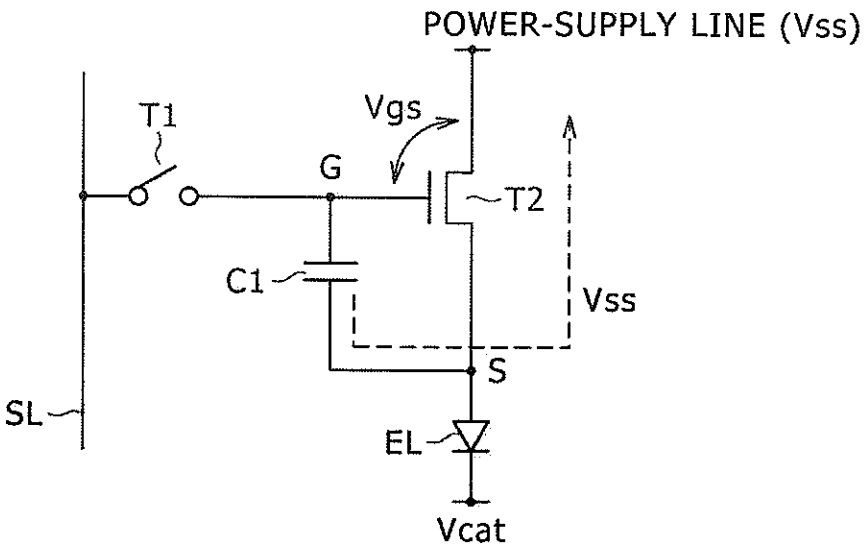


FIG. 6C

(4)

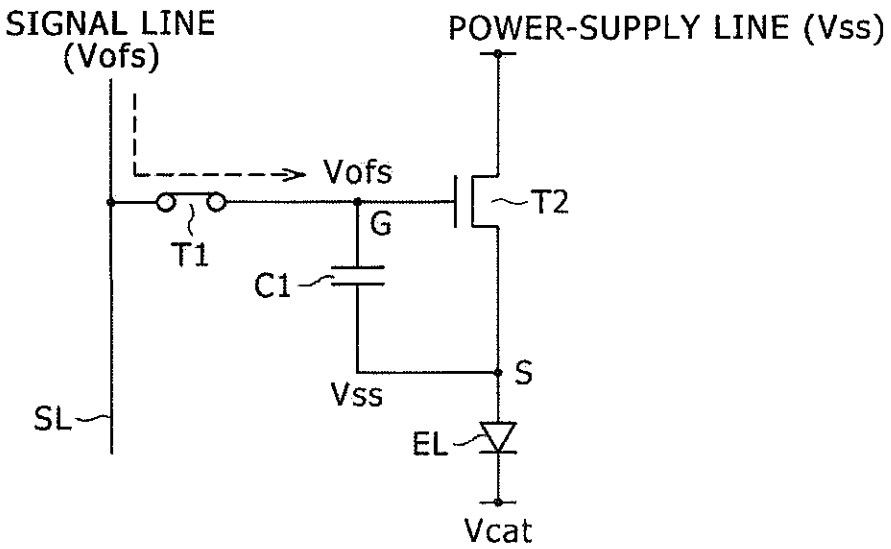


FIG. 6D

(5)

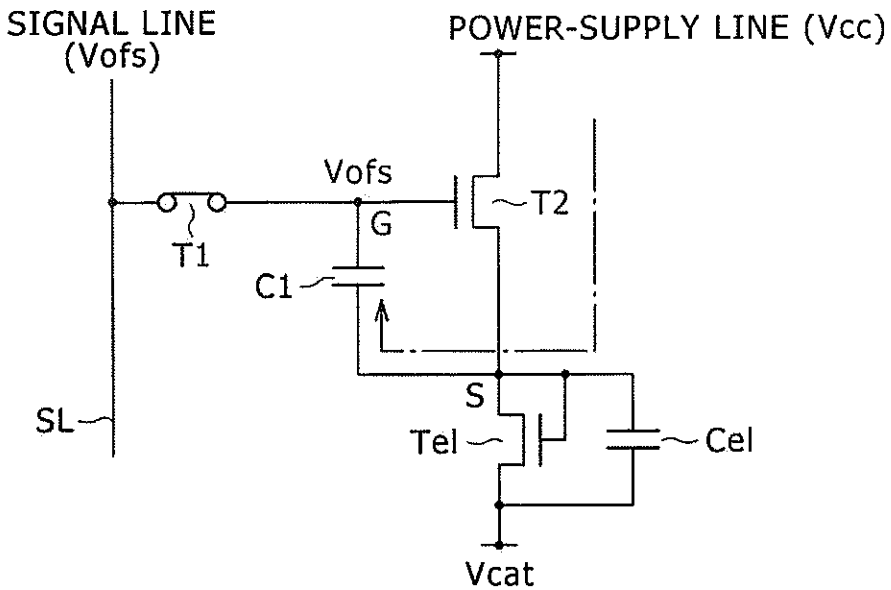


FIG.6E

(5a)

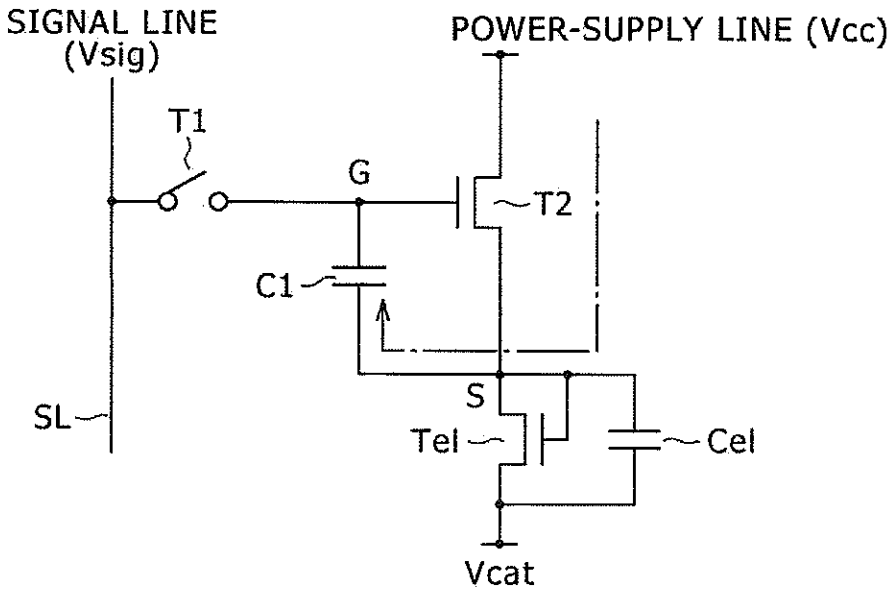


FIG.6F

(6)

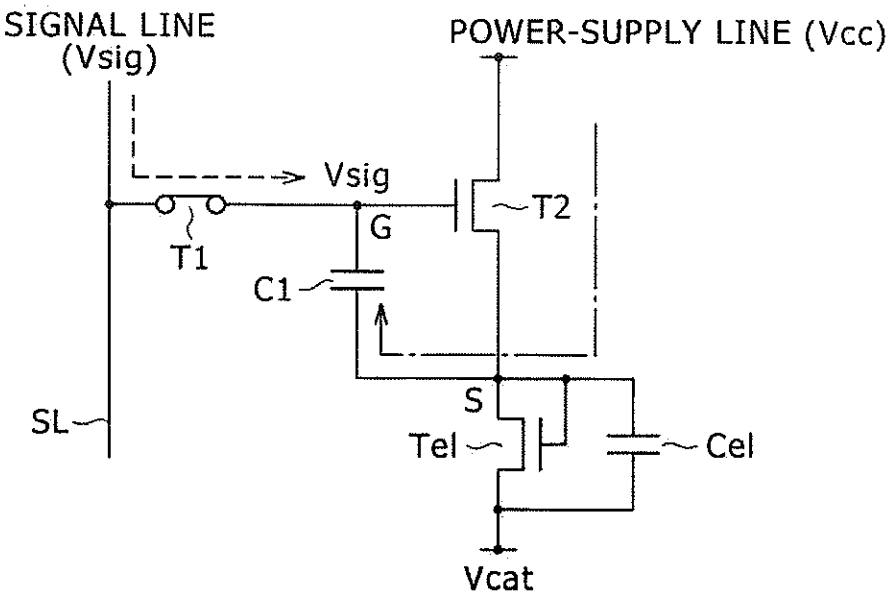


FIG. 6G

(7)

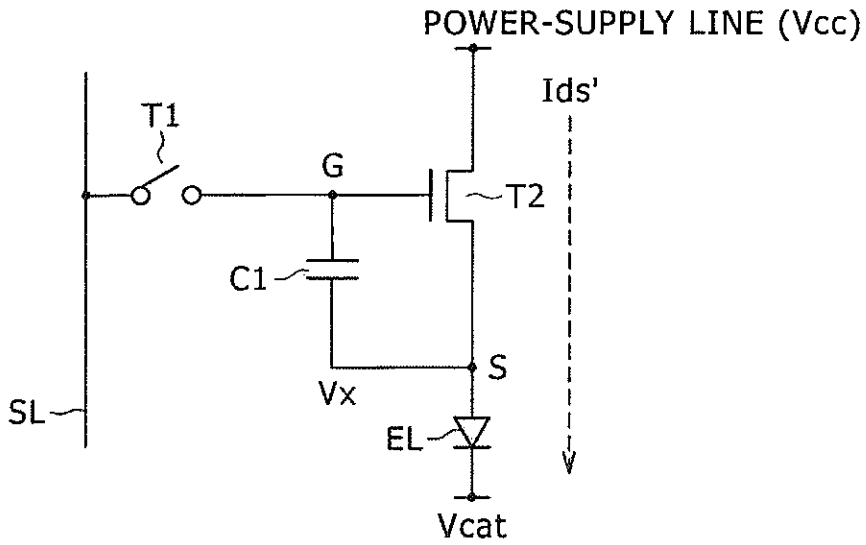


FIG. 7

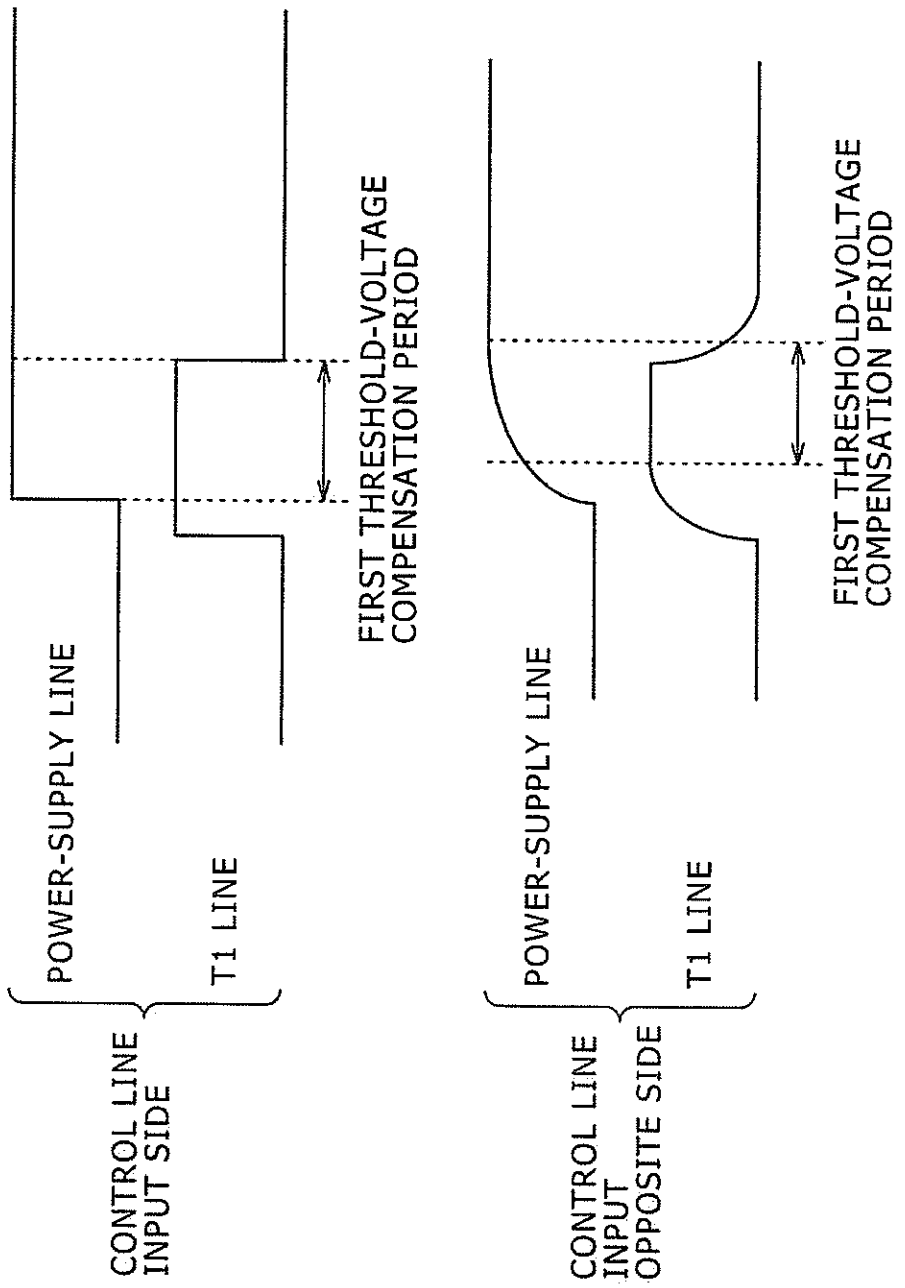

CONTROL LINE
INPUT SIDE
POWER-SUPPLY LINE
T1 LINE
FIRST THRESHOLD-VOLTAGE
COMPENSATION PERIOD
CONTROL LINE
INPUT
OPPOSITE SIDE
POWER-SUPPLY LINE
T1 LINE
FIRST THRESHOLD-VOLTAGE
COMPENSATION PERIOD

FIG. 8

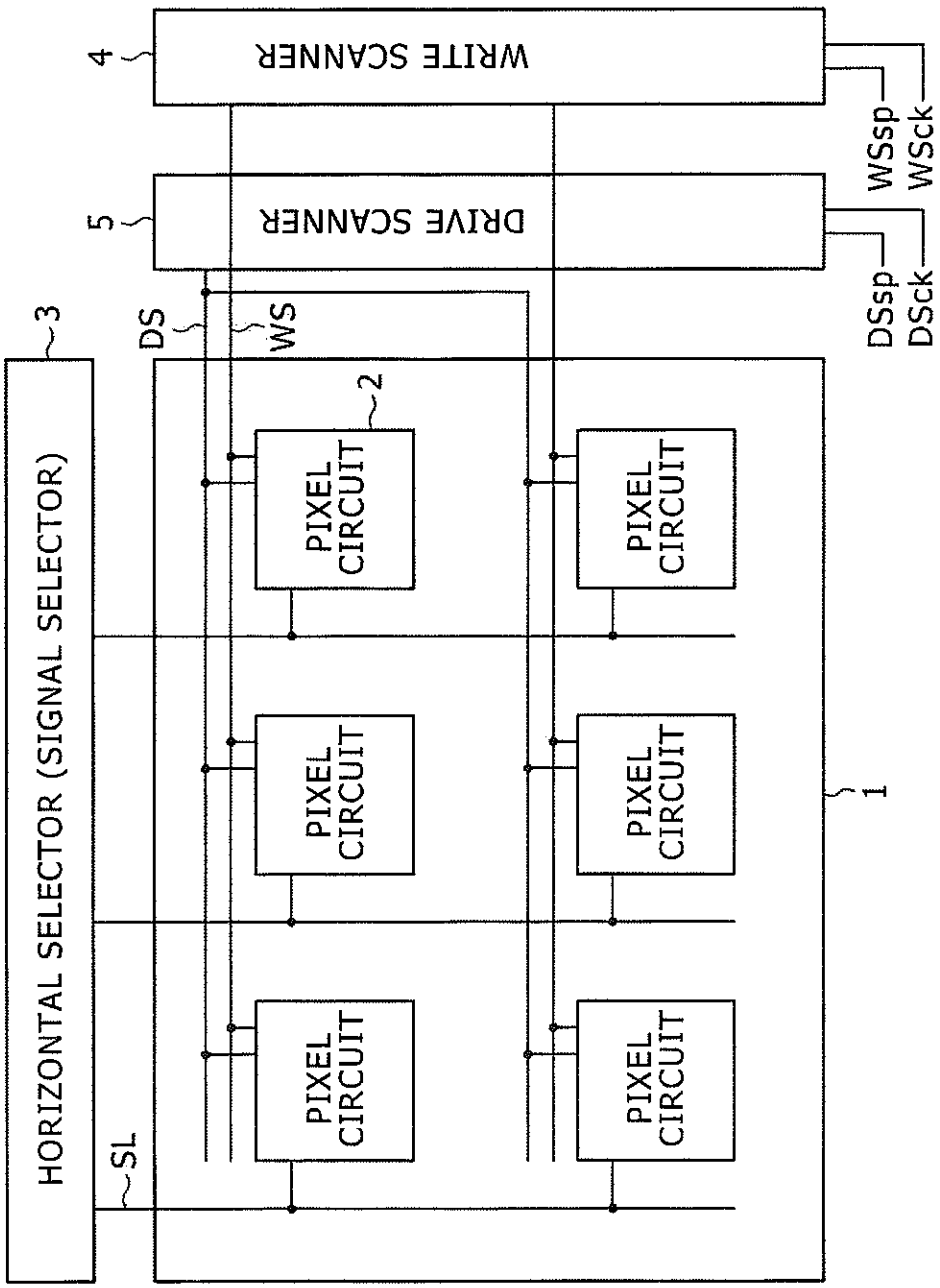

WRITE SCANNER
4
DRIVE SCANNER
5
WSsp
WSck
DSsp
DSck
HORIZONTAL SELECTOR (SIGNAL SELECTOR)
3
DS
WS
SL
PIXEL CIRCUIT
2
1

FIG. 9

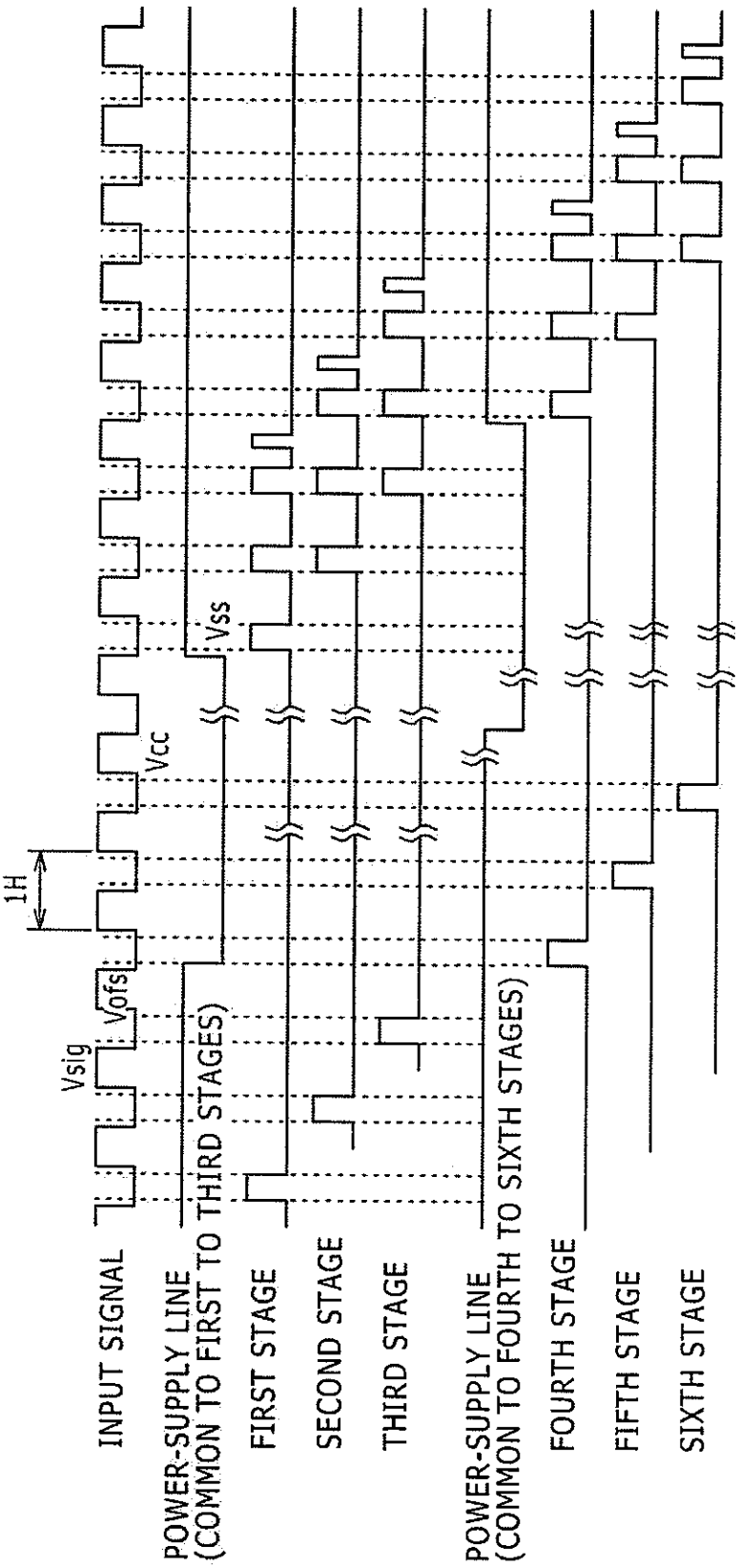

INPUT SIGNAL
POWER-SUPPLY LINE (COMMON TO FIRST TO THIRD STAGES)
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE (COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE
FIFTH STAGE
SIXTH STAGE
Vsig
Vofs
Vcc
Vss
1H

FIG. 10

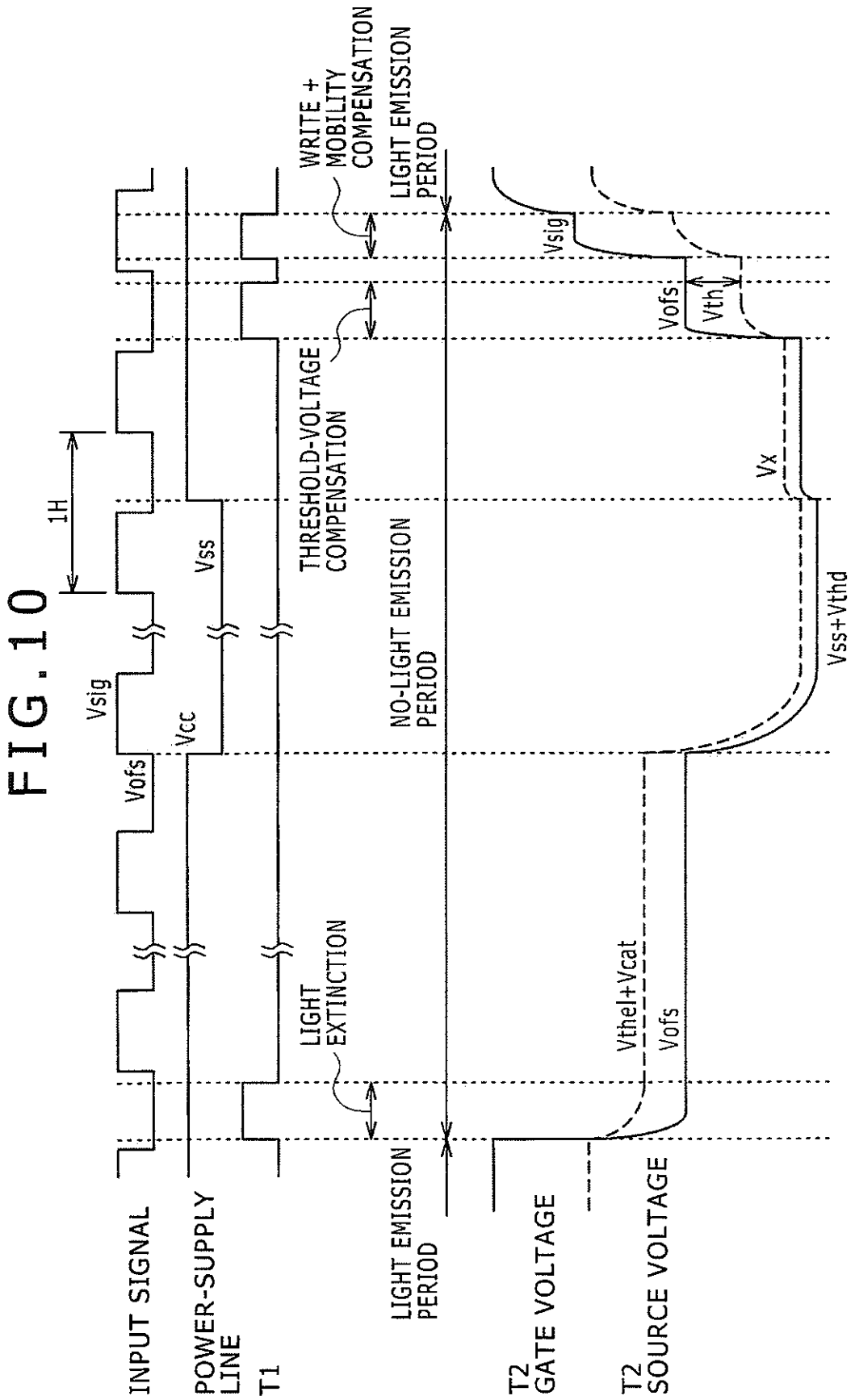

INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
1H
Vsig
Vofs
Vcc
Vss
LIGHT EXTINCTION
THRESHOLD-VOLTAGE COMPENSATION
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
NO-LIGHT EMISSION PERIOD
LIGHT EMISSION PERIOD
Vthel+Vcat
Vofs
Vsig
Vofs
Vth
Vx
Vss+Vthd

FIG. 11

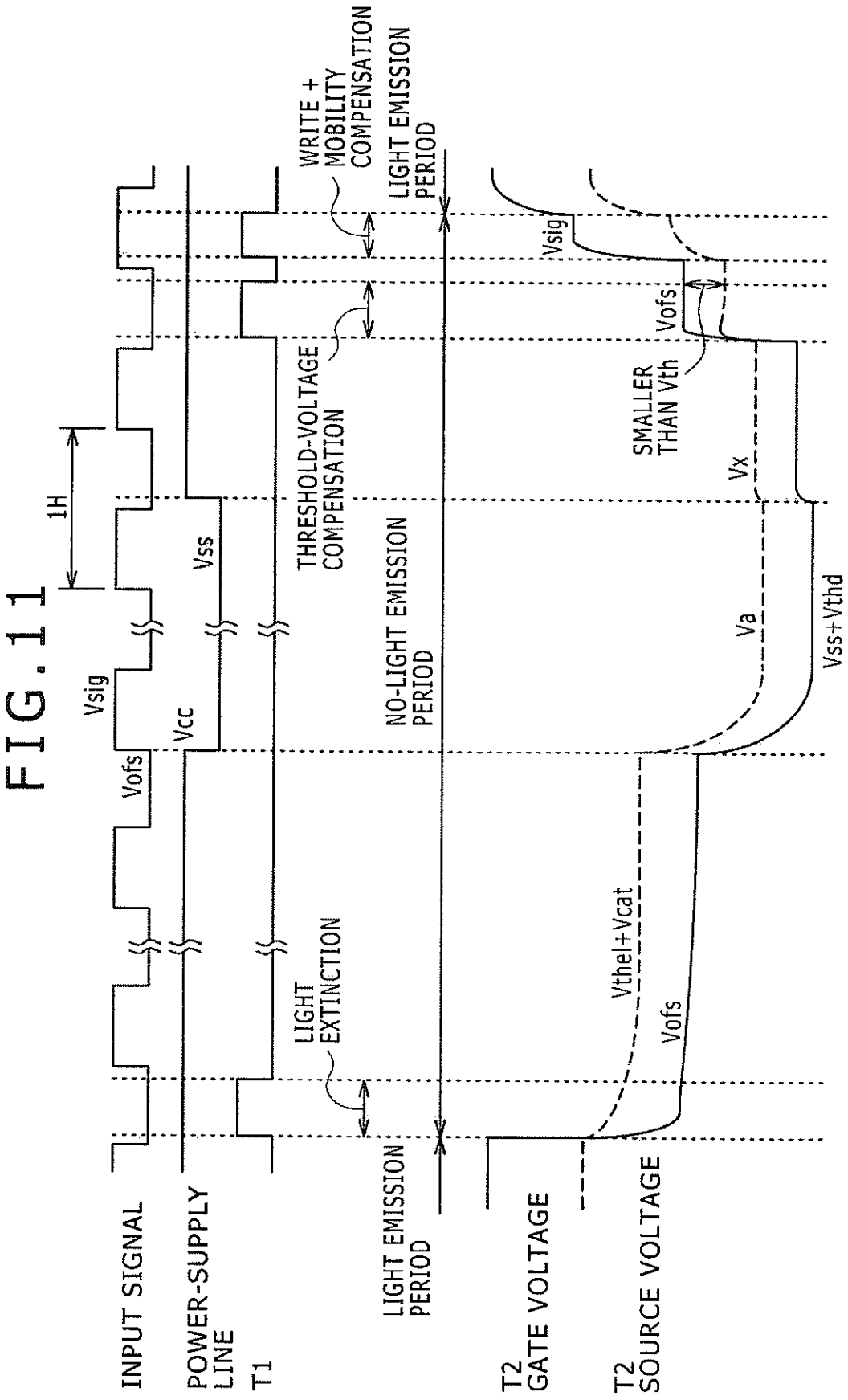

INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
1H
Vsig
Vofs
Vcc
Vss
LIGHT EXTINCTION
THRESHOLD-VOLTAGE COMPENSATION
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
NO-LIGHT EMISSION PERIOD
LIGHT EMISSION PERIOD
Vthel+Vcat
Vofs
Vsig
Vofs
SMALLER THAN Vth
Vx
Va
Vss+Vthd

FIG. 12

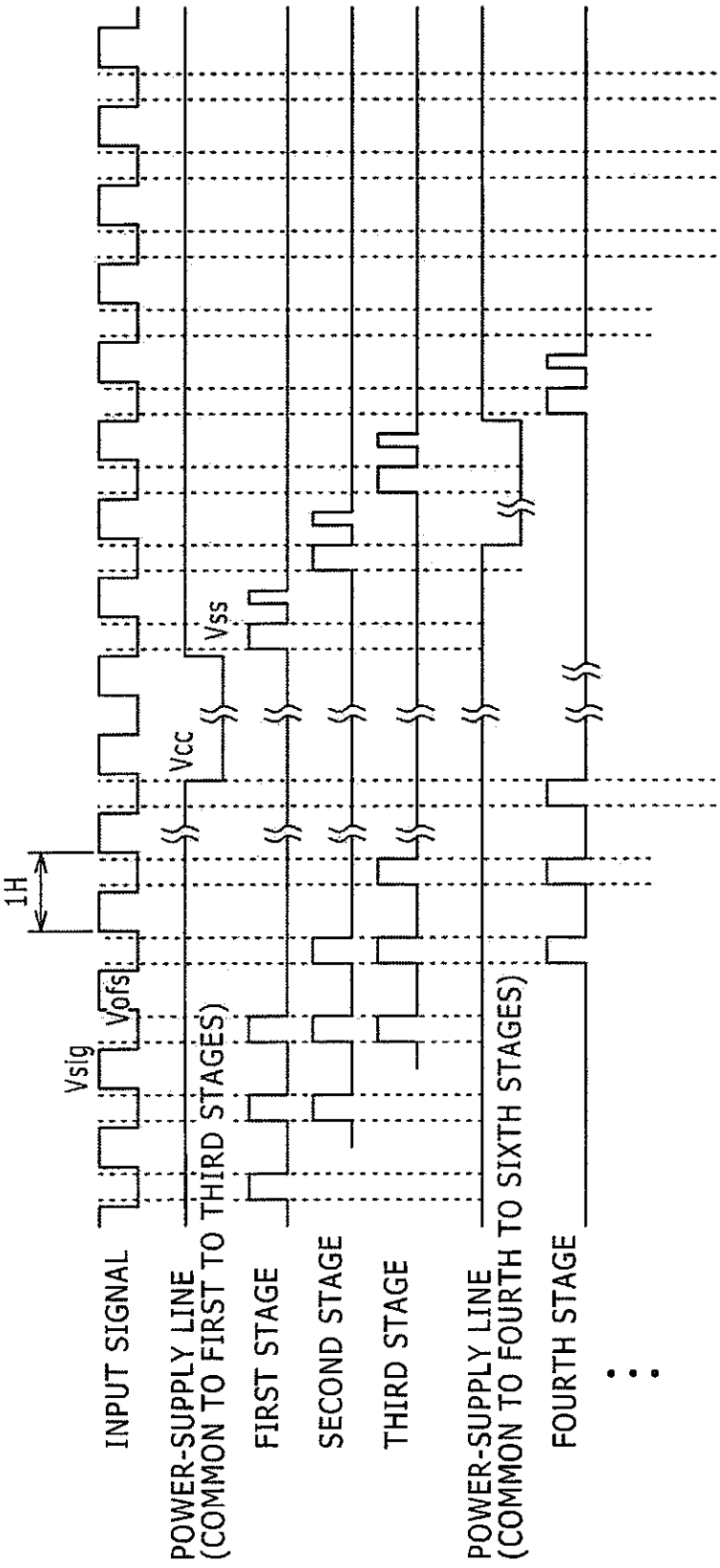

1H
Vsig
Vofs
Vcc
Vss
INPUT SIGNAL
POWER-SUPPLY LINE (COMMON TO FIRST TO THIRD STAGES)
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE (COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE
...

FIG. 13

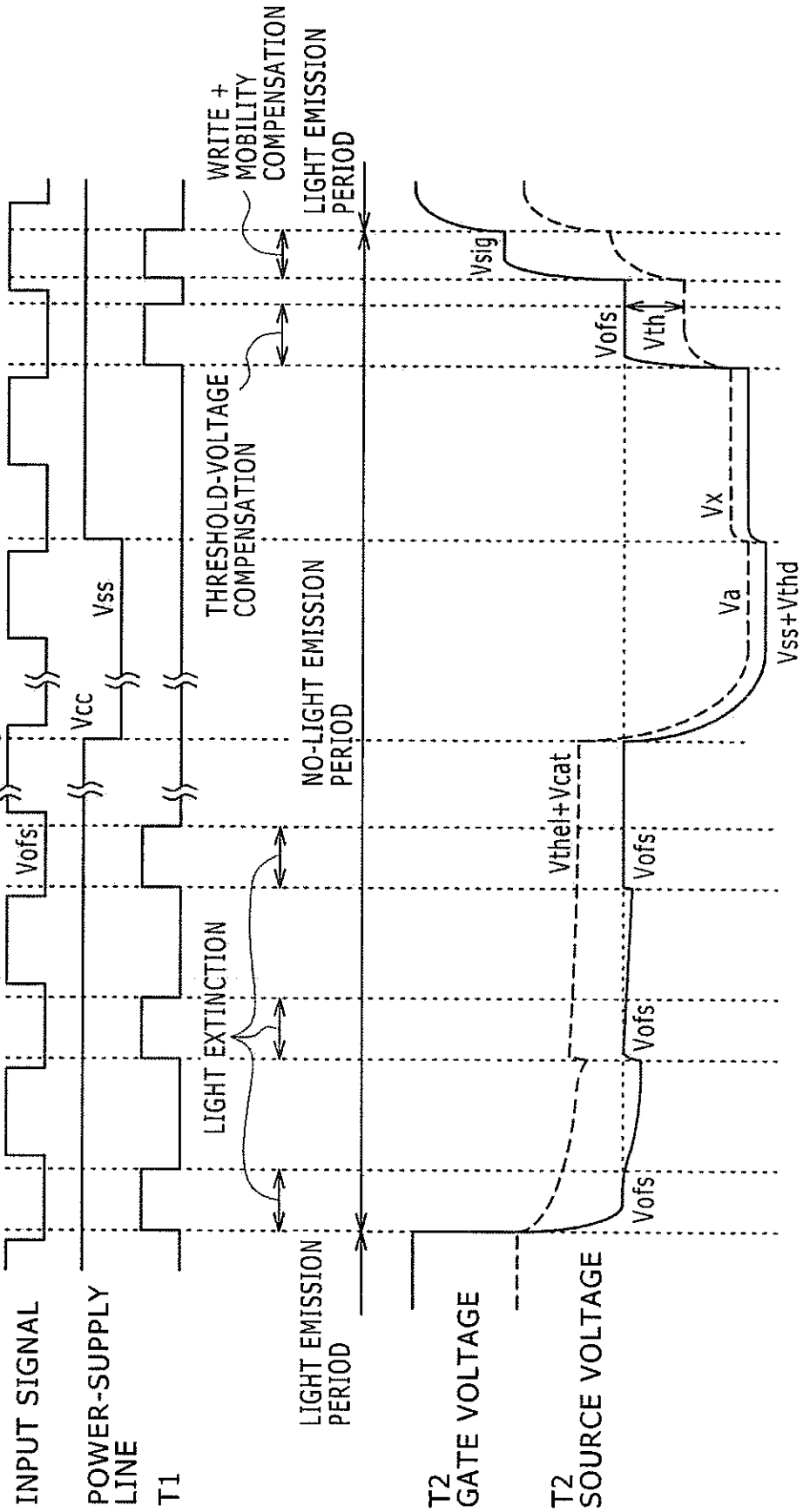

INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
1H
Vsig
Vofs
Vcc
Vss
THRESHOLD-VOLTAGE COMPENSATION
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
LIGHT EXTINCTION
NO-LIGHT EMISSION PERIOD
LIGHT EMISSION PERIOD
Vthel+Vcat
Vofs
Vofs
Vofs
Vofs
Vsig
Vofs
Vth
Vx
Va
Vss+Vthd

FIG. 14

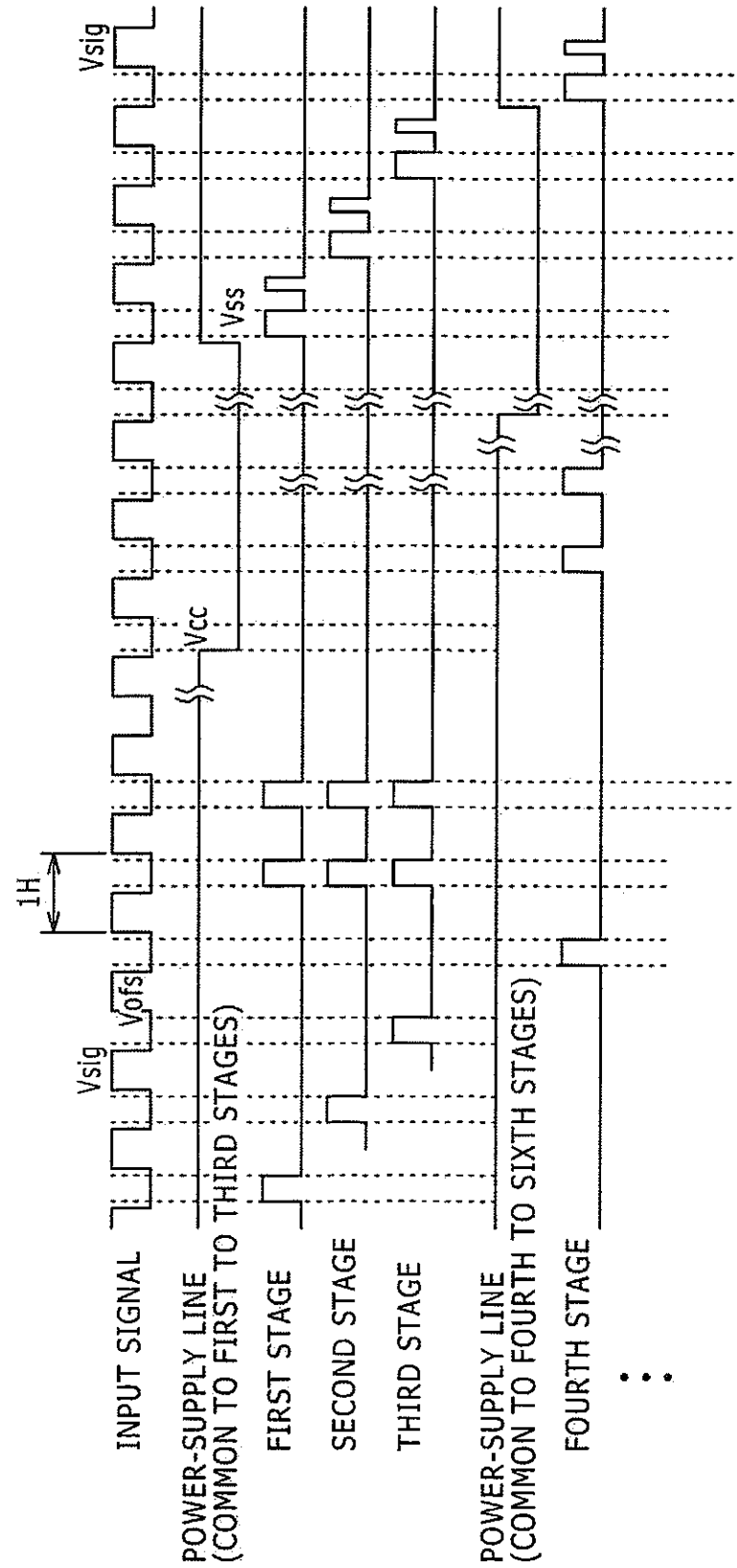

Vsig
Vofs
1H
Vcc
Vss
INPUT SIGNAL
POWER-SUPPLY LINE (COMMON TO FIRST TO THIRD STAGES)
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE (COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE
...

FIG. 15A

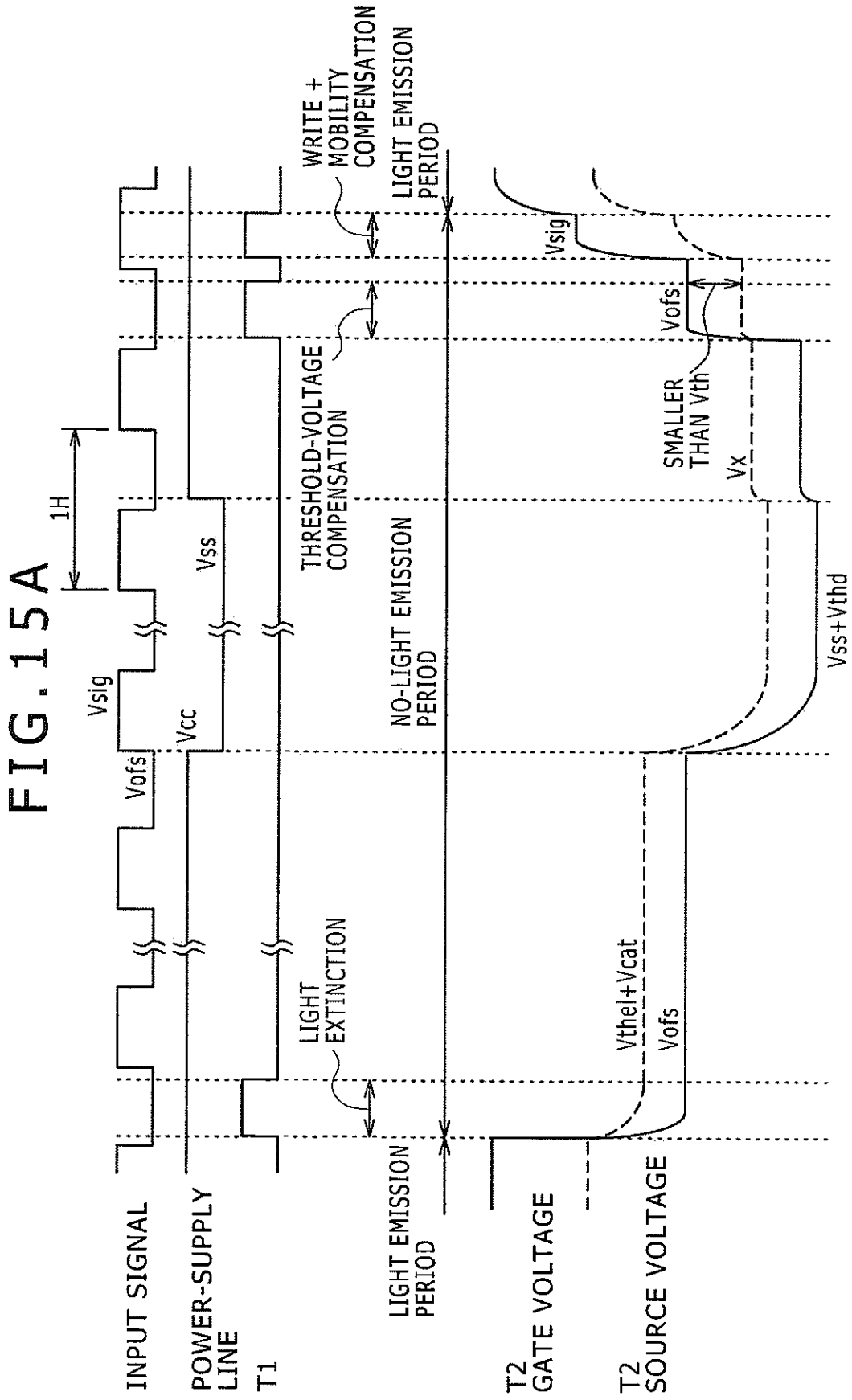

INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
1H
Vsig
Vofs
Vcc
Vss
LIGHT EXTINCTION
THRESHOLD-VOLTAGE COMPENSATION
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
NO-LIGHT EMISSION PERIOD
LIGHT EMISSION PERIOD
Vthel+Vcat
Vofs
Vsig
Vofs
SMALLER THAN Vth
Vx
Vss+Vthd

FIG.15B

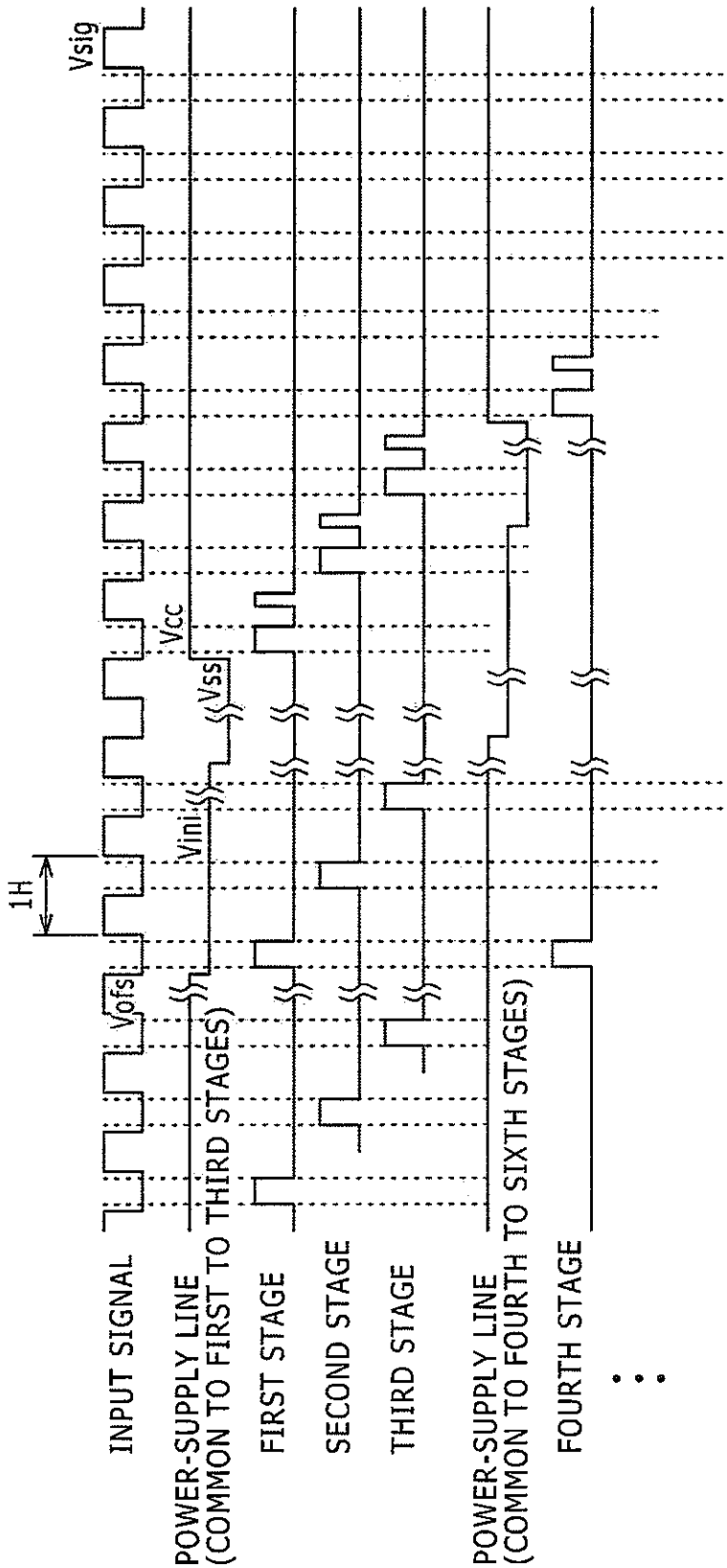

Vsig
Vcc
Vss
Vini
Vofs
1H
INPUT SIGNAL
POWER-SUPPLY LINE (COMMON TO FIRST TO THIRD STAGES)
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE (COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE

FIG. 16

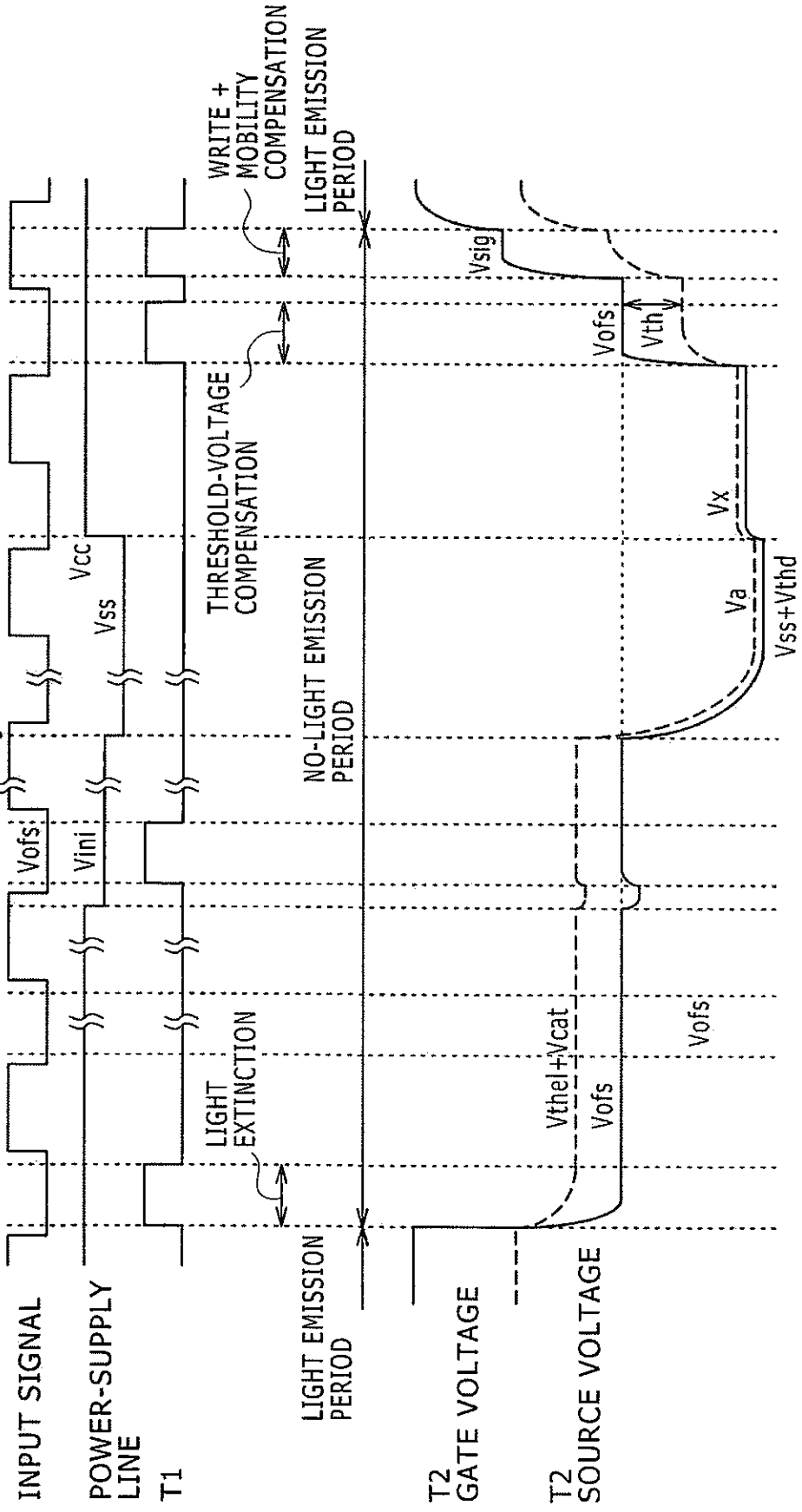

INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
1H
Vsig
Vofs
Vini
Vcc
Vss
LIGHT EXTINCTION
LIGHT EMISSION PERIOD
THRESHOLD-VOLTAGE COMPENSATION
NO-LIGHT EMISSION PERIOD
WRITE + MOBILITY COMPENSATION
LIGHT EMISSION PERIOD
Vthel+Vcat
Vofs
Vofs
Vsig
Vofs
Vth
Vx
Va
Vss+Vthd

FIG. 17

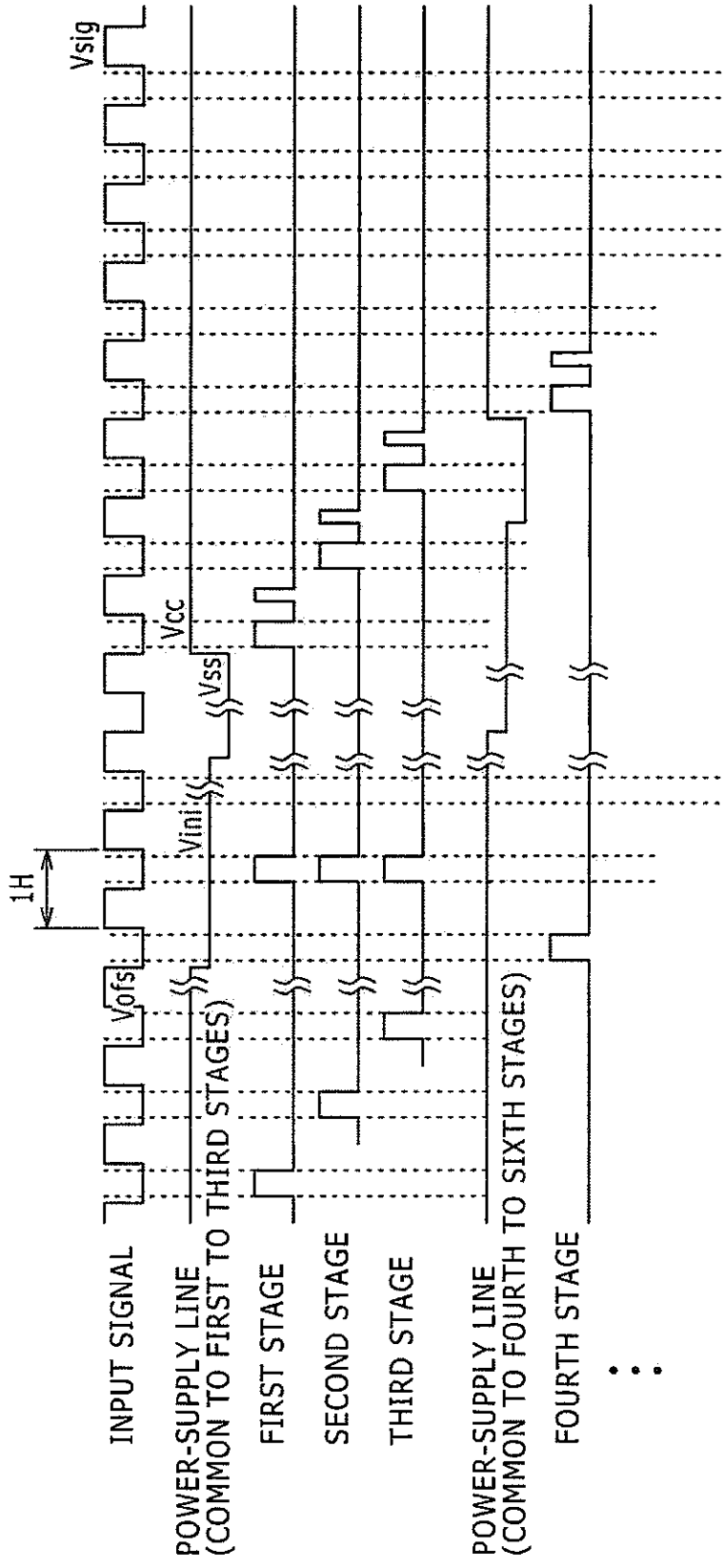

Vsig
Vofs
Vini
Vcc
Vss
1H
INPUT SIGNAL
POWER-SUPPLY LINE (COMMON TO FIRST TO THIRD STAGES)
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE (COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE
• • •

FIG. 18

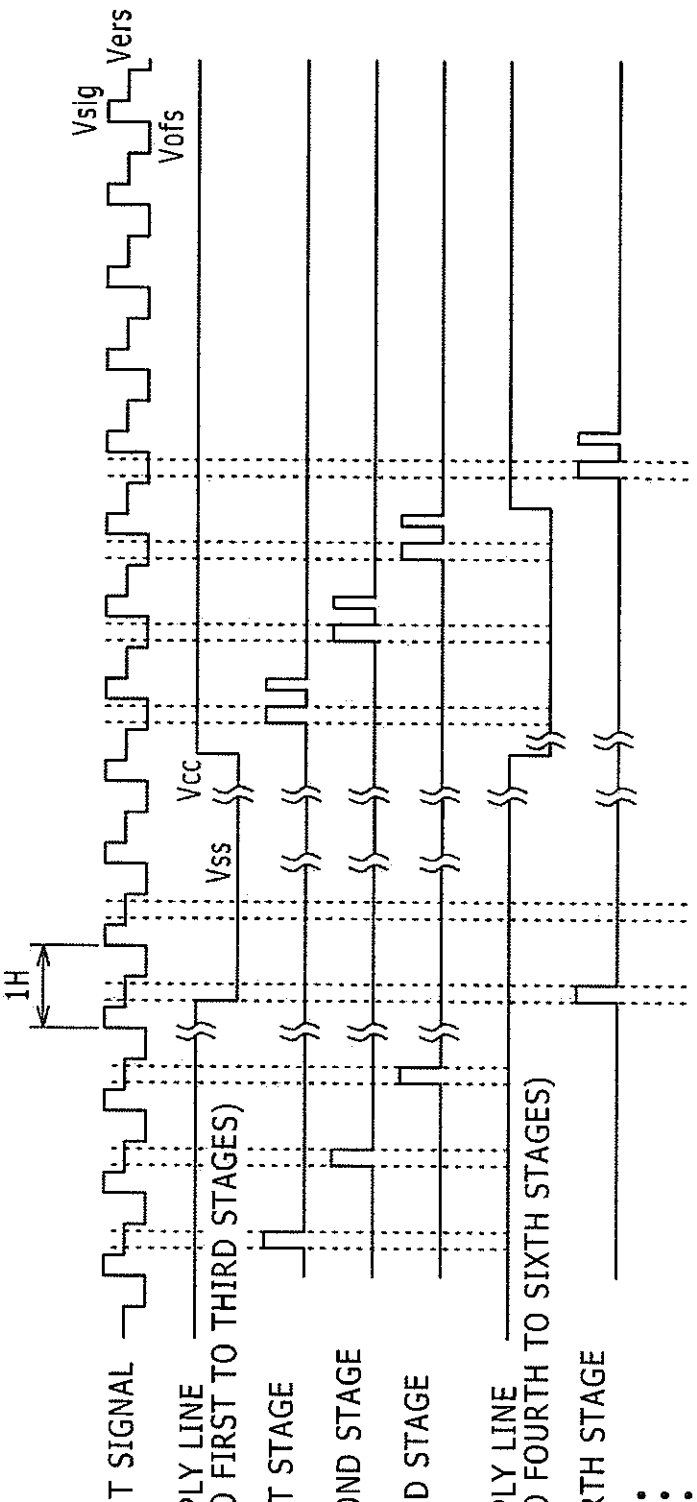

Vsig
Vers
Vofs
1H
Vcc
Vss
INPUT SIGNAL
POWER-SUPPLY LINE
(COMMON TO FIRST TO THIRD STAGES)
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE
(COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE

FIG. 19

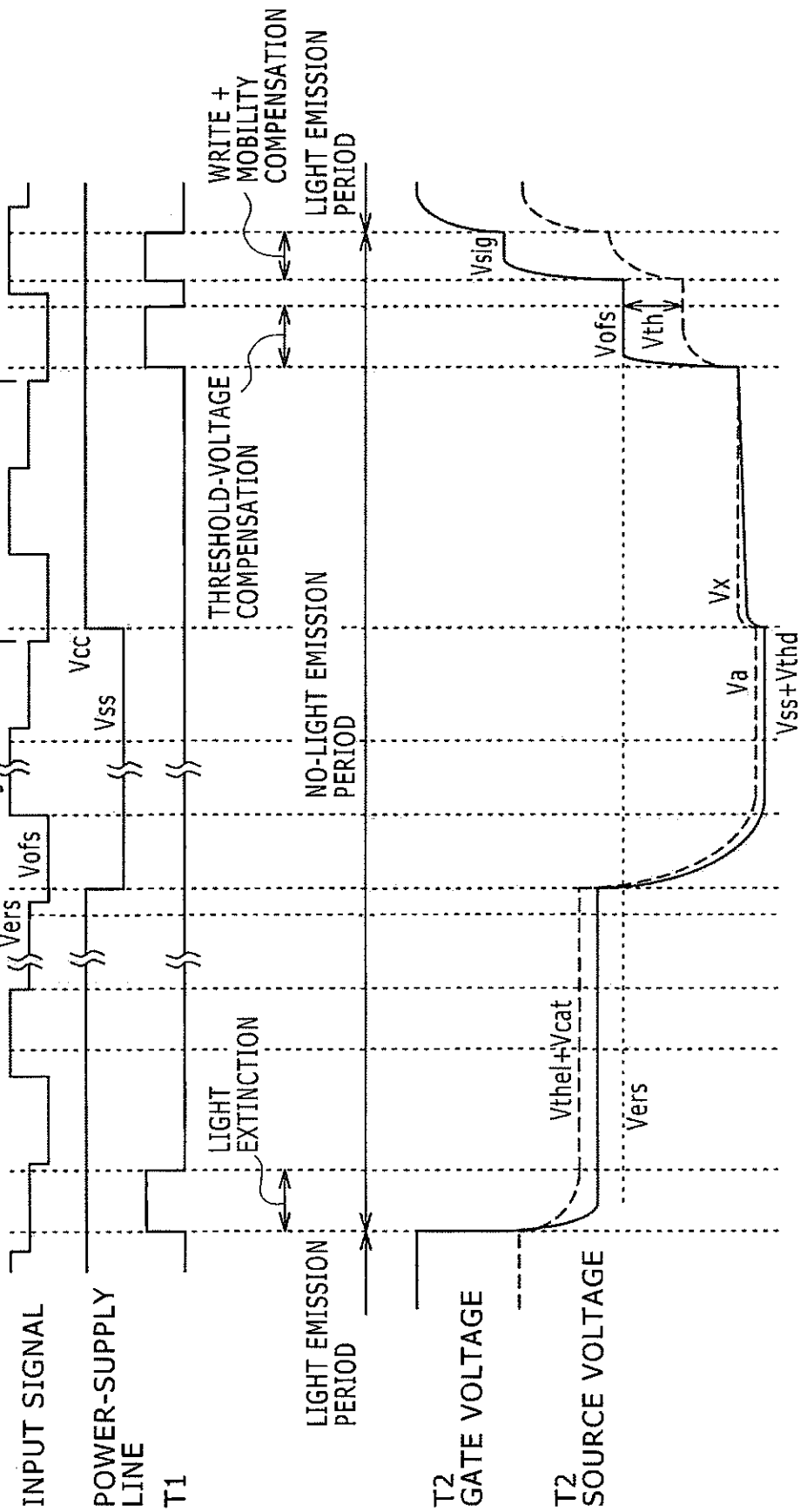

INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
1H
Vsig
Vofs
Vers
Vcc
Vss
LIGHT EXTINCTION
LIGHT EMISSION PERIOD
THRESHOLD-VOLTAGE COMPENSATION
WRITE + MOBILITY COMPENSATION
NO-LIGHT EMISSION PERIOD
LIGHT EMISSION PERIOD
Vthel+Vcat
Vers
Vsig
Vofs
Vth
Vx
Va
Vss+Vthd

FIG. 20

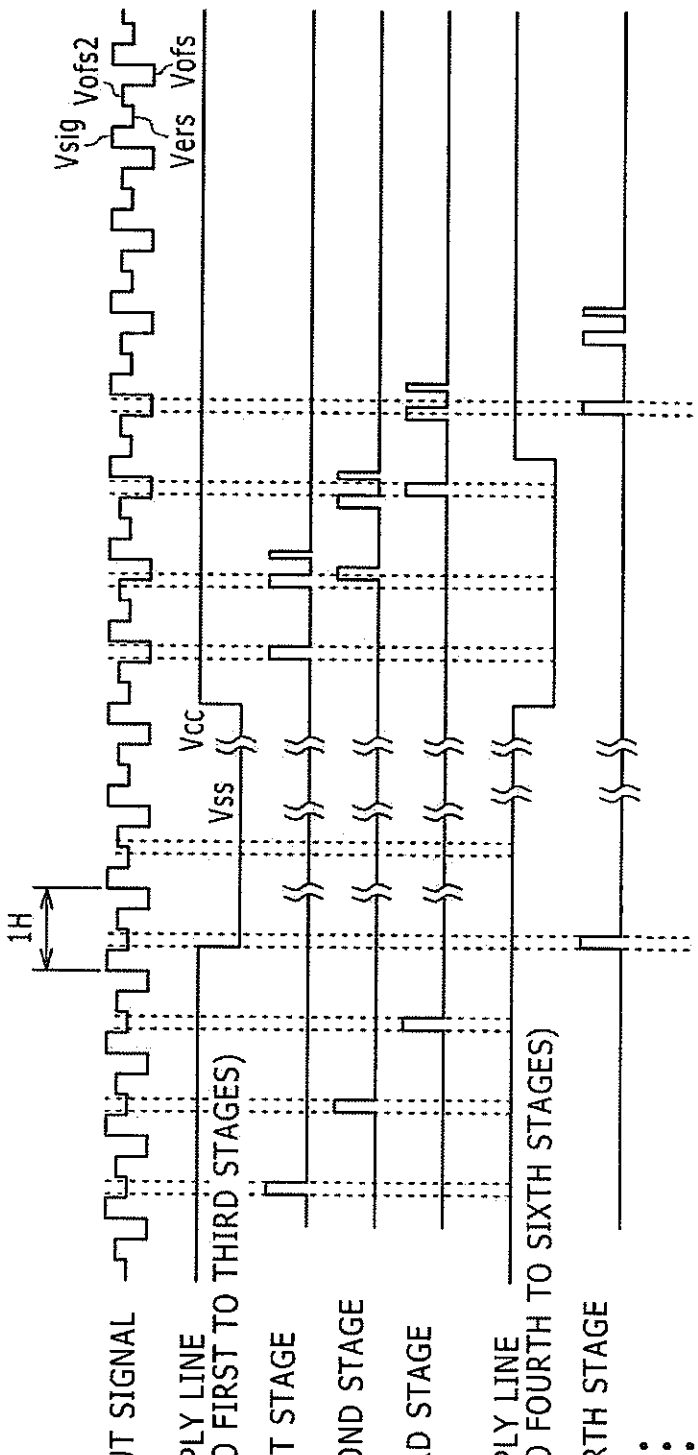

1H
INPUT SIGNAL
Vsig
Vofs2
Vers
Vofs
POWER-SUPPLY LINE
(COMMON TO FIRST TO THIRD STAGES)
Vcc
Vss
FIRST STAGE
SECOND STAGE
THIRD STAGE
POWER-SUPPLY LINE
(COMMON TO FOURTH TO SIXTH STAGES)
FOURTH STAGE
• • •

FIG. 21

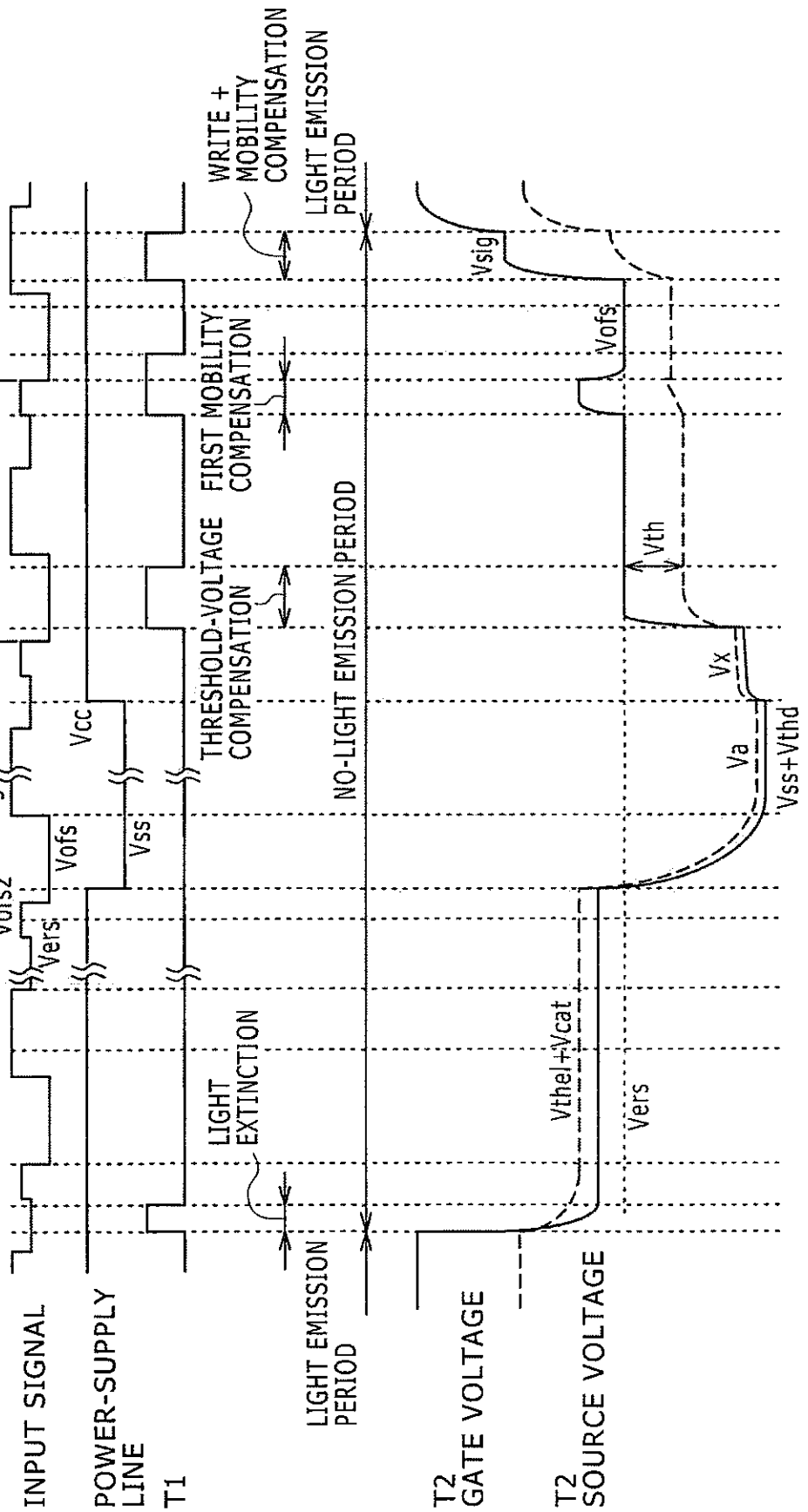

1H
INPUT SIGNAL
POWER-SUPPLY LINE
T1
T2 GATE VOLTAGE
T2 SOURCE VOLTAGE
Vofs2
Vers
Vsig
Vofs
Vss
Vcc
LIGHT EXTINCTION
LIGHT EMISSION PERIOD
THRESHOLD-VOLTAGE COMPENSATION
FIRST MOBILITY COMPENSATION
WRITE + MOBILITY COMPENSATION
NO-LIGHT EMISSION PERIOD
LIGHT EMISSION PERIOD
Vthel+Vcat
Vers
Vsig
Vofs
Vth
Vx
Va
Vss+Vthd

FIG. 22

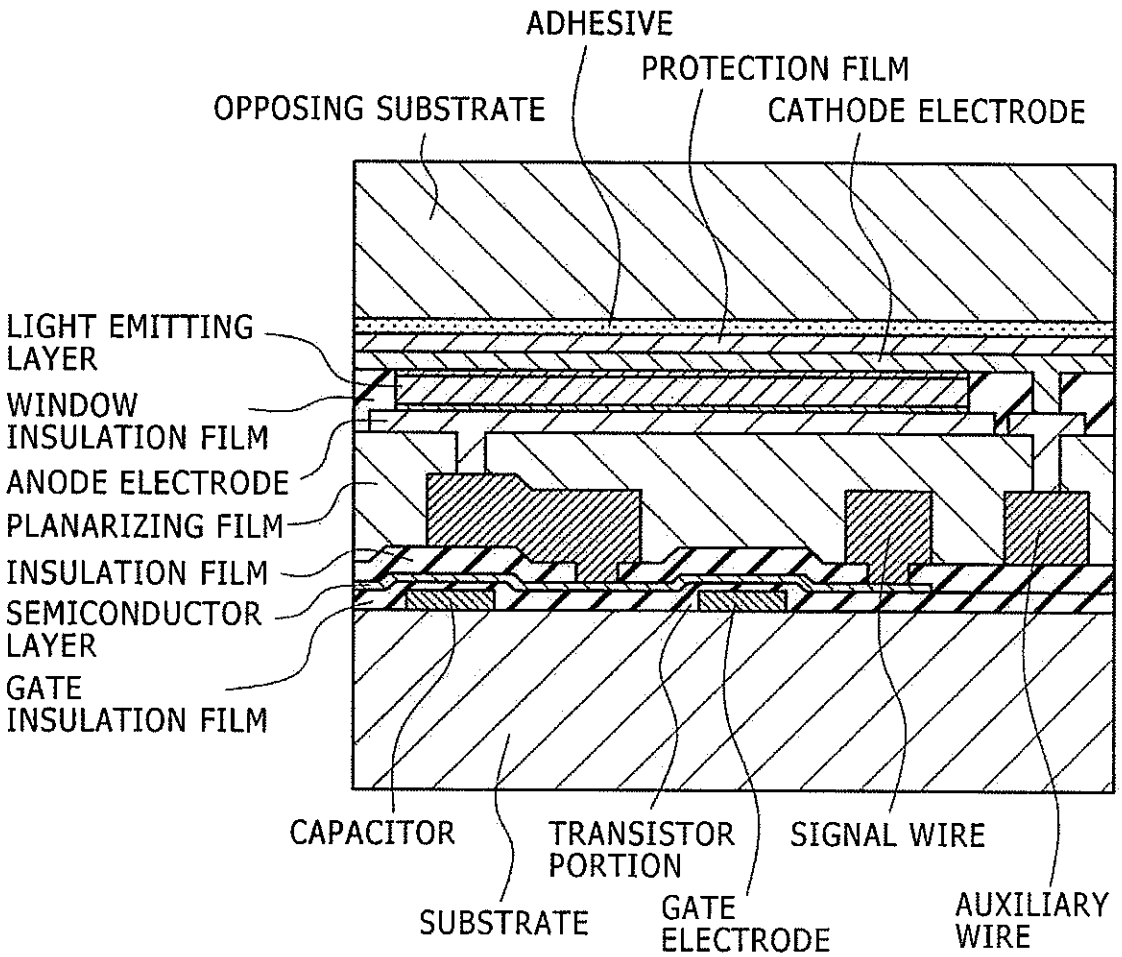

ADHESIVE
PROTECTION FILM
OPPOSING SUBSTRATE
CATHODE ELECTRODE
LIGHT EMITTING LAYER
WINDOW INSULATION FILM
ANODE ELECTRODE
PLANARIZING FILM
INSULATION FILM
SEMICONDUCTOR LAYER
GATE INSULATION FILM
CAPACITOR
TRANSISTOR PORTION
SIGNAL WIRE
SUBSTRATE
GATE ELECTRODE
AUXILIARY WIRE

FIG. 23

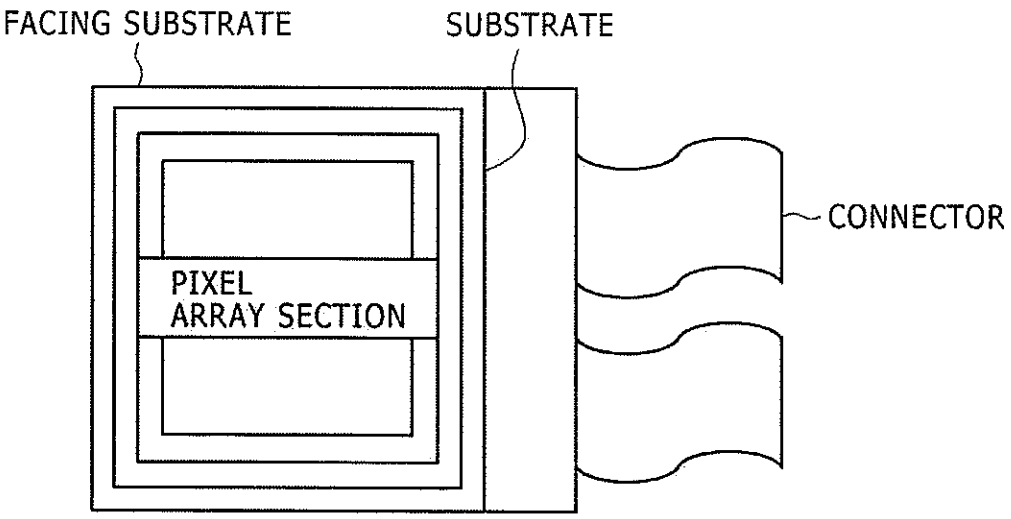

FACING SUBSTRATE
SUBSTRATE
CONNECTOR
PIXEL ARRAY SECTION

FIG.24

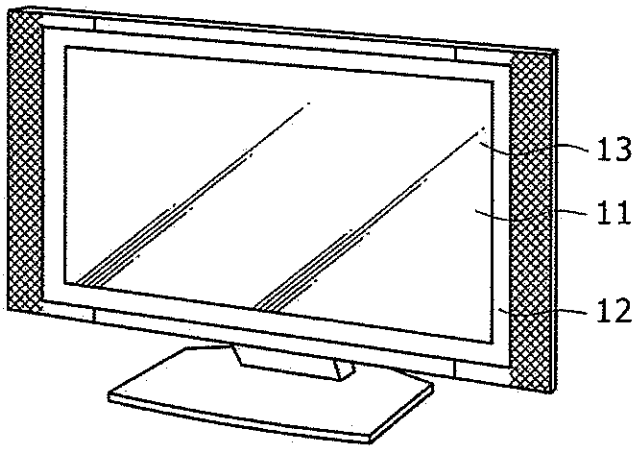
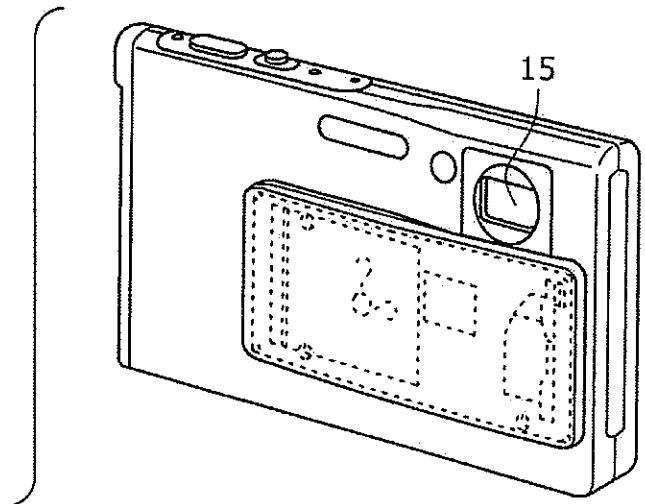


FIG.25



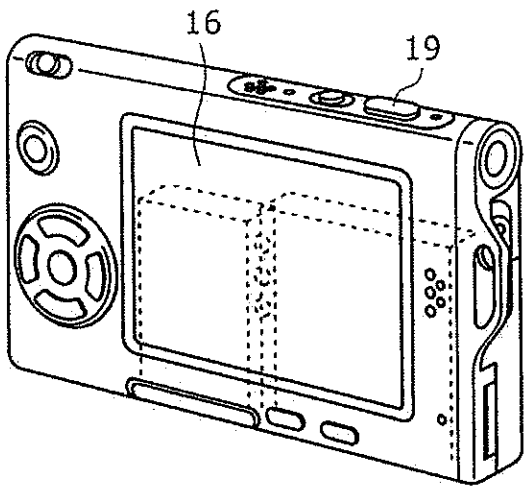


FIG.26

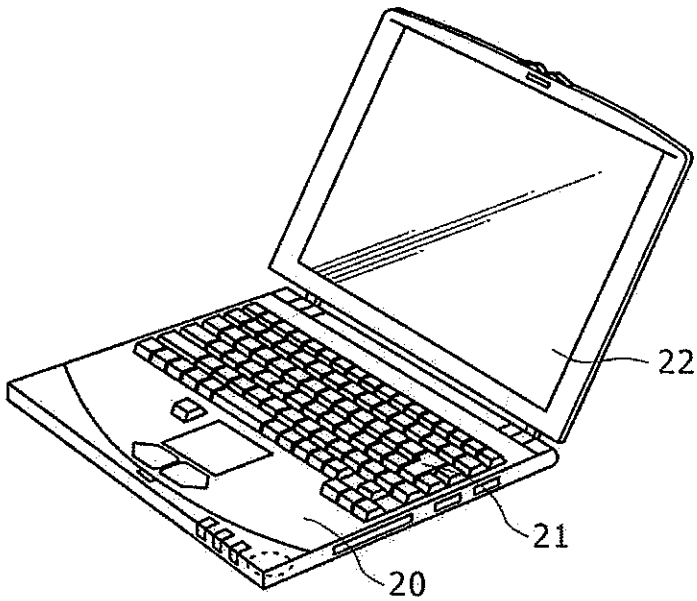


FIG.27

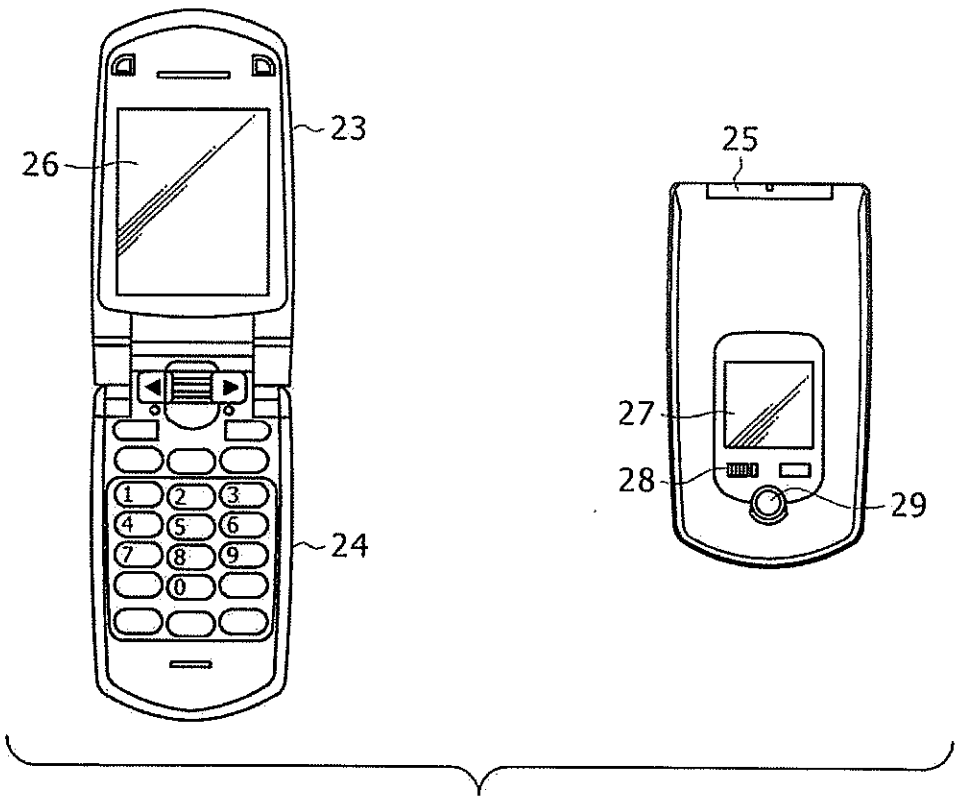


FIG.28

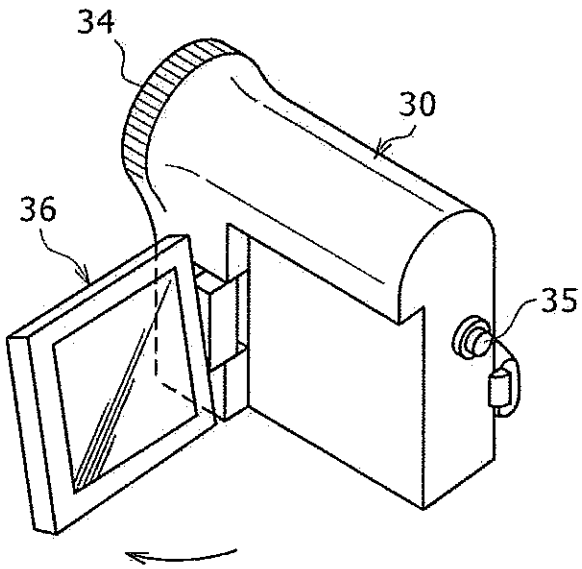


FIG. 29

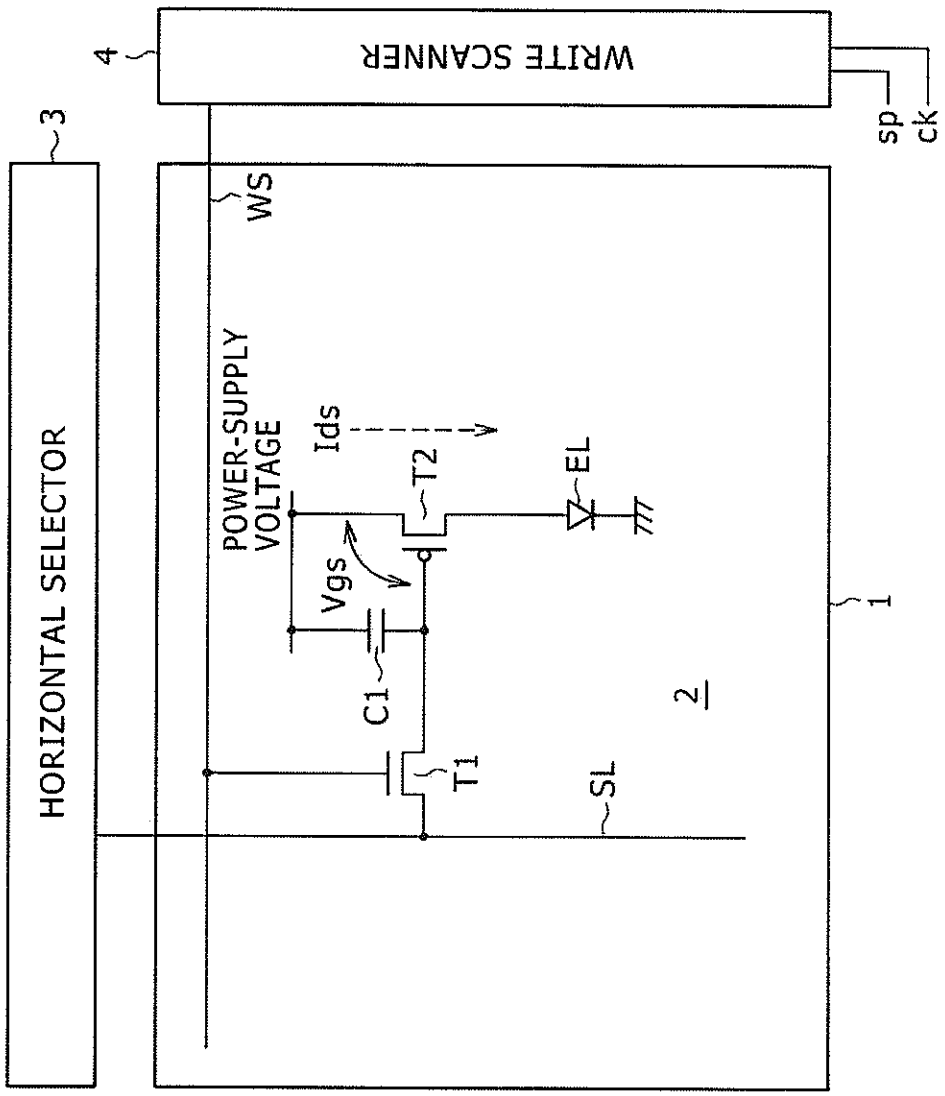

WRITE SCANNER
4
sp
ck
3
HORIZONTAL SELECTOR
WS
POWER-SUPPLY VOLTAGE
Ids
T2
EL
Vgs
C1
T1
SL
2
1

FIG.30

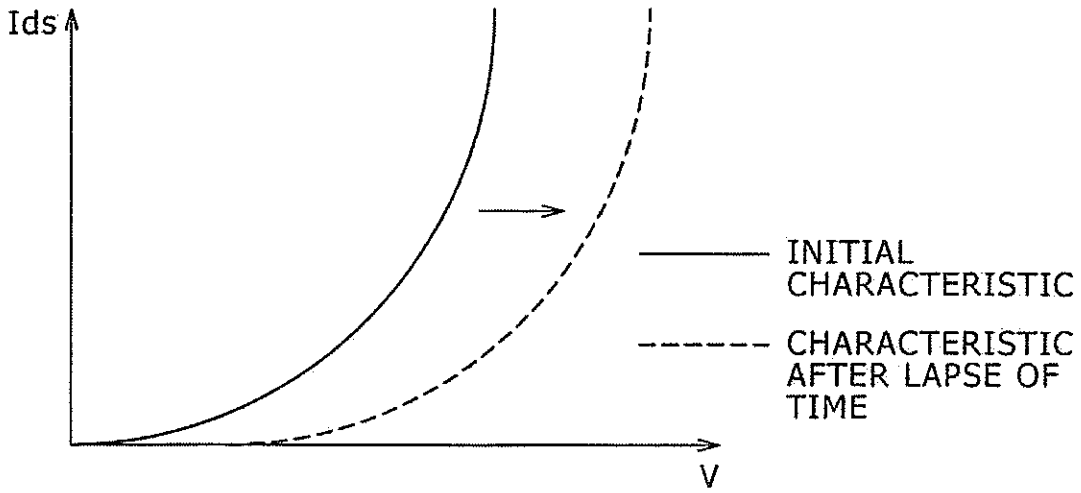
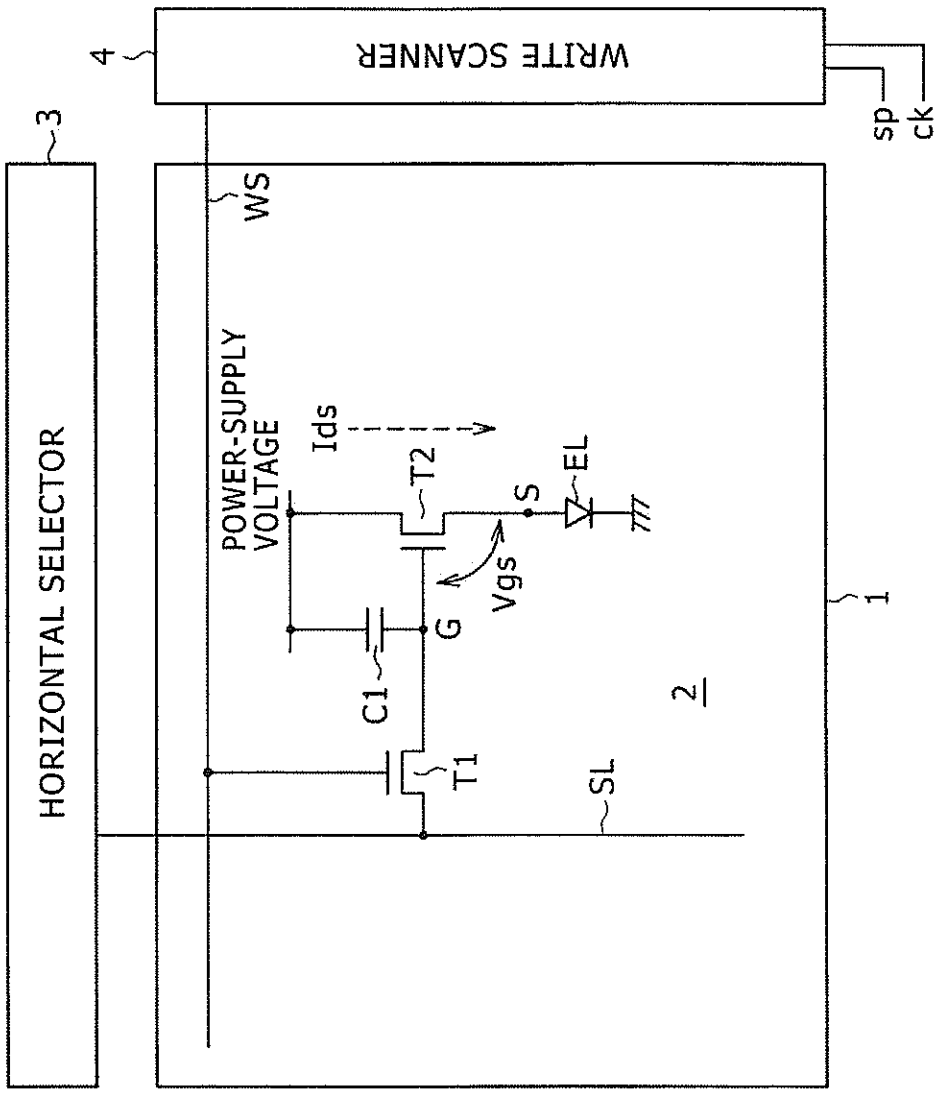

Ids
V
INITIAL CHARACTERISTIC
CHARACTERISTIC AFTER LAPSE OF TIME

FIG. 31


WRITE SCANNER
4
sp
ck
3
HORIZONTAL SELECTOR
WS
POWER-SUPPLY VOLTAGE
Ids
T2
S
EL
Vgs
G
C1
T1
SL
2
1