METHOD FOR BONDING TWO SUBSTRATES

The invention relates to a method for bonding two substrates, and in particular to a method wherein at least one of the two substrates may comprise processed or at least partially processed devices. This kind of bonding situation occurs, for example, in the fabrication process of backside illuminated CMOS imager structures, when a first substrate comprising the opto-electronic devices of the CMOS imager are bonded to a second substrate. After bonding, the first substrate is thinned, preferentially by grinding, so that light can enter into the device via the backside.

During bonding, the adhesion between two substrates is achieved via molecular forces (Van de Waals forces). To achieve a high quality bonding and to facilitate the subsequent thinning step, it is mandatory to obtain a high bonding energy, at least in the range of 700 to 1000 mJ/m^2 or even more. In the prior art high bonding energies are obtained by heating the assembled structure, typically over 1000°C.

Unfortunately, there are situations in which it is not possible to expose the bonded assembly to high temperature. This is the case for instance if devices are present on one of the substrates, and the standard thermal treatment to improve the bonding energy cannot be carried out. Indeed, the high temperatures of about 1000 to about 1100°C in the standard thermal treatment would have negative impacts on the functioning of the devices due to, for example, the spreading out of dopant concentrations or the diffusion of metals forming the devices. Using the mentioned temperature regime, a bonding energy in a range of 1,5J/m^2 to 2 J/m^2 has been observed.

As an alternative to high temperature annealing of the bonded assembly, it has been proposed to reach high bonding energy by surface activation steps, for instance plasma activation followed by low temperature annealing, of the surfaces to be bonded. However, it has been observed that these steps could lead to bond voids, like e.g. edge voids, thus defects at the bonded interface. It has furthermore been observed that the higher the bonding energy, the higher

the number of edge voids. This phenomenon has a negative impact on the fabrication yield, in particular in case that the non-transferred layers comprise electronic devices.

It is therefore the object of the present invention to provide a method for bonding with which satisfying bonding energies can be achieved in the absence of a high temperature thermal treatment.

This object is achieved with the method according to claim 1. The inventive method for bonding two substrates, thus comprises the steps of a) applying an activation treatment to at least one of the two substrates, and b) performing the contacting step of the two substrates under partial vacuum.

It is the surprising finding of this invention that it is the combination of the two steps a) and b) that leads to the desired level in the bonding energy, namely of the order of 700 – 1000 mJoule/m^2 with a reduced number of edge voids compared to the known bonding processes. Furthermore, by only applying a partial vacuum, which can easily be reached by using standard rough pumps only, the process is fast and easy to carry out. A high bonding quality, namely no or at least with a reduced number of edge voids, can be achieved even with two substrates having thermal expansion coefficients which are so different that the standard thermal anneal methods cannot be applied. Finally, the bonding quality observed with the inventive method is sufficient to carry out a layer transfer according to the Smart Cut™ technology, where ions are implanted into a donor wafer to define a plane of weakness. The bonded assembly comprising the donor wafer can then be split in the absence or with a reduced number of edge defects and despite relatively low temperatures.

Preferably, at least one of the two substrates can comprise processed or at least partially processed devices.

In this context, the term "device" relates to any structure on at least one of the substrates which at least partially belongs to the final devices like electronic devices or opto-electronic devices comprising, amongst others, capacitor and/or transistor structures. It is the particular advantage of the invention that it can be

applied to any bonded structure that requires high bonding energy but cannot be exposed to high temperature and/or that suffers from the presence of edge voids. This is the case when devices are present in or on one of the substrates.

According to an advantageous embodiment of the invention, the partial vacuum can have a pressure of 1 – 50 Torr (1,33mbar – 66,7mbar), preferably 1 – 20 Torr (1,33mbar – 26,6 mbar), preferably between 10 to 20 Torr (13,3mbar – 26,6 mbar). This level of vacuum can be easily and rapidly be reached with rough pumps, which at the same time have a cost advantage. There is thus no need to go up to a secondary vacuum to reach the desired bonding energy and a reduced level of defects.

Advantageously, step b) can be carried out at room temperature, in particular at a temperature in a range of 18 - 26°C. The possibility to carry out the contacting step which is under partial vacuum, at room temperature facilitates the practical realisation of the process.

Preferably, after bonding and during subsequent treatment steps, the bonded substrates are exposed to temperatures of at most 500°C, preferably at most 300°C. With the inventive method, the bonding energy is high enough for the subsequent treatments and at the same a reduced number of bonding voids compared to the prior art is observed, which in turn improves the bonding. Furthermore a degradation of devices like back side imagers in already processed layers, e.g. due to diffusion of metals, fusion of metallic lines and/or contacts can be prevented.

According to a preferred embodiment, the activation treatment can comprise at least one of a plasma activation, a polishing step, a cleaning step and a brushing step of the surface/s to be bonded. In this context, it is further preferred that the activation treatment for a substrate without processed or at least partially processed devices comprises a cleaning step, a plasma activation, a cleaning step and a brushing step, in this order. Furthermore, concerning the activation treatment for a substrate with processed or at least partially processed devices, the activation treatment can preferably comprise a polishing step and a cleaning step in this order. Further preferred, the activation treatment can further

comprise a plasma activation step and/or brushing step after the cleaning. With these treatments, further optimised results concerning the bonding energy are achievable.

According to an advantageous embodiment, the contacting step can be carried out in a dry atmosphere, in particular with less than 100 ppm H_2O molecules. The dry atmosphere further reduces the occurrence of defects, in particular of edge voids.

More advantageously, the contacting step can be carried out in a neutral atmosphere, in particular in an argon and/or nitrogen atmosphere.

According to a preferred variant, the inventive method can further comprise the step of providing a dielectric layer, in particular an oxide layer, over the processed devices wherein bonding occurs between the surface of the dielectric layer and one surface of the second substrate. This dielectric layer can, for instance, be a PECVD deposited oxide which, furthermore, is planarised to represent a surface roughness of less than 5 Å RMS. Thus, bonding can be carried out independently of the topology of the processed device structures on at least one of the substrates under predetermined conditions.

Preferably, the inventive method can comprise an additional step of thinning at least one of the two substrates after bonding. As a consequence of the high bonding energy achieved and the reduced number of bonding voids according to the inventive method, it is thus possible to carry out the thinning after bonding even after a limited thermal treatment.

Finally, the invention also relates to opto-electronic devices provided on substrates fabricated according to one of the above-described methods.

Advantageous embodiments of the invention will now be described in detail with respect to the following Figures:

Figures 1a – 1g illustrate one embodiment of the bonding method according to the invention.

Figure 1a illustrates a first substrate 1, which is also called a donor substrate. In this embodiment, the donor substrate is a silicon on insulator wafer with a silicon layer 3 provided on a buried oxide layer 5 in turn provided on a base substrate 7, e.g. a silicon wafer. Instead of an SOI substrate, any other suitable substrate such as a plain silicon wafer, a germanium arsenide wafer or a germanium on insulator, etc. can be used as the first substrate 1. Processed devices 9, such as electronic devices or opto-electronic devices, already have been fabricated in and/or on the semiconductor layer 3 of the first substrate 1. Typically, the semiconductor layer 3, together with the devices 9, has a thickness of about 2 to 30 µm, for instance 15 µm. The devices 9 present on the first substrate 1 can be completely processed or only partially processed, meaning that, in subsequent process steps, the devices will be finalised, e.g. by provided electric connections etc.

Figure 1b illustrates the next step of the method which consists in providing a dielectric layer 11, for example an oxide, on the devices 9. The dielectric layer 11 in this embodiment is deposited using a suitable process, like plasma enhanced CVD. Following the deposition of this layer 11, a planarisation step is carried out, e.g. using chemical mechanical polishing CMP, to obtain a surface roughness of less than 5 Å RMS, so that the dielectric layer 11 can serve as a leveling layer.

Figure 1c illustrates a second substrate 13, here called the support substrate, which is typically a silicon wafer, but could also be out of any other suitable material. Prior to bonding, an oxidation step is carried out to provide an oxide layer 15 on the support substrate 13 with a thickness of about 0.5 – 2.5 µm. Alternatively, the subsequent bonding is performed without any oxide formation step or by depositing the oxide on the support substrate.

The donor substrate 1 with the devices and the dielectric layer 11 and/or the support substrate 13 with its oxide layer 15, as illustrated in Figure 1d, are then activated.

In the case of the donor substrate 1 activation, first of all a further second polishing step is carried out. The removal of material is typically less than 1

micron or even less than 0.3 micron so that the surface is activated and prepared for bonding. The polishing step is followed by a cleaning step, which can for instance comprise scrubbing of the surface and SC1 cleaning to remove particles or polishing slurry residue. These steps are carried out on the surface of the dielectric layer 11, which represents the surface at which bonding will occur in the subsequent process step. In some instances, however, this polishing step can be omitted.

According to a variant, the donor substrate's activation can be complemented by a plasma activation using an O_2 and/or N_2 plasma with or without a subsequent brushing step. This step e.g. consist in the exposure of the donor substrates surface to be bonded to an oxygen plasma or a plasma containing O_2. The plasma exposure tool can be, for example, a Reactive Ion Etching tool, with a plasma power of about 100 W to 1000 W for a 200 mm wafer and a plasma pressure of about 1 to 100mTorr (1,33mbar to 133mbar).

The support substrate 13 activation in turn consists in cleaning of the surface, for instance using SC1 30 to 80°C for about 10min, an O_2 and/or N_2 plasma activation under the same conditions as mentioned above, a further cleaning and a final brushing step of the surface of oxide layer 15 at which bonding will occur in a subsequent process step.

The role of the activation process step is to prepare the surfaces for bonding so that high bonding energies can be achieved.

Subsequently, illustrated in Figure 1e, the first and second substrates are placed into a bonding chamber 17 with the surface 19 of the oxide layer 15 on the support substrate 13 facing the surface 21 of the dielectric layer 11 on the donor substrate 1. Typically, both substrates are aligned with respect to their notches. After the introduction of the substrates and their alignment, the chamber is closed and pumped down to a vacuum in the order of 1 – 50 Torr, preferably 1 – 20 Torr, and even preferably between 10 to 20 Torr. Typically, this takes about 2 – 3 minutes and, for the purpose of the invention, this level of partial vacuum provides the increase in bonding energy in a reasonable time, e.g. compared to

high or ultra high vacuum. Furthermore less sophisticated vacuum pumps, like primary rough pumps are sufficient to carry out the invention.

The atmosphere in the bonding chamber in the embodiment is essentially composed of a dry atmosphere, in particular with less than 100 ppm H_2O molecules, and/or further preferred of a neutral atmosphere, composed for instance of argon and/or nitrogen. The bonding chamber is kept at room temperature, thus in a range of 18°C to 26°C.

When the desired pressure level is reached, the two surfaces 19 and 21 are brought into contact, as illustrated in Figure 1f, and bonding is initiated. Typically, bonding starts at one point and a bonding wave spreads out so that, in the end, surfaces 19 and 21 are attached to each other via molecular adhesive forces (van der Waals forces) and form a donor-support compound 23. The initial contact can be achieved by applying a slight pressure on the side or in the centre, for instance by a mechanical finger.

With the described bonding method, due to the advantageous synergistic effects of carrying out the surface activation steps in combination with the contacting under partial vacuum, bonding energies in a range of at least 700 – 1000 mJoule/m^2 with a reduced level of or even without bonding defects are achieved. In addition, these results are achieved without having to carry out a post-bonding anneal at high temperatures of greater than 500°C. It has been observed that the occurrence of edge voids can be suppressed or limited (by at least one order of magnitude compared to the prior art bonding methods) except for voids arising from the presence of particles on one of the surfaces before bonding.

According to a variant of the embodiment, the donor substrate 1 can be thinned down, as illustrated in Figure 1g. Thinning can be achieved by a grinding and/or a polishing step, followed by a chemical etch that stops on the buried oxide 5 of the initial SOI donor substrate 1. Eventually, additional finishing steps, such as edge polishing and/or grinding, can be performed. The thinning does not necessarily stop at the buried oxide 5. According to further variants, even this oxide layer 5 could also be removed. In this layer 3 and eventually 5 are transferred on the second substrate. In this case, the inventive bonding method

shows further advantageous effects as, again due to the high bonding energy achieved, the edge of the transferred layer is of high quality, it shows a regular outline, no cracking or tearing off on the edge of the wafer due to the mechanical thinning of the donor wafer.

As illustrated in Figure 1g, the initial devices 9 of the SOI device layer 3 have now been transferred onto the support substrate 13. To complete the devices, additional processing steps, such as electrical connection etc, can be performed.

In addition, the structure 25 of Figure 1g might serve as a support substrate 13 in subsequent fabrication process steps. In this case, both the donor substrate and the support substrate can comprise devices.

In opto-electronic applications, the structure as illustrated in Figure 1g will receive light via the buried oxide layer 5 so that it impinges on the backside of electronic devices 9.

According to a variant, the thinning could also be achieved using a Smart Cut™ approach. In this case, prior to bonding, light species such as helium or hydrogen are implanted into the donor substrate 1 to form a predetermined splitting area. Splitting is then achieved during or after the exposition of the bonded 23 assembly, as illustrated in Figure 1f to higher than room temperature, e.g. in a range of 300 - 500°C.

In this embodiment the first substrate 1 carries already devices 9 on it. The invention is nevertheless not limited to this kind of situation as any substrate with our without device structures can be processed according to the invention and thus achieve high bonding energy and reduced edge void concentration.

Claims

1. Method for bonding two substrates comprising the steps of:
   a) applying an activation treatment to at least one of the two substrates
   b) performing a contacting step of the two substrates under partial vacuum.

2. Method according to claim 1, wherein at least one of the two substrates comprises processed or at least partially processed devices.

3. Method according to claim 1, wherein the partial vacuum has a pressure of 1 – 50 Torr (1,33mbar – 66,7mbar), preferably 1 – 20 Torr (1,33 mbar – 26,6 mbar), even preferably between 10 to 20 Torr (13,3 mbar – 26,6 mbar).

4. Method according to one of claims 1 to 3, wherein step b) is carried out at room temperature, in particular at a temperature in a range of 18°C to 26°C.

5. Method according to one of claims 1 to 4, wherein after bonding and during subsequent treatment steps, the bonded substrates are exposed to temperatures of at most 500°C, in particular at most 300°C.

6. Method according to one of claims 1 to 5, wherein the activation treatment comprises at least one of a plasma activation, a polishing step, a cleaning step and a brushing step of the surface/s to be bonded.

7. Method according to claim 6, wherein the activation treatment for a substrate without processed or at least partially processed devices comprises a cleaning step, a plasma activation, a cleaning step and a brushing step in this order.

8. Method according to claim 6 or 7, wherein the activation treatment for a substrate with processed or at least partially processed devices comprises a polishing step and a cleaning step in this order.

9. Method according to claim 8, wherein the activation treatment furthermore comprises a plasma activation step and/or brushing step after the cleaning.

10. Method according to one of claims 1 to 9, wherein the contacting step is carried out in a dry atmosphere, in particular with less than 100ppm H_2O molecules.

11. Method according to one of claims 1 to 10, wherein the contacting step is carried out in a neutral atmosphere, in particular a Ar and/or N atmosphere.

12. Method according to one of claims 1 to 11, further comprising a step of providing a dielectric layer, in particular an oxide layer over the processed devices wherein bonding occurs between the surface of the dielectric layer and one surface of the second substrate.

13. Method according to one of claims 1 to 12, further comprising a step of thinning at least one of the two substrates after bonding.

14. Opto-electronic device comprising a substrate fabricated according to one of claims 1 – 13.