CLAIMS

1. An arithmetic logic unit in a processor, wherein the arithmetic logic unit comprises a floating-point number decomposition circuit, a second-precision multiplier, and an accumulator;

the floating-point number decomposition circuit is configured to decompose each input to-be-computed first-precision floating-point number into at least two second-precision floating-point numbers, wherein precision of the second-precision floating-point number is lower than precision of the first-precision floating-point number;

the second-precision multiplier is configured to: receive a combination comprising two second-precision floating-point numbers obtained by decomposing different first-precision floating-point numbers, perform a multiplication operation on the second-precision floating-point numbers in each combination, and output an intermediate computation result corresponding to each combination; and

the accumulator is configured to perform an operation to obtain a computation result for the plurality of to-be-computed first-precision floating-point numbers based on the intermediate computation result corresponding to each combination;

wherein the arithmetic logic unit further comprises an exponent adjustment circuit;

the floating-point number decomposition circuit is further configured to output, to the exponent adjustment circuit, an exponent bias value corresponding to each second-precision floating-point number;

the second-precision multiplier is further configured to output, to the exponent adjustment circuit, the intermediate computation result corresponding to each combination; and

the exponent adjustment circuit is configured to: adjust, based on the exponent bias value corresponding to the second-precision floating-point number in each input combination, an exponent of the intermediate computation result corresponding to each input combination; and output an adjusted intermediate computation result to the accumulator.

2. The arithmetic logic unit according to claim 1, wherein the operation is a summation operation.

3. The arithmetic logic unit according to claim 1, wherein the exponent adjustment circuit is configured to: add the exponent bias value corresponding to the second-precision floating-point number in each input combination and the exponent of the intermediate computation result corresponding to each input combination, and output the adjusted intermediate computation result to the accumulator.

4. The arithmetic logic unit according to claim 1, wherein the intermediate computation result is a first-precision intermediate computation result, and the computation result is a first-precision computation result.

5. The arithmetic logic unit according to claim 4, wherein the first-precision floating-point number is a single-precision floating-point number, the second-precision floating-point number is a half-precision floating-point number, the first-precision intermediate computation result is a single-precision intermediate computation result, the first-precision computation result is a single-precision computation result, and the second-precision multiplier is a half-precision multiplier; or

the first-precision floating-point number is a double-precision floating-point number, the second-precision floating-point number is a single-precision floating-point number, the first-precision intermediate computation result is a double-precision intermediate computation result, the first-precision computation result is a double-precision computation result, and the second-precision multiplier is a single-precision multiplier.

6. The arithmetic logic unit according to claim 1, wherein the arithmetic logic unit further comprises a format conversion circuit;

the second-precision multiplier is specifically configured to: perform a multiplication operation on the second-precision floating-point numbers in each combination, and output, to the format conversion circuit, a first-precision intermediate computation result corresponding to each combination;

the format conversion circuit is configured to: perform format conversion on each input first-precision intermediate computation result, and output, to the exponent adjustment circuit, a third-precision intermediate computation result corresponding to each combination, wherein precision of the third-precision intermediate computation result is higher than precision of the first-precision intermediate computation result;

the exponent adjustment circuit is configured to: adjust, based on the exponent bias value corresponding to the second-precision floating-point number in each input combination, an exponent of the third-precision intermediate computation result corresponding to each input combination; and output an adjusted third-precision intermediate computation result to the accumulator; and

the accumulator is configured to: perform a summation operation on the adjusted third-precision intermediate computation results corresponding to all the input combinations, and output a third-precision computation result for the plurality of first-precision floating-point numbers.

7. The arithmetic logic unit according to claim 6, wherein the format conversion circuit is configured to:

perform zero padding processing on an exponent and a mantissa of each input first-precision

intermediate computation result, and output, to the exponent adjustment circuit, the third-precision intermediate computation result corresponding to each combination.

8. The arithmetic logic unit according to claim 6 or 7, wherein the first-precision floating-point number is a single-precision floating-point number, the second-precision floating-point number is a half-precision floating-point number, the first-precision intermediate computation result is a single-precision intermediate computation result, the third-precision intermediate computation result is a double-precision intermediate computation result, the third-precision computation result is a double-precision computation result, and the second-precision multiplier is a half-precision multiplier.

9. The arithmetic logic unit according to claim 1, wherein the arithmetic logic unit further comprises a format conversion circuit;

the second-precision multiplier is configured to: perform a multiplication operation on the second-precision floating-point numbers in each combination, and output, to the format conversion circuit, a third-precision intermediate computation result corresponding to each combination;

the format conversion circuit is configured to: perform format conversion on each input third-precision intermediate computation result, and output, to the exponent adjustment circuit, a first-precision intermediate computation result corresponding to each combination;

the exponent adjustment circuit is configured to: adjust, based on the exponent bias value corresponding to the second-precision floating-point number in each input combination, an exponent of the first-precision intermediate computation result corresponding to each input combination; and output an adjusted first-precision intermediate computation result to the accumulator; and

the accumulator is configured to: perform a summation operation on the adjusted first-precision intermediate computation results corresponding to all the input combinations, and output a first-precision computation result for the plurality of first-precision floating-point numbers.

10. The arithmetic logic unit according to claim 9, wherein the first-precision floating-point number is a double-precision floating-point number, the second-precision floating-point number is a half-precision floating-point number, the third-precision intermediate computation result is a single-precision intermediate computation result, the first-precision intermediate computation result is a double-precision intermediate computation result, the first-precision computation result is a double-precision computation result, and the second-precision multiplier is a half-precision multiplier.

11. The arithmetic logic unit according to any one of claims 1 to 10, wherein the arithmetic logic unit further comprises a computation mode switching circuit;

the computation mode switching circuit is configured to: when the computation mode

switching circuit is set to a second-precision floating-point number computation mode, set the floating-point number decomposition circuit and the exponent adjustment circuit to be invalid;

the second-precision multiplier is configured to: receive a plurality of groups of to-be-computed second-precision floating-point numbers that are input from the outside of the arithmetic logic unit, perform a multiplication operation on each group of second-precision floating-point numbers, and input an intermediate computation result corresponding to each group of to-be-computed second-precision floating-point numbers; and

the accumulator is configured to: perform a summation operation on the intermediate computation results corresponding to all the input groups of to-be-computed second-precision floating-point numbers, and output a computation result for the plurality of groups of to-be-computed second-precision floating-point numbers.

12. A floating-point number multiplication computation method, wherein the method comprises:

obtaining a plurality of to-be-computed first-precision floating-point numbers;

decomposing each to-be-computed first-precision floating-point number to obtain at least two second-precision floating-point numbers, wherein precision of the second-precision floating-point number is lower than precision of the first-precision floating-point number;

determining various combinations comprising two second-precision floating-point numbers obtained by decomposing different first-precision floating-point numbers;

inputting the second-precision floating-point numbers in each combination into a second-precision multiplier to obtain an intermediate computation result corresponding to each combination; and

determining a computation result for the plurality of to-be-computed first-precision floating-point numbers based on the intermediate computation result corresponding to each combination.

wherein after the decomposing each to-be-computed first-precision floating-point number to obtain at least two second-precision floating-point numbers, further comprising:

determining an exponent bias value corresponding to each second-precision floating-point number; and

the determining a computation result for the plurality of to-be-computed first-precision floating-point numbers based on the intermediate computation result corresponding to each combination comprises:

adjusting, based on the exponent bias value corresponding to the second-precision floating-point number in each combination, an exponent of the intermediate computation result corresponding to each combination, to obtain an adjusted intermediate computation result; and

performing a summation operation on the adjusted intermediate computation results

corresponding to all the combinations, to obtain the computation result for the plurality of first-precision floating-point numbers.

13. The method according to claim 12, wherein the adjusting, based on the exponent bias value corresponding to the second-precision floating-point number in each combination, an exponent of the intermediate computation result corresponding to each combination, to obtain an adjusted intermediate computation result comprises:

adding the exponent of the intermediate computation result corresponding to each combination of second-precision floating-point numbers and the exponent bias value corresponding to the second-precision floating-point number in each combination, to obtain the adjusted intermediate computation result.

14. The method according to claim 12, wherein the intermediate computation result is a first-precision intermediate computation result, and the computation result is a first-precision computation result.

15. A floating-point number multiplication computation apparatus, wherein the apparatus comprises:

an obtaining module, configured to obtain a plurality of to-be-computed first-precision floating-point numbers;

a decomposition module, configured to decompose each to-be-computed first-precision floating-point number to obtain at least two second-precision floating-point numbers, wherein precision of the second-precision floating-point number is lower than precision of the first-precision floating-point number;

a combination module, configured to determine various combinations comprising two second-precision floating-point numbers obtained by decomposing different first-precision floating-point numbers;

an input module, configured to input the second-precision floating-point numbers in each combination into a second-precision multiplier to obtain an intermediate computation result corresponding to each combination; and

a determining module, configured to determine a computation result for the plurality of to-be-computed first-precision floating-point numbers based on the intermediate computation result corresponding to each combination;

wherein the decomposition module is further configured to:

determining an exponent bias value corresponding to each second-precision floating-point number; and the determining module is configured to:

adjusting, based on the exponent bias value corresponding to the second-precision floating-point number in each combination, an exponent of the intermediate computation result

corresponding to each combination, to obtain an adjusted intermediate computation result; and

performing a summation operation on the adjusted intermediate computation results corresponding to all the combinations, to obtain the computation result for the plurality of first-precision floating-point numbers.

16. The apparatus according to claim 15, wherein the decomposition module is further configured to:

determine an exponent bias value corresponding to each second-precision floating-point number; and

the determining module is configured to:

adjust, based on the exponent bias value corresponding to the second-precision floating-point number in each combination, an exponent of the intermediate computation result corresponding to each combination, to obtain an adjusted intermediate computation result; and

perform a summation operation on the adjusted intermediate computation results corresponding to all the combinations, to obtain the computation result for the plurality of first-precision floating-point numbers.

17. An electronic device, wherein the electronic device comprises a processor and a memory, the memory stores at least one instruction, and the instruction is loaded and executed by the processor to implement an operation performed in the floating-point number multiplication computation method according to any one of claims 12 to 14.

18. A processor, wherein the processor comprises the arithmetic logic unit according to claims 1 to 11.