

PATENT SPECIFICATION

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(54) A SEMI-CONDUCTOR DEVICE AND A METHOD OF MAKING THE SAME

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:-

This invention relates to semi-conductor devices and methods of making the same.

Uptil now integrated circuitry used in electronic apparatus has been of the CMOS, IIL etc. type. Integrated circuitry has the advantage over other types of circuit construction that they have a low power consumption, a high operating speed, high reliability, low cost, and can be constructed to perform a number of different functions.

When electronic circuitry has to be accommodated in a limited spaced, for example, in an electronic wristwatch, low power integrated circuitry is the answer, particularly for increasing the operational life of a relatively small single electric cell provided to power the circuitry. At present, an electric cell having a capacity of 50m AH has a continuous operating life of about two years. However, it is desirable for such an electric cell to have a continuous operating life of between 5 and 10 years. Furthermore, in the field of electronic watches, there is a demand for greater and greater accuracy. Nowadays, an electronic watch using a quartz crystal vibrator to produce a 32 KHz standard time signal has an accuracy of about 10 seconds per month. If an AT-cut quartz crystal vibrator operating at 4MHz is used as the standard time signal source the accuracy can be brought down to within 10 seconds per year. In the case of digital watches, there is also a demand for multi-functional operation and already there is produced chronographs and world time-pieces having integrated circuitry containing 10,000 transistors. It has been realised that

these demands cannot be satisfied in the case of electronic watches using conventional integrated circuitry because they cannot operate efficiently at frequencies of 4MHz if they are of the CMOS type since the power consumption increases by a factor of 1000 compared to the power consumption at an operating frequency of 32 KHz.

Integrated circuitry of the IIL type, i.e. static logic circuitry, has a finite power consumption even when it is non-operative, this power consumption being proportional to the number of gates. The power consumption of IIL type integrated circuitry containing 10,000 gates is several tens of times greater than the power consumption of CMOS type integrated circuitry. Consequently, uptil now it has been found impossible to manufacture high performance, lower power consumption electronic watches using either CMOS type or IIL type integrated circuitry.

The present invention seeks to provide integrated circuitry for a highly efficient electronic watch or other electronic apparatus with a relatively low power consumption.

For example integrated circuitry may be produced by using a N-conductivity type semi-conductor substrate having an impurity concentration of 10^{19} and an epitaxial layer of N-conductivity type semi-conductor material having an impurity concentration of 10^{13} thereon. Such integrated circuitry may easily be made using conventional planar techniques.

According to one aspect of the present invention there is provided a semi-conductor device comprising a first junction field effect transistor, a second junction field effect transistor of opposite polarity to the first transistor, an input terminal connected to gate electrodes of the transistors, and an output terminal connected to drain electrodes thereof so that one transistor is

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rendered non-conductive when the gate voltage is equal to the source voltage thereof, and is rendered conductive when the gate voltage is equal to the source voltage of the other transistor.

Preferably the channel of the first transistor extends substantially parallel to the surface of a substrate in which it is formed and the channel of the second transistor extends substantially perpendicularly to the surface of the substrate.

The diffusion depth of the gate of the first transistor may be less than the diffusion depth of the source thereof. Similarly, the diffusion depth of the drain of the second transistor may be less than the diffusion depth of the gate thereof.

In the preferred embodiment the semiconductor device is connected to operate as an inverter.

According to a further aspect of the present invention there is provided a method of making a semi-conductor device as recited above including forming said transistors on a single substrate and diffusing into the substrate the gate of one transistor and the channel of the other transistor simultaneously.

Preferably the drain of said first transistor is diffused into the substrate simultaneously with the gate of the other transistor.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 (a) is a sectional view of an inverter according to the present invention;

Figure 1 (b) is a plan view of the inverter of Figure 1 (a);

Figure 1 (c) is a circuit diagram of the inverter of Figure 1 (a);

Figure 2 (a) is a section of a P-channel transistor forming part of the inverter of Figure 1 (a);

Figure 2 (b) is a plan view of the P-channel transistor of Figure 2 (a);

Figure 2 (c) is a circuit diagram of the P-channel transistor of Figure (a);

Figure 3 (a) is a section of an N-channel transistor forming part of the inverter of Figure 1 (a);

Figure 3 (b) is a plan view of the N-channel transistor of Figure 3 (a); and

Figure 3 (c) is a circuit diagram of the N-channel transistor of Figure 3 (a).

Referring first to Figures 1 (a) to 1 (c) there is shown one embodiment of a complementary junction field effect transistor inverter 9 according to the present invention. The inverter is composed of a P-channel transistor 7 and an N-channel transistor 8.

As shown in Figures 2 (a) to 2 (c), the P-channel transistor 7 is a lateral type conjunction field effect transistor having a gate 2 of N-conductivity type semi-

conductor material with an impurity concentration of 10^{19} . A source electrode 11 is in ohmic contact with a source 1a of P-conductivity type semi-conductor material. A channel 1b is formed in the P-conductivity type material beneath the gate 2. A drain electrode 13a is in ohmic contact with a drain 1c of P-conductivity type semi-conductor material. A gate electrode 12a is in ohmic contact with the gate 2.

As shown in Figures 3 (a) to 3 (c) the N-channel transistor 8 is a vertical type junction field effect transistor having a channel 3a of N-conductivity type semi-conductor material with an impurity concentration of 10^{18} and a gate 5 of P-conductivity type semi-conductor material with an impurity concentration of 10^{15} . A source electrode 16 is connected to an integrated circuit substrate 4, a drain electrode 13b is in ohmic contact with a drain 6 of N-conductivity type semi-conductor material and a gate electrode 12b is connected to the gate 5.

Referring back to Figures 1 (a) to 1 (c) the source electrode 11 of the P-channel transistor 7 and the source electrode 16 of the N-channel transistor 8 are connected with respective positive and negative terminals of a power supply (not shown). The drain electrodes 13a, 13b are connected to a common output electrode 13, and the gate electrodes 12a, 12b are connected to a common input electrode 12.

The inverter according to the present invention and described above operates in a similar manner to a conventional CMOS inverter. The P-channel transistor 7 is designed so that it is non-conductive by closing the channel 1b, when a gate voltage VG applied to the gate 2 is equal to the source voltage. When the impurity concentration of the channel 1b and the gate 2 are respectively 10^{15} and 10^{19} , the expansion of the depletion layer is approximately 0.89 μm . Accordingly, if the difference of the depth of diffusion Xp of the P-conductivity type semi-conductor material constituting the source 1a, the drain 1c and the channel 1b, and the depth of diffusion Xn of the N-conductivity type semi-conductor material constituting the gate 2 is smaller than 0.89 μm , the P-channel transistor 7 is rendered non-conductive.

On the other hand, when the breadth of the depletion layer is reduced by lowering the voltage VG applied to the gate 2 relative to the source voltage, the P-channel transistor 7 is rendered conductive due to the expansion of the channel 1b. When the difference (Xp, Xn) is equal to 0.8 μm , the breadth of the channel 1b is 0.23 μm by lowering the voltage VG to 0.5V relative to the source voltage.

The N-channel transistor 8 is designed so that it is non-conductive by closing the

channel 3a when the gate voltage is equal to the source voltage. If the impurity concentration of the N-conductivity type semiconductor material 3 forming the channel 3a is 10^{13} (more usually 10^{18}) and that of the P-conductivity type semiconductor material forming the gate 5 is 10^5 (more usually 10^{15}), the length l between the gate 5 is suitably chosen since the expansion of the depletion layer becomes $7.16 \mu\text{m}$ and the breadth of the channel 3a becomes $14.3 \mu\text{m}$ or less.

On the other hand, if the depletion layer of the channel 3a is reduced by raising the voltage of the gate 6 relative to the source voltage, the N-channel transistor 8 can be made conductive by the expansion of the channel 3a.

When the length l of the gate 5 is $14 \mu\text{m}$, the breadth of the channel 3a becomes $10 \mu\text{m}$ by raising the voltage to the gate 6 to 0.5V relative to the source voltage.

In the case of the inverter illustrated in the drawings, if OV is applied to the terminal 16 and 0.5V is applied to the terminal 11, and if 0.5V representing a high level signal is applied to the input terminal 12, the output terminal 13 becomes OV representing a low level signal. If OV representing a low level signal is applied to the input terminal 12, the output terminal 13 becomes 0.5V representing a high level signal.

The inverter illustrated in the drawings has the following advantages over other types of integrated circuitry:

1. The junction capacitance is small because of the low impurity concentration. In IIL type integrated circuitry a low impurity concentration semiconductor material cannot be used for base and emitter due to using bipolar transistor therein.

2. The gate capacitance does not have to be as large as that of CMOS type integrated circuitry.

3. It can be used at sufficiently low voltages since operating voltage is determined by the way in which the integrated circuitry is made.

As will be seen from the drawings the diffusion depth of the gate 2 is less than the diffusion depth of the source 1a and the channel 1c. Moreover the diffusion depth of the drain 6 is less than the diffusion depth of the gate 5. The gate 5 may be diffused into the substrate 4 simultaneously with the channel 1b and the drain 6 may be diffused simultaneously with the gate 2.

A semiconductor device or devices according to the present invention may be used in electronic wristwatches, for example, to enable high speed operation thereof because they have a small junction capacitance, are capable of driving a quartz crystal vibrator operating at 4 MHz with low power consumption and also are capable of driving

large circuitry with low power consumption since there is little static current because of the complementary structure. Therefore, by use of the present invention it is possible to achieve a highly efficient electronic wrist-watch operating a high frequency, employing highly integrated circuitry and operating with a low power consumption. It will, however, be appreciated that the present invention can be applied to other electronic apparatus apart from electronic timepieces.

WHAT WE CLAIM IS:

1. A semiconductor device comprising a first junction field effect transistor, a second junction field effect transistor of opposite polarity to the first transistor, an input terminal connected to gate electrodes of the transistors, and an output terminal connected to drain electrodes thereof so that one transistor is rendered non-conductive when the gate voltage is equal to the source voltage thereof, and is rendered conductive when the gate voltage is equal to the source voltage of the other transistor.

2. A device as claimed in claim 1 in which the channel of the first transistor extends substantially parallel to the surface of a substrate in which it is formed and the channel of the second transistor extends substantially perpendicularly to the surface of the substrate.

3. A device as claimed in claim 1 or 2 in which the diffusion depth of the gate of the first transistor is less than the diffusion depth of the source thereof.

4. A device as claimed in any preceding claim in which the diffusion depth of the drain of the second transistor is less than the diffusion depth of the gate thereof.

5. A semiconductor device as claimed in any preceding claim connected to operate as an inverter.

6. A semiconductor device as claimed in claim 1 and substantially as herein described with reference to and as shown in the accompanying drawings.

7. A method of making a semiconductor device as claimed in claim 1 including forming said transistors on a single substrate and diffusing into the substrate the gate of one transistor and the channel of the other transistor simultaneously.

8. A method as claimed in claim 7 in which the drain of said first transistor is diffused into the substrate simultaneously with the gate of the other transistor.

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channel 3a when the gate voltage is equal to the source voltage. If the impurity concentration of the N-conductivity type semiconductor material 3 forming the channel 3a is 10^{13} (more usually 10^{18}) and that of the P-conductivity type semiconductor material forming the gate 5 is 10^5 (more usually 10^{15}), the length l between the gate 5 is suitably chosen since the expansion of the depletion layer becomes $7.16 \mu\text{m}$ and the breadth of the channel 3a becomes $14.3 \mu\text{m}$ or less.

On the other hand, if the depletion layer of the channel 3a is reduced by raising the voltage of the gate 6 relative to the source voltage, the N-channel transistor 8 can be made conductive by the expansion of the channel 3a.

When the length l of the gate 5 is $14 \mu\text{m}$, the breadth of the channel 3a becomes $10 \mu\text{m}$ by raising the voltage to the gate 6 to 0.5V relative to the source voltage.

In the case of the inverter illustrated in the drawings, if OV is applied to the terminal 16 and 0.5V is applied to the terminal 11, and if 0.5V representing a high level signal is applied to the input terminal 12, the output terminal 13 becomes OV representing a low level signal. If OV representing a low level signal is applied to the input terminal 12, the output terminal 13 becomes 0.5V representing a high level signal.

The inverter illustrated in the drawings has the following advantages over other types of integrated circuitry:

1. The junction capacitance is small because of the low impurity concentration. In IIL type integrated circuitry a low impurity concentration semiconductor material cannot be used for base and emitter due to using bipolar transistor therein.

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As will be seen from the drawings the diffusion depth of the gate 2 is less than the diffusion depth of the source 1a and the channel 1c. Moreover the diffusion depth of the drain 6 is less than the diffusion depth of the gate 5. The gate 5 may be diffused into the substrate 4 simultaneously with the channel 1b and the drain 6 may be diffused simultaneously with the gate 2.

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WHAT WE CLAIM IS:

1. A semiconductor device comprising a first junction field effect transistor, a second junction field effect transistor of opposite polarity to the first transistor, an input terminal connected to gate electrodes of the transistors, and an output terminal connected to drain electrodes thereof so that one transistor is rendered non-conductive when the gate voltage is equal to the source voltage thereof, and is rendered conductive when the gate voltage is equal to the source voltage of the other transistor.

2. A device as claimed in claim 1 in which the channel of the first transistor extends substantially parallel to the surface of a substrate in which it is formed and the channel of the second transistor extends substantially perpendicularly to the surface of the substrate.

3. A device as claimed in claim 1 or 2 in which the diffusion depth of the gate of the first transistor is less than the diffusion depth of the source thereof.

4. A device as claimed in any preceding claim in which the diffusion depth of the drain of the second transistor is less than the diffusion depth of the gate thereof.

5. A semiconductor device as claimed in any preceding claim connected to operate as an inverter.

6. A semiconductor device as claimed in claim 1 and substantially as herein described with reference to and as shown in the accompanying drawings.

7. A method of making a semiconductor device as claimed in claim 1 including forming said transistors on a single substrate and diffusing into the substrate the gate of one transistor and the channel of the other transistor simultaneously.

8. A method as claimed in claim 7 in which the drain of said first transistor is diffused into the substrate simultaneously with the gate of the other transistor.



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9. A method as claimed in claim 7 and substantially as herein described with reference to the accompanying drawings.

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