CLAIMS

I claim:

1. A multi-chip module hybrid integrated circuit (MCM-HIC) configured to support cold spare of an apparatus that includes a plurality of circuits that are not cold spare compliant, the MCM-HIC comprising:

an interconnecting substrate that is divided into a plurality of power zones, said plurality of power zones including a first power zone and a second power zone, wherein power can be applied to and withdrawn from the first power zone independently of the second power zone;

at least one core IC installed on the substrate; and

at least one cold spare chiplet installed on the substrate, at least partly on the first power zone, the at least one cold spare chiplet being configured, when not fully powered, to present a defined impedance, voltage, and/or logic level to at least one of its input or output signal lines;

whereby when power is withdrawn from the first power zone, and consequently at least partially withdrawn from the at least one cold spare chiplet, all circuits among the plurality of circuits that are at least partly unpowered are protected by the at least one cold spare chiplet from damage, while also being prevented by the at least one cold spare chiplet from hindering operation of any other circuits among the plurality of circuits that remain in operation.

2. The MCM-HIC of claim 1, wherein the first and second power zones are adjacent, and wherein each of ~~at least~~ one or more cold spare chiplets of the at least one cold spare chiplet~~s~~ is installed such that it extends across a boundary between the first and second power zones and draws power from both the first power zone and the second power zone.

3. The MCM-HIC of claim 1, wherein the at least one core IC includes a first core IC installed on the first power zone and a second core IC installed on the second power zone.

4. The MCM-HIC of claim 3, wherein for each of the first and second power zones, power can be applied thereto at a voltage and/or current that is compatible with the first and second core IC, respectively.

5. The MCM-HIC of claim 3, wherein interconnections between the first and second core IC's are mediated by at least one mediating chiplet that enables interoperability between the first and second core ICs.

6. The MCM-HIC of claim 5, wherein the at least one mediating chiplet provides at least one of impedance, voltage and current intercompatibility of signals transmitted between the first and second core ICs.

7. The MCM-HIC of claim 6, wherein:

the at least one mediating chiplet is one of the at least one cold spare chiplet~~s~~, being thereby a mediating cold spare chiplet; and

when power is withdrawn from the first power zone, and consequently from the first core IC and at least partially from the at least one mediating cold spare chiplet, while the second power zone and second core IC remain powered, the first core IC is protected from being damaged by the second core IC, and operation of the second core IC is not hindered by the unpowered first core IC.

8. The MCM-HIC of claim 7, wherein the mediating cold spare chiplet is installed such that it extends across a boundary between the first and second power zones and draws power from both the first power zone and the second power zone, and wherein when power is withdrawn from the first power zone:

power is also at least partially withdrawn from the mediating cold spare chiplet; and

the mediating cold spare chiplet presents ~~a~~ specified voltages and/or logic levels to the second core IC.

9. The MCM-HIC of claim 1, wherein a group of external signal lines provides interconnection between an interface chiplet installed on the substrate and an external circuit of the plurality of circuits, the group of external signal

lines being configured for transmitting signals between the external circuit and a first core IC of the at least one core IC.

10. The MCM-HIC of claim 9, wherein the interface chiplet provides at least one of impedance, voltage and/or current interoperability to the signals transmitted between the external circuit and the first core IC.

11. The MCM-HIC of claim 9, wherein:

the external circuit is not cold spare compliant;

the interface chiplet is one of the at least one cold spare chiplet~~s~~, being thereby an interface cold spare chiplet, the interface cold spare chiplet being at least partly installed on the first power zone; and

when power is withdrawn from the first power zone:

power is also at least partially withdrawn from the interface cold spare chiplet; and

power can also be withdrawn from the external circuit without damaging the external circuit, and without impeding operation of any core IC of the at least one core IC~~s~~ installed on the MCM-HIC.

12 The MCM-HIC of claim 11, wherein:

the interface cold spare chiplet is installed such that it extends across a boundary between the first power zone and a second power zone and draws power from both the first power zone and the second power zone;

the first core IC is installed on the second power zone; and

when power is withdrawn from the first power zone, power is also partially withdrawn from the interface cold spare chiplet, such that the interface cold spare chiplet presents defined impedances to the external circuit, while presenting at least one specified voltage and/or logic level to the first core IC.

13. The MCM-HIC of claim 1, wherein:

the first power zone comprises a plurality of independently controlled power circuits; and

power can be selectively withdrawn and applied to the first power zone under control of a controller by withdrawing and applying power to the plurality of power circuits according to a determined sequence thereof.

14. The MCM-HIC of claim 1, wherein the MCM-HIC is whole device cold spare compliant.

15. The MCM-HIC of claim 1, wherein at least one of the at least one core IC~~s~~ is a VLSI IC.

16. The MCM-HIC of claim 1, wherein the substrate is divided into at least five power zones.

17. The MCM-HIC of claim 1, wherein the substrate is divided into at least ten power zones.

18. The MCM-HIC of claim 1, wherein the MCM-HIC further comprises, installed on the substrate, at least one ~~of a~~ chiplet that is not a cold spare chiplet and a passive component.

19. A method of providing cold spare support to an apparatus that includes a plurality of circuits that are not cold spare compliant, the method comprising:

selecting at least one core IC from among the plurality of circuits,

selecting an interconnecting substrate having a plurality of power zones including a first power zone and a second power zone;

selecting at least one cold spare chiplet, the at least one cold spare chiplet being configured, when not fully powered, to present a defined impedance, voltage, and/or logic level to at least one of its input or output signal lines;

installing the core IC on the interconnecting substrate;

installing the at least one cold spare chiplet on the interconnecting substrate, at least partly on the first power zone; and

configuring the first power zone so that power can be applied thereto and withdrawn therefrom independently of the second power zone, such that when power is withdrawn from the first power zone, and consequently at least partially

withdrawn from the at least one cold spare chiplet, all circuits among the plurality of circuits that are at least partly unpowered are protected by the at least one cold spare chiplet from damage, while also being prevented by the at least one cold spare chiplet from hindering operation of any other circuits among the plurality of circuits that remain in operation.

20. The method of claim 19, wherein selecting the at least one cold spare chiplet includes selecting at least one chiplet from among a group of pre-manufactured cold spare chiplets.

21. The method of claim 19, wherein selecting the at least one cold spare chiplet includes designing and manufacturing a cold spare chiplet.

22. The method of claim 19, wherein selecting the substrate includes selecting the substrate from among a group of pre-manufactured substrates.

23. The method of claim 19, wherein selecting the substrate includes designing and manufacturing the substrate.