CLAIMS

1. A semiconductor structure comprising:

a substrate;

a semiconductor pillar located on the substrate and a gate pillar located on the semiconductor pillar, wherein the semiconductor pillar and the gate pillar both extend in a direction perpendicular to a plane of the substrate;

a first word line extending in a first direction parallel to the plane of the substrate and surrounding the semiconductor pillar; and

a semiconductor layer located above the semiconductor pillar and at least surrounding a sidewall of the gate pillar.

2. The semiconductor structure of claim 1, wherein the gate pillar and the semiconductor pillar are in one-to-one correspondence; or

wherein a top of the semiconductor pillar is electrically connected to a bottom of the gate pillar; or

wherein an orthographic projection of the semiconductor pillar is at least partially overlapped with an orthographic projection of the gate pillar on the plane of the substrate, and a material of the gate pillar is same as a material of the semiconductor pillar.

3. The semiconductor structure of claim 1, wherein the semiconductor pillar comprises a first electrode, a first channel region, and a second electrode distributed from bottom to top, and the first electrode, the first channel region, and the second electrode are same in term of conductivity type.

4. The semiconductor structure of claim 1, wherein the semiconductor layer comprises a first sub-portion, a second sub-portion, and a third sub-portion connected to each other, and

wherein the first sub-portion covers a top surface of the gate pillar, the second sub-portion covers the sidewall of the gate pillar, and the third sub-portion partially covers an upper surface of the substrate between adjacent gate pillars.

5. The semiconductor structure of claim 4, wherein the semiconductor structure further comprises:

a second word line extending in the first direction, surrounding an end, close to the semiconductor pillar, of the second sub-portion and covering an upper surface of the third sub-portion; and

a first bit line and a second bit line extending in a second direction parallel to the plane of the substrate and perpendicular to the first direction, wherein the first bit line is located below the semiconductor pillar and electrically connected to a lower portion of the semiconductor pillar, while the second bit line is located above the semiconductor layer and electrically connected to the first sub-portion.

68. The semiconductor structure of claim 3, wherein the semiconductor structure further comprises:

a first gate dielectric layer located between the first word line and the semiconductor pillar, and surrounding the first channel region and the second electrode; and

a second gate dielectric layer comprising a first sub-layer and a second sub-layer connected to each other, wherein the first sub-layer is located between the gate pillar and the semiconductor layer, covers a top and the sidewall of the gate pillar, while the second sub-layer covers an upper surface of the substrate between adjacent gate pillars.

7. The semiconductor structure of claim 3, wherein the semiconductor structure further comprises:

a first gate dielectric layer located between the first word line and the semiconductor pillar, and surrounding the first channel region and the second electrode;

a second gate dielectric layer covering a top and the sidewall of the gate pillar; and

a fourth dielectric layer covering an upper surface of the substrate between adjacent gate pillars.

8. The semiconductor structure of claim 1, wherein materials of the semiconductor pillar and the semiconductor layer comprise at least one or a combination of indium oxide, tin oxide, In-Zn oxide, Sn-Zn oxide, Al-Zn oxide, In-Ga oxide, In-Ga-Zn oxide, In-Al-Zn oxide, In-Sn-Zn oxide, Sn-Ga-Zn oxide, Al-Ga-Zn oxide, or Sn-Al-Zn oxide.

9. The semiconductor structure of claim 1, wherein the semiconductor structure further comprises: a word line isolation structure extending in the first direction and located between two adjacent first word lines to isolate the adjacent first word lines; or

wherein the semiconductor structure further comprises: a first dielectric layer located above the substrate and a second dielectric layer located above the first dielectric layer, wherein the semiconductor pillar and the first word line are located in the first dielectric layer, while the gate pillar, the semiconductor layer and the second word line are located in the second dielectric layer.

10. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

forming a pillar on the substrate, wherein the pillar comprises a semiconductor pillar, and extends in a direction perpendicular to a plane of the substrate;

forming a first word line extending in a first direction parallel to the plane of the substrate and surrounding part of the pillar;

forming a gate pillar right above the semiconductor pillar, wherein the gate pillar extends in the direction perpendicular to the plane of the substrate; and

forming a semiconductor layer, wherein the semiconductor layer at least surrounds a sidewall of the gate pillar.

11. The method of claim 10, before forming the pillar on the substrate, further comprising:

forming an insulating layer on the substrate;

performing an etching process on the insulating layer to form a plurality of first trenches extending in a second direction in the insulating layer, wherein the second direction is parallel

to the plane of the substrate and perpendicular to the first direction; and

filling the plurality of first trenches with a conductive material to form a plurality of first bit lines extending in the second direction.

12. The method of claim 11, after filling the plurality of first trenches with the conductive material to form the plurality of first bit lines extending in the second direction, further comprising:

forming a first dielectric layer;

etching the first dielectric layer to form a plurality of second trenches extending in the first direction in the first dielectric layer; and

filling the plurality of second trenches with an insulating material to form a plurality of word line isolation structures extending in the first direction.

13. The method of claim 12, wherein the forming the pillar on the substrate comprises:

etching the first dielectric layer to form a plurality of first channel holes for exposing the first bit lines;

filling each of the first channel holes with a semiconductor material to form the pillar, wherein the pillar comprises the semiconductor pillar; and

wherein the forming the first word line extending in a first direction parallel to the plane of the substrate and surrounding the semiconductor pillar comprises:

forming a plurality of third trenches extending in the first direction, wherein each of the third trenches is located between two adjacent word line isolation structures;

forming a first gate dielectric layer in each of the third trenches, wherein the first gate dielectric layer surrounds part of the semiconductor pillar; and

forming the first word line in each of the third trenches, wherein the first word line surrounds part of the first gate dielectric layer.

14. The method of claim 10, wherein the forming the gate pillar right above the semiconductor

pillar comprises:

forming and etching a second dielectric layer to form a plurality of second channel holes in the second dielectric layer, wherein each of the second channel holes is used for exposing a top of the semiconductor pillar;

forming the gate pillar in each of the second channel holes; and

wherein after forming the gate pillar, the method further comprises:

exposing a top surface and a sidewall of the gate pillar;

depositing a second gate dielectric layer, wherein the second gate dielectric layer comprises a portion surrounding the sidewall and a top of the gate pillar, and a portion covering an upper surface of the first dielectric layer;

forming a semiconductor material layer and a word line material layer on the second gate dielectric layer sequentially, wherein the semiconductor material layer is conformal with the second gate dielectric layer, and the word line material layer fills a gap between adjacent semiconductor material layers; and

etching the semiconductor material layer and the word line material layer to respectively form the semiconductor layer and a plurality of second word lines extending in the first direction.

15. The method of claim 10, after forming the semiconductor layer, further comprising:

forming a third dielectric layer;

etching the third dielectric layer to form a fourth trench extending in a second direction and exposing an upper surface of the semiconductor layer; and

forming a second bit line in the fourth trench.

16. The method of claim 10, wherein the forming the pillar on the substrate comprises:

forming the pillar the substrate, wherein the pillar protrudes from a surface of the substrate, extends in the direction perpendicular to the plane of the substrate, comprises the

semiconductor pillar and a gate pillar located right above the semiconductor pillar, and

wherein after forming the first word line, the method further comprises: forming a semiconductor layer at least surrounding a sidewall of the gate pillar.

17. The method of claim 16, before forming the pillar on the substrate, further comprising:

forming a plurality of first bit lines extending in a second direction on the substrate;

forming a first dielectric layer; and

forming a plurality of word line isolation structures extending in the first direction in the first dielectric layer.

18. The method of claim 17, wherein the forming the pillar on the substrate comprises:

etching the first dielectric layer to form a plurality of first channel holes for exposing the first bit lines;

forming a semiconductor material layer, wherein the semiconductor material layer covers an upper surface of the first dielectric layer and fills the first channel hole; and

etching the semiconductor material layer to form the pillar, wherein a portion of the pillar located in the first channel hole is defined as the semiconductor pillar, and a portion of the pillar located right above the first channel hole is defined as the gate pillar.

19. The method of claim 18, wherein the forming the first word lines extending in the first direction comprises:

forming a plurality of third trenches extending in the first direction, wherein each of the third trenches is located between two adjacent word line isolation structures;

forming a gate dielectric layer, wherein the gate dielectric layer comprises a first gate dielectric layer surrounding part of the semiconductor pillar, and a second gate dielectric layer surrounding the sidewall and a top of the gate pillar; and

forming the first word line in each of the third trenches, wherein the first word line surrounds part of the first gate dielectric layer.

20. The method of claim 19, after forming the first word line, further comprising:

forming a semiconductor material layer and a word line material layer on the second gate dielectric layer sequentially, wherein the semiconductor material layer at least covers the second gate dielectric layer, and the word line material layer fills a gap between adjacent semiconductor material layers; and

etching the semiconductor material layer and the word line material layer to remove part of the semiconductor material layer and the word line material layer located above the word line isolation structure, so as to form the semiconductor layer and a plurality of second word lines extending in the first direction respectively.