

DESCRIPTION

PHASE-LOCKED LOOP APPARATUS

Technical Field

5 The present invention relates to a phase-locked loop apparatus and, more particularly, to a phase-locked loop apparatus improved by digitizing a phase-locked loop which is used to reproduce a clock for reproducing digital data recorded on recording media such as optical disk media, magneto-optical
10 disk media, and magnetic media.

Background Art

Optical disk apparatuses are widely known as one of apparatuses for recording and reproducing digital data. In the
15 optical disk apparatus, a phase-locked loop (PLL) circuit is conventionally used to lock a phase of a clock component included in a reproduction signal and a phase of a reproduction clock, when the digital data is reproduced. Particularly, an erasable optical disk medium has plural unit blocks called
20 "sectors", each of which comprises a set of a header part on which address information and the like is written and a data part on which the digital data is actually recorded. The phase locking is performed sector by sector by the phase-locked loop.

In order to perform this intermittent reproduction
25 normally, the header part and data part have locking patterns

(VFO patterns) 42a-42d, as shown in figure 19, each of which comprises a single pattern (single frequency). The data reproduction is performed using a method of increasing the response characteristic of the phase-locked loop circuit to perform high-speed and stable phase locking in these VFO pattern areas, and decreasing the response characteristic of the phase-locked loop circuit before ends of the VFO pattern areas to reduce influences of noises and the like, thereby to maintain a locked state.

Figure 19 is a diagram showing a data format in a sector of an optical disk reproduction apparatus. In the figure, reference numeral 43 designates a sector mark (hereinafter referred to as SM) indicating a start position of the sector. Numeral 44 designates an address mark (hereinafter referred to as AM) indicating a start position of address information. Numeral 45 designates address information (hereinafter referred to as ID) indicating the address of the sector. Numeral 46 designates a postamble (hereinafter referred to as PA) indicating an end point of each of the header part and the data part. Numeral 47 designates a data mark (hereinafter referred to as DM) indicating a start position of data 48.

Figure 20 is a block diagram illustrating a digital data reproduction circuit of a prior art optical disk reproduction apparatus.

The prior art optical disk reproduction apparatus as shown

in figure 20 is constituted by an optical disk 49, a reproduction means 50, a waveform equalization means 1, a binarization means 51, a phase-locked loop circuit 52, a loop gain switching unit 57, and a demodulation circuit 58. The phase-locked loop
5 circuit 52 is constituted by a phase comparator 53, a loop filter 54, an amplifier 55, and a Voltage Controlled Oscillator (VCO) 56.

Hereinafter, its operation will be described.

On the optical disk 49 medium, digital data comprising 0
10 and 1, the number of continuous 0 or 1 being controlled to from 3 to 14 inclusive, is recorded as in the 8-16 modulation method for example. In a reproduction signal which is obtained by reproducing data with the reproduction means 50, as the recording density of the data in the linear direction is
15 increased, the amplitude of a waveform having high-band frequency components is attenuated by interference. Then, the waveform equalization means 1 corrects the reproduction signal so as to emphasize its high-band frequency components. The binarization means 51 binarizes the reproduction signal having
20 the emphasized high-band frequency components at a prescribed slice level to convert the signal into a binarized digital signal. In the phase-locked loop circuit 52, a phase of a reproduction clock as a free-running frequency of the phase-locked loop circuit 52 and a phase of a clock component
25 of the binarized signal are compared by the phase comparator

53, and the phase of the reproduction clock is changed on the basis of phase error information which is output as a result of the comparison so as to have the minimum phase error, by using the loop filter 54, the amplifier 55 and the VCO 56, whereby
5 the phase of the clock component of the binarized signal and the phase of the reproduction clock are locked. The response characteristic of the phase-locked loop circuit 52 is switched by the loop gain switching unit 57. Then, the binarized signal and the locked reproduction clock are input to the demodulation
10 circuit 58 to demodulate the digital data.

In the VFO pattern areas on the recording medium, a range where the reproduction is normally performed is sometimes limited due to defects of the recording medium, servo processing or signal processing in the reproduction of the recording medium.
15 Accordingly, improvements are made to perform the phase locking surely as in a method of detecting the defects or the method as shown in figure 19 of detecting SM 43, AM 44, and DM 47 to make the best use of all the VFO pattern areas.

The above-mentioned prior art is adapted to a method which
20 binarizes the reproduction signal to demodulate the digital data. However, when a signal-to-noise ratio of the reproduction signal is significantly deteriorated as the density in the linear direction is increased, the quality of reproduced data is deteriorated.

25 Accordingly, as the recording density in the linear

direction becomes higher, a PRML (Partial Response Maximum Likelihood) signal processing method as a signal processing method which is suitable for the high-density recording and reproduction in the linear direction is increasingly adopted.

5 The PRML signal processing method is the one which urges intentional waveform interference for the reproduction signal, equalizes the reproduction signal with a band which is controlled to reduce emphasis on noises to the utmost, and thereafter demodulates data by a maximum likelihood decoder for
10 demodulating the most likelihood series in accordance with a known regulation of interference. However, when this PRML signal processing method is utilized, multi-bit data obtained by sampling a reproduction clock which is locked to a phase of a clock component included in the reproduction signal should
15 be generated.

This prior art phase-locked loop circuit is constituted by analog elements. Accordingly, a system where analog circuits and digital circuits are mixed complicatedly is obtained and this system is not suitable for the integration.
20 In addition, the dispersion of characteristics caused by the analog elements constituting the analog circuits or secular changes occur in the analog circuits. Accordingly, careful consideration should be given also to the quality control, compensation circuits and the like, whereby the cost of the
25 digital data reproduction apparatus which is constituted by

using the phase-locked loop circuit is increased.

Therefore, a system which is suitable for the PRML signal processing should be realized by digitizing also a clock reproduction circuit and equalization means, thereby
5 increasing the quality of reproduced data and reducing the cost by the integration also in the high-density recording and reproduction.

However, when the phase-locked loop circuit for performing the clock reproduction is realized by digital circuits, as a
10 transfer rate is increased, a delay amount of the phase-locked loop is increased and a capture range indicating a range where a frequency and a phase can be locked at the phase locking is reduced. When phase error information is obtained from analog signals, an amount of a continuous time error can be handled.
15 However, when the phase error information is obtained from digital data after the sampling, the phase error information should be assumed from an amplitude value in the vicinity of a zero cross point. Therefore, sufficient continuous areas of phase error signals cannot be secured.

20 When the capture range is reduced, in a case where the frequency of the reproduction clock is significantly different from the frequency of the clock component included in the reproduction signal, the phase locking is not completed only by the VFO pattern areas. Therefore, errors such as burst
25 errors are increased at the reproduction time and thereby the

data quality is deteriorated.

In addition, the VFO pattern areas are small and, in the case of erasable disks, there is an increase in a risk that the first half part of that area is deteriorated as the number of writing times is increased or a DC offset position is substantially shifted. Therefore, when the frequency of the reproduction clock is significantly different from the frequency of the clock component included in the reproduction signal, errors such as burst errors at the reproduction time are increased and the quality of data is deteriorated.

Further, when data recorded on the recording medium does not include the VFO pattern, the reproduction signal is a random signal. Therefore, when the phase locking is performed using only the phase information, the capture range in locking the phase of the clock component of the reproduction signal and the phase of the reproduction clock is reduced. Accordingly, when the both frequencies are significantly different from each other, the phase locking cannot be performed surely.

The present invention is directed to solve the above problems, and an object of the present invention is to provide a phase-locked loop apparatus which detects phase information from a reproduction signal as well as detects frequency information from a temporal change of the phase information, has a wider capture range than that of an analog phase-locked loop circuit, and performs the phase locking at a high speed,

when a phase-locked loop circuit is digitized.

In addition, an object of the present invention is to provide a phase-locked loop apparatus which predicts phase error information to obtain a wider capture range, as well as
5 locks the phase of the reproduction clock and the phase of the clock component included in the reproduction digital signal at a high speed and with good stability, when the phase-locked loop circuit is digitized.

Further, in addition to the above objects, the present
10 invention has another object to provide a phase-locked loop apparatus which can perform the phase locking also for digital data having no pattern signal comprising a single frequency in a data format of digital information which is recorded on a recording medium.

15 Furthermore, in addition to the above objects, another object of the present invention is to provide a low cost phase-locked loop apparatus which can be integrated easily and has higher reliability.

20 Disclosure of the Invention

To solve the above problems, according to Claim 1 of the present invention, a phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining
25 a reproduction digital signal, comprises: phase error

information detection means for detecting phase error information from a signal area other than a single frequency data area comprising a single frequency in the data format; frequency error information detection means for detecting
5 frequency error information from the single frequency data area comprising the single frequency in the data format; and a feedback loop for locking a phase of the reproduction clock and a phase of a clock component included in the reproduction digital signal, on the basis of the phase error information and
10 the frequency error information, whereby a phase-locked loop circuit is digitized.

According to the present invention, clock reproduction which is suitable for a PRML signal processing method can be performed. In addition, when a multi-bit digital signal which
15 is obtained by the sampling by the A/D converter is a VFO pattern signal, a phase error signal and a frequency error signal are input to the feedback loop as input signals. Therefore, in a VFO pattern area, even when a reproduction signal includes DC components, the phase error is detected correctly, whereby the
20 VFO pattern area can be effectively utilized. Further, a frequency error detector detects a correct inclination of a phase error curve. Therefore, a capture range is substantially extended, whereby a phase-locked loop apparatus which can perform the phase locking at a high speed and with good stability
25 even when a frequency of a reproduction clock is significantly

different from a frequency of a clock component included in the reproduction signal can be provided.

According to Claim 2 of the present invention, a phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprises: waveform equalization means for emphasizing a predetermined frequency band of a reproduction signal; A/D conversion means for sampling the reproduction signal, the predetermined frequency band of which is emphasized by the waveform equalization means, using a reproduction clock at a time when a digital signal is reproduced, to obtain a digital signal; high-pass filter (HPF) means for removing DC components from the digital signal obtained by the sampling when the obtained digital signal is a VFO pattern signal; low-band component suppression means for suppressing low-band noises of the digital signal obtained by the sampling when the obtained digital signal is a signal other than the VFO pattern signal; zero cross detection means for detecting a position where an output of the HPF means or low-band component suppression means crosses a zero level, and outputting a zero cross flag; phase error detection means for detecting a phase error from data in the vicinity of a zero cross, using the zero cross flag and the output of the HPF means or low-band component suppression means; "n" pieces of holding means for holding continuous "n" ("n" is

a positive integer) pieces of the phase errors on the basis of the zero cross flag, which holding means are connected in series with each other; frequency error detection means for detecting an inclination of a phase error curve from outputs of the
5 respective "n" pieces of holding means, and converting the inclination into a frequency error; phase controlling loop filter means for receiving a phase error signal which is an output of the phase error detection means and a frequency error signal which is an output of the frequency error detection means,
10 as input signals when the digital signal obtained by the sampling is the VFO pattern signal, and receiving the phase error signal which is the output of the phase error detection means as an input signal when the obtained digital signal is a signal other than the VFO pattern signal; and oscillator means
15 for generating a reproduction clock on the basis of an output of the phase controlling loop filter means, whereby a phase-locked loop circuit is digitized.

According to the present invention, the clock reproduction which is suitable for the PRML signal processing method can be
20 performed. In addition, when a multi-bit digital signal which is obtained by the sampling by the A/D converter is a VFO pattern signal, the phase error signal and the frequency error signal are input to the feedback loop as input signals. Therefore, in a VFO pattern area, even when a reproduction signal includes
25 DC components, the phase error is detected correctly, whereby

the VFO pattern area can be effectively utilized. Further, the frequency error detector detects a correct inclination of a phase error curve. Therefore, the capture range is substantially extended, whereby a phase-locked loop apparatus
5 which can perform the phase locking at a high speed and with good stability even when a frequency of the reproduction clock is significantly different from a frequency of a clock component included in the reproduction signal can be provided.

According to Claim 3 of the present invention, a
10 phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprises: phase error information detection means for detecting phase error information from a random signal
15 area in the digital data; frequency error information detection means for detecting frequency error information from the random signal area in the digital data; and a feedback loop for locking a phase of the reproduction clock and a phase of a clock component included in the reproduction digital signal on the basis of the
20 phase error information and the frequency error information, and a feedback loop phase controlling loop filter receives a phase error signal and a frequency error signal as input signals.

According to the present invention, when re-locking of
25 phases is required in an area of data other than the VFO pattern

because of defects of a recording medium or the like, the capture range is extended as well as the re-locking time is reduced. Therefore, deterioration in the quality of reproduced data due to burst errors or the like can be minimized. Further, a
5 phase-locked loop apparatus which can obtain the same effects as described above also in a recording medium having no VFO pattern area can be provided.

According to Claim 4 of the present invention, a phase-locked loop apparatus which reads digital data recorded
10 on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprises: waveform equalization means for emphasizing a predetermined frequency band of a reproduction signal; A/D conversion means for sampling the reproduction
15 signal, the predetermined frequency band of which is emphasized by the waveform equalization means, using a reproduction clock at a time when a digital signal is reproduced, to obtain a digital signal; low-band component suppression means for suppressing low-band noises of the digital signal obtained by the sampling;
20 zero cross detection means for detecting a position where an output of the low-band component suppression means crosses a zero level, and outputting a zero cross flag; phase error detection means for detecting a phase error from data in the vicinity of a zero cross, using the zero cross flag and the output
25 of the low-band component suppression means; "n" pieces of

holding means for holding continuous "n" ("n" is a positive integer) pieces of the phase errors on the basis of the zero cross flag, which holding means are connected in series with each other; frequency error detection means for detecting an inclination of a phase error curve from outputs of the
5 respective "n" pieces of holding means, and converting the inclination into a frequency error; phase controlling loop filter means for receiving a phase error signal which is an output of the phase error detection means and a frequency error
10 signal which is an output of the frequency error detection means, as input signals; and oscillator means for generating a reproduction clock on the basis of an output of the phase controlling loop filter means, and the phase controlling loop filter receives the phase error signal and the frequency signal
15 as input signals.

According to the present invention, when the re-locking of phases is required in an area of data other than the VFO pattern because of defects of a recording medium or the like, the capture range is extended as well as the re-locking time
20 is reduced. Therefore, deterioration in the quality of reproduced data due to burst errors or the like can be minimized. Further, a phase-locked loop apparatus which can obtain the same effects as described above also in a recording medium having no VFO pattern area can be provided.

25 According to Claim 5 of the present invention, in the

phase-locked loop apparatus of Claim 2 or 4, the phase error detection means comprises: first holding means and second holding means for holding amplitudes of reproduction signals at adjacent zero cross positions for each zero cross, on the basis of the zero cross flag; subtraction means for receiving an output of the first holding means and an output of the second holding means as inputs; polarity decision means for deciding whether a reproduction waveform at a timing when the amplitude is held by the first holding means is a leading edge or a trailing edge, on the basis of previous and subsequent data; and sign manipulation means for manipulating a sign of an output of the subtraction means on the basis of an output of the polarity decision means.

According to the present invention, correlation of phase error information in the temporal direction is enhanced, whereby the phase error detection having resistance to high-band noise components can be performed. Therefore, a phase-locked loop apparatus which can perform the phase locking without being affected by the high-band noises as well as can maintain a locked state stably can be provided.

According to Claim 6 of the present invention, in the phase-locked loop apparatus of Claim 2 or 4, the frequency error detection means comprises: plural subtraction means each obtaining a difference between the phase errors output by predetermined two holding means among the "n" pieces of holding

means; polarity decision means for deciding which is a polarity of an output of each of the plural subtraction means among positive, negative, and zero; selection means for removing information at a discontinuous point of the phase error curve
5 on the basis of plural inclination information output by the plural subtraction means, and selecting information of an inclination where frequency information is obtained stably; balancing means for balancing the inclination information selected by the selection means; and a gain stage for
10 arbitrarily adjusting a gain of an output of the balancing means, and outputting the adjusted gain to the phase controlling loop filter means, and a correct frequency error is assumed using only a phase error in a linear and continuous area of the phase error curve.

15 According to the present invention, the capture range is extended as well as the response speed of frequency control is increased. Therefore, a phase-locked loop apparatus which can perform the phase locking at a high speed can be provided.

According to Claim 7 of the present invention, in the
20 phase-locked loop apparatus of Claim 2 or 4, the frequency error detection means of Claim 6 is included and the phase controlling loop filter means comprises: phase error absolute value conversion means for converting the output of the phase error detection means into an absolute value; phase decision means
25 for deciding a magnitude of the obtained absolute value with

a predetermined threshold; start time setting means for manipulating a control start time so as to start an operation of a loop filter from the vicinity of a zero phase as a stable point of the phase error curve when control is executed using
5 the phase error signal on the basis of an output of the selection means of the frequency error detection means of Claim 6 and an output of the phase decision means; and loop filter means for outputting a control signal for the oscillator means on the basis of an output of the start time setting means.

10 According to the present invention, when the frequency error detection means of Claim 6 is utilized, a time for performing the phase locking is made equal to a case where a zero phase start is performing, i.e., the phase of the reproduction clock is adjusted so that the clock component
15 included in the reproduction signal and the reproduction clock are in phase and then the phase locking is started. Therefore, a phase-locked loop apparatus which can perform the phase locking at the minimum time can be provided.

According to Claim 8 of the present invention, in the
20 phase-locked loop apparatus of Claim 2 or 4, the phase controlling loop filter means comprises: frequency error absolute value conversion means for converting the output of the frequency error detection means into an absolute value; frequency decision means for deciding a magnitude of the
25 obtained absolute value with a predetermined threshold; error

selection means for performing switching on the basis of an output of the frequency decision means, so that control is executed using only the phase error signal when a frequency of the reproduction clock is within a phase locked range, and using
5 only the frequency error signal when the frequency of the reproduction clock is outside the phase locked range; and loop filter means for outputting a control signal for the oscillator means on the basis of an output of the error selection means.

According to the present invention, when the frequency of
10 the reproduction clock is quite different from the frequency of the clock component included in the reproduction signal and is outside the phase locked range, the control is executed using only the frequency error signal. Therefore, with relative to a case where the phase error is simultaneously fed back, the
15 frequency locking is completed at a higher speed. On the other hand, when the frequency of the reproduction clock is within the phase locked range, the control is executed using only the phase error signal. Therefore, the phase locking is completed smoothly. Accordingly, a phase-locked loop apparatus which
20 can execute the optimal control making the best use of respective advantages of the phase error and frequency error can be provided.

According to Claim 9 of the present invention, a phase-locked loop apparatus which reads digital data recorded
25 on a recording medium in a predetermined data format, and

generates a reproduction clock for obtaining a reproduction digital signal, comprises: acquisition phase error information detection means for detecting acquisition phase error information from a single frequency data area comprising a single frequency in the data format; tracking phase error information detection means for detecting tracking phase error information from a random signal data area comprising a random signal in the digital data; and a feedback loop for locking a phase of the reproduction clock and a phase of a clock component included in the reproduction digital signal on the basis of the acquisition phase error information and the tracking phase error information.

In the present invention, in the pattern area comprising the single frequency, a correct phase error can be detected also when the reproduction signal includes DC components.

Therefore, the pattern area can be utilized effectively as well as a continuous area of the phase error curve can be expanded, whereby the capture range is substantially extended.

Accordingly, a phase-locked loop apparatus which can lock the phase of the reproduction clock and the phase of the clock component included in the reproduction digital data at a high speed and with good stability also when the frequency of the reproduction clock is significantly different from the frequency of the clock component included in the reproduction signal can be provided.

According to Claim 10 of the present invention, a phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprises: A/D conversion means for sampling
5 digital data in the data format with a reproduction clock, to obtain a digital data signal; band-pass filter means for removing direct current components from the digital data signal obtained by the sampling, during reproduction of a single
10 frequency data area in the data format; zero cross detection means for detecting positions where an output signal of the band-pass filter and the digital data signal cross a zero level, and outputting respective zero cross flags; cycle counter means for starting counting with the zero cross flag as a start point;
15 acquisition phase error detection means for detecting a phase error from the output signal of the band-pass filter at a timing when a timing signal is obtained by the cycle counter means; tracking phase error detection means for detecting a phase error of the digital data signal on the basis of the zero cross flag;
20 loop filter means for receiving a phase error signal which is an output of the acquisition phase error detection means as an input signal when the digital signal obtained by the sampling is a VFO pattern signal, and receiving a phase error signal which is an output of the tracking phase error detection means as an
25 input signal when the obtained digital signal is a signal other

than the VFO pattern signal; D/A conversion means for converting
an output signal of the loop filter means into an analog signal;
and oscillator means for generating the reproduction clock on
the basis of the analog signal output by the D/A conversion
5 means.

In the present invention, a correct phase error can be
detected in the pattern area comprising the single frequency
also when the reproduction signal includes DC components.
Therefore, the pattern area can be utilized effectively as well
10 as the continuous area of the phase error curve can be expanded,
whereby the capture range is substantially extended.
Therefore, also when the frequency of the reproduction clock
is significantly different from the frequency of the clock
component included in the reproduction signal, the phase of the
15 reproduction clock and the phase of the clock component included
in the reproduction digital data can be locked at a high speed
and with good stability. Further, when the phase-locked loop
is digitized, the integration can be easily performed when it
is realized as an IC, whereby the cost can be reduced as well
20 as the clock reproduction which is suitable for the PRML signal
processing method can be performed. Therefore, a system which
is suitable for the high-density recording/reproduction can be
provided.

According to Claim 11 of the present invention, a
25 phase-locked loop apparatus which reads digital data recorded

on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprises: first phase error information detection means for obtaining first phase error information
5 from prediction of a zero cross position in a random signal area in the digital data; second phase error information detection means for detecting second phase error information from a random signal in the digital data; and a feedback loop for locking a phase of the reproduction clock and a phase of a clock component
10 included in the reproduction digital signal on the basis of the first phase error information and the second phase error information.

In the present invention, the continuous area of the phase error curve can be expanded also for digital data having no
15 single frequency signal in data format, the capture range is substantially extended. Therefore, a phase-locked loop apparatus can be provided which can lock the phase of the reproduction clock and the phase of the clock component included in the reproduction digital data at a high speed and with good
20 stability, as well as can reduce the re-locking time when the re-locking of phases is required because of defects of a recording medium or the like, whereby the deterioration in the quality of reproduced data due to burst errors or the like can be minimized.

25 According to Claim 12 of the present invention, a

phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprises: loop gain control means for

5 outputting a loop gain control signal for increasing a phase-locking capacity for a predetermined period from a phase-locking start; A/D conversion means for sampling the digital data with a reproduction clock, to obtain a digital data signal; zero cross position prediction means for predicting a

10 zero cross position of random data in the digital data signal obtained by the sampling; acquisition phase error detection means for detecting phase error information of the random data, from an output signal of the zero cross position prediction means and the digital data signal; zero cross detection means

15 for detecting a position where the obtained digital data signal crosses a zero level, and outputting a zero cross flag; tracking phase error detection means for detecting a phase error of the digital data signal on the basis of the zero cross flag; loop filter means for receiving a phase error signal which is an

20 output of the acquisition phase error detection means as an input signal, and receiving a phase error signal which is an output of the tracking phase error detection means as an input signal; D/A conversion means for converting an output signal of the loop filter into an analog signal; and oscillator means

25 for generating the reproduction clock on the basis of the analog

signal output by the D/A conversion means.

According to the present invention, when the zero cross position prediction means is utilized, the continuous area of the phase error curve is expanded also for digital data having
5 no single frequency signal in a data format, whereby the capture range is extended. Therefore, the phase of the reproduction clock and the phase of the clock component included in the reproduction digital data can be locked at a high speed and with good stability, as well as the re-locking time can be reduced
10 when the re-locking of phases is required because of defects of a recording medium or the like, whereby the deterioration in the quality of reproduced data due to burst errors or the like can be minimized. Further, when the phase-locked loop is digitized, the integration can be performed easier when it is
15 realized as an IC. Therefore, the cost can be reduced as well as the clock reproduction which is suitable for the PRML signal processing method can be performed, whereby a system which is suitable for high-density recording/reproduction can be provided.

20

Brief Description of the Drawings

Figure 1 is a block diagram illustrating a frequency detection type of phase-locked loop apparatus according to a first embodiment of the present invention.

25 Figure 2 is a block diagram illustrating a HPF 4 of the

first embodiment.

Figure 3 is a block diagram illustrating a frequency error detector 8 of the first embodiment.

Figure 4 is a block diagram illustrating a phase error
5 detector 6 of the first embodiment or a second embodiment.

Figure 5 is a block diagram illustrating a frequency error detector 8 of the first embodiment.

Figure 6 is a block diagram illustrating a phase controlling loop filter 9 of the first or second embodiment.

10 Figure 7 is a diagram showing a temporal change of phase error information, for explaining an operation of a phase decision unit 29 as a constituent of the phase controlling loop filter 9 of the first or second embodiment.

Figure 8 is a block diagram illustrating a phase controlling
15 loop filter 9 of the first or second embodiment.

Figure 9 is a diagram showing temporal changes of the phase error information and absolute values of frequency errors, for explaining an operation of a frequency decision unit 34 as a constituent of the phase controlling loop filter 9 of the first
20 or second embodiment.

Figure 10 is a block diagram illustrating a frequency detection type of phase-locked loop apparatus according to the second embodiment of the present invention.

Figure 11 is a block diagram illustrating a frequency error
25 detection unit 8 of the second embodiment.

Figure 12 is a block diagram illustrating a structure of a digital phase-locked loop circuit as a phase-locked loop apparatus according to a third embodiment of the present invention.

5 Figure 13 is a block diagram illustrating a structure of a BPF shown in figure 12.

Figure 14 is a diagram for explaining a relationship between a counting operation of a cycle counter shown in figure 12 and phase error signals.

10 Figures 15 are diagrams for explaining continuity of phase error signals. Figure 15(a) is a diagram for explaining continuity of phase error signals in the digital phase-locked loop circuit of the third embodiment. Figure 15(b) is a diagram for explaining continuity of phase error signals in a prior art
15 phase-locked loop.

Figure 16 is a diagram for explaining a phase error signal which is output by an acquisition phase error detector shown in figure 12 under conditions of different locking frequencies.

Figure 17 is a block diagram illustrating a structure of
20 a digital phase-locked loop circuit as a phase-locked loop apparatus according to a fourth embodiment of the present invention.

Figure 18 is a block diagram illustrating a structure of a zero cross position prediction unit shown in figure 17.

25 Figure 19 is a diagram showing a data format in a sector

of an optical disk reproduction apparatus (DVD-RAM).

Figure 20 is a block diagram illustrating a prior art optical disk reproduction apparatus.

5 Best Mode for Carrying out the Invention

Hereinafter, embodiments of the present invention will be described. The embodiments shown below are examples of the present invention. Therefore, the present invention is not limited to these embodiments.

10 [Embodiment 1]

Figure 1 is a block diagram illustrating a phase-locked loop apparatus according to a first embodiment of the present invention.

As shown in figure 1, the frequency detection type of
15 phase-locked loop apparatus according to the first embodiment is constituted by a waveform equalization means 1 for emphasizing high-band frequency components of a reproduction signal, an A/D converter 2 for converting an analog signal into a digital signal, a gate generator 3 for generating a gate signal,
20 a high-pass filter (HPF) 4 for removing DC components, a zero cross detector 5 for detecting a position where a signal waveform crosses a zero level, a phase error detector 6 for detecting a phase error, holding means 7a-7d for holding the phase errors, a frequency error detector 8 for detecting a
25 frequency error, a phase controlling loop filter 9 for locking

a phase of a reproduction clock and a phase of the reproduction signal, an oscillator 10 for generating the reproduction clock, and a low-band component suppression circuit 11 for suppressing low-band noises.

5 A phase error information detection means 1000 for detecting phase error information from a signal area other than a single frequency data area comprising a single frequency in the data format is constituted by the waveform equalization means 1, the A/D converter 2, the low-band component suppression
10 circuit 11, the gate generator 3, the high-pass filter (HPF) 4, the zero cross detector 5, and the phase error detector 6. A frequency error information detection means 2000 for detecting frequency error information from the single frequency data area comprising the single frequency in the data format
15 is constituted by the waveform equalization means 1, the A/D converter 2, the low-band component suppression circuit 11, the gate generator 3, the high-pass filter (HPF) 4, the zero cross detector 5, the phase error detector 6, the holding means 7a-7d, and the frequency error detector 8. A feedback loop 3000 for
20 locking the phase of the reproduction clock to the phase of the clock component included in the reproduction digital signal on the basis of the phase error information and the frequency error information is constituted by the phase controlling loop filter 9, the oscillator 10, and the A/D converter 2.

25 Hereinafter, constructions of the respective elements will

be described in more detail.

Initially, the HPF 4, the phase error detector 6, the frequency error detector 8, and the phase controlling loop filter 9 are described with reference to figures.

5 Figure 2 is a block diagram illustrating the HPF according to the first embodiment.

The HPF 4 according to the first embodiment is a digital filter for removing DC components in cycles of the VFO patterns, and constituted by a delay means 12 and a subtraction means 13.

10 For example in the case of DVD-RAM (DVD random access memory), the VFO pattern is the one in which 4T patterns (T is a minimum recording unit) are continuously repeated. In this case, as shown in figure 2, the delay means 12 delays an input signal (4T continual waveform) for a time corresponding to 4T
15 and the subtraction means 13 subtracts an output of the delay means 12 from present data, thereby constructing the HPF for removing the DC components.

Figure 3 is a block diagram illustrating the frequency error detector according to the first embodiment.

20 As shown in figure 3, the frequency error detector 8 of the first embodiment is constituted by a subtraction means 14a for subtracting an output of the holding means 7b from an output of the holding means 7a, a subtraction means 14b for subtracting an output of the holding means 7c from an output of the holding
25 means 7b, a subtraction means 14c for subtracting an output of

the holding means 7d from an output of the holding means 7c, polarity decision means 15a-15c for deciding which are polarities of outputs of the subtraction means 14a-14c among positive, negative and zero, an output decision means 16 for
5 deciding whether a frequency error signal is to be output or not on the basis of outputs of the polarity decision means 15a-15c, and a gain stage 17 for adjusting a gain of the output of the subtraction means 14a only when the output decision means 16 decides that the frequency error signal is to be output,
10 thereby outputting a frequency error signal.

Figure 4 is a block diagram illustrating the phase error detector according to the first embodiment.

As shown in figure 4, the phase error detector 6 of the first embodiment is constituted by holding means 18 and 19 for
15 holding amplitudes of reproduction signals at adjacent zero cross positions for each zero cross on the basis of a zero cross flag, a subtraction means 20 for receiving outputs of the holding means 18 and 19 as input, a polarity decision means 21 for deciding whether a reproduction waveform at a timing when
20 the amplitude is held by the holding means 18 is a leading edge or trailing edge, on the basis of previous and subsequent data, and a sign manipulation means 22 for manipulating a sign of an output of the subtraction means 20 on the basis of an output of the polarity decision means 21.

25 Figure 8 is a block diagram illustrating the phase

controlling loop filter according to the first embodiment.

As shown in figure 8, the phase controlling loop filter 9 of the first embodiment is constituted by a frequency error absolute value conversion means 33 for converting an output of the frequency error detector 8 into an absolute value, a frequency decision unit 34 for deciding a magnitude of the obtained absolute value using a prescribed threshold 36, an error selection means 35 for outputting a selection signal to a loop filter 31 on the basis of an output of the frequency decision unit 34, so that the loop filter 31 performs control using only the frequency error signal when a frequency of a reproduction clock is outside a phase locked range, and using only the phase error signal when the frequency of the reproduction clock is within the phase locked range, and the loop filter 31 for outputting an oscillator control signal in accordance with an output of the error selection means 35.

As shown in figure 9, in an area where the absolute value of the frequency error is larger than the threshold 36, the frequency decision unit 34 outputs a signal so that the error selection means 35 selects the frequency error signal. In an area where the absolute value of the frequency error is smaller than the threshold 36, the frequency decision unit 34 outputs a signal so that the error selection means 35 selects the phase error signal.

Next, the waveform equalization means 1, the A/D converter

2, the gate generator 3, the zero cross detector 5, the holding means 7a-7d, the oscillator 10, and the low-band component suppression circuit 11 will be described.

The waveform equalization means 1 is constituted by a filter
5 such as a high-order ripple filter, which can arbitrarily set a boost amount and a cut-off frequency of the input signal.

The A/D converter 2 converts an analog signal into a multi-bit digital signal by the sampling, using a reproduction clock generated by the oscillator 10.

10 The gate generator 3 starts counting from the head of a sector with a counter with the reproduction clock as a reference signal, and outputs a gate signal for distinguishing between the VFO pattern area and an area of data other than the VFO pattern according to a count number at a predetermined place.

15 The zero-cross detector 5 detects a zero cross position as a position where a signal waveform crosses the zero level.

The holding means 7a-7d are connected in series with each other and hold continuous four phase errors.

The oscillator 10 is constituted by a VCO for controlling
20 an oscillated frequency according to a controlled voltage. Or, it is constituted by a digital element.

The low-band component suppression circuit 11 inputs amplitude information in the vicinity of the zero cross of the reproduction signal into a low-pass filter, and subtracts
25 obtained low-band components from the input signal considering

correlation of data, thereby suppressing low-band noises.

Hereinafter, the operation will be described.

A reproduction signal from an optical disk or the like is corrected by the waveform equalization means 1 so as to emphasize high-band frequency components. Thereafter, it is sampled by the A/D converter 2 to obtain a multi-bit digital signal. Then, a gate signal indicating whether the multi-bit digital signal obtained by the sampling by the A/D converter 2 is a VFO pattern signal or not is generated by the gate generator 3.

When the gate signal generated by the gate generator 3 indicates that the multi-bit digital obtained by the sampling by the A/D converter 2 is the VFO pattern signal, this multi-bit digital signal obtained by the A/D converter 2 is input to the HPF 4 and its DC components are removed. Thereafter, this signal is output to the zero cross detector 5 and the phase error detector 6.

When the digital signal whose DC components are removed by the HPF 4 is input to the zero cross detector 5, the detector 5 detects a zero cross flag as a signal indicating the zero cross position, and outputs the zero cross flag to the phase error detector 6 and the holding means 7a-7d.

When the zero cross flag output by the zero cross detector 5 and the digital signal output by the HPF 4 are input to the phase error detector 6, the detector 6 detects a phase error

from data in the vicinity of the zero cross, and outputs the phase error to the holding means 7a-7d and the phase controlling loop filter 9.

The phase error output by the phase error detector 6 is held by the holding means 7a on the basis of the zero cross flag output by the zero cross detector 5. At the same time, a phase error which is held by the holding means 7a immediately before is held by the holding means 7b, a phase error which is held by the holding means 7b immediately before is held by the holding means 7c, and a phase error which is held by the holding means 7c immediately before is held by the holding means 7d.

The frequency error detector 8 detects an inclination of a phase error curve from the phase errors held by the respective holding means 7a-7d, converts the inclination into a frequency error, and output the frequency error to the phase controlling loop filter 9.

The phase controlling loop filter 9 locks the phase of the reproduction clock and the phase of the clock component included in the reproduction digital signal, using the phase error signal output by the phase error detector 6 and the frequency error signal output by the frequency error detector 8, and outputs the signal to the oscillator 10.

The oscillator 10 generates a reproduction clock on the basis of the output of the phase controlling loop filter 9, and outputs the reproduction clock to the A/D converter 2.

When the gate signal output by the gate generator 3 indicates that the multi-bit digital signal obtained by the sampling by the A/D converter 2 is data other than a VFO pattern signal, this multi-bit digital signal obtained by the A/D
5 converter 2 is input to the low-band component suppression circuit 11 and its low-band noises are suppressed. Thereafter, this signal is output to the zero cross detector 5 and the phase error detector 6.

When the digital whose low-band noises are suppressed by
10 the low-band component suppression circuit 11 is input to the zero cross detector 5, the detector 5 detects a zero cross flag as a signal indicating a zero cross position, and outputs the zero cross flag to the phase error detector 6 and the holding means 7a-7d.

15 When the zero cross flag output by the zero cross detector 5 and the digital signal output by the low-band component suppression circuit 11 are input to the phase error detector 6, the detector 6 detects a phase error from data in the vicinity of the zero cross, and outputs the phase error to the holding
20 means 7a-7d and the phase controlling loop filter 9.

The phase controlling loop filter 9 locks the phase of the reproduction clock and the phase of the clock component included in the reproduction digital signal using the phase error signal output by the phase error detector 6, and outputs the signal
25 to the oscillator 10.

The oscillator 10 generates a reproduction clock on the basis of the output of the phase controlling loop filter 9, and outputs the reproduction clock to the A/D converter 2.

As described above, according to the first embodiment, even
5 when the reproduction signal includes the DC components in the VFO pattern area, a correct phase error is detected, whereby the VFO pattern area can be effectively utilized. In addition, according to this first embodiment, a correct inclination of the phase error curve is detected, whereby a capture range can
10 be substantially extended. Therefore, even when the frequency of the reproduction clock is significantly different from the frequency of the clock component included in the reproduction signal, the phase of the reproduction clock and the phase of the clock component included in the reproduction digital data
15 can be locked at a high speed and with good stability.

In addition, the subtraction means of the phase error detector has an effect which is equal to that of a primary low-pass filter, whereby the correlation between phase error signals in the temporal direction is enhanced. Therefore, the
20 phase error detection has a resistant to high-band noise components. Accordingly, the phase locking can be performed without being affected by the high-band noises as well as the locked state can be maintained stably.

When the frequency of the reproduction clock is
25 significantly different from the frequency of the clock

component included in the reproduction signal and is outside the phase locked range, the phase controlling loop filter performs control using only the frequency error signal. Therefore, with relative to a case where the phase error is simultaneously fed back, the frequency locking is completed at a higher speed. On the other hand, when the frequency of the reproduction clock is within the phase locked range, the phase controlling loop filter performs control using only the phase error signal. Therefore, the phase locking is smoothly completed. Accordingly, optimal control can be performed making good use of respective advantages of the phase error and the frequency error.

In this first embodiment, four holding means 7a-7d are provided. However, "n" pieces ("n" is a positive integer) of holding means connected in series can be provided. The larger the "n" is, the more correctly the phase curve can be reproduced.

In addition, in this first embodiment, the frequency error detector 8 as shown in figure 3 is provided. However, a frequency error detector having a structure as shown in figure 5 can be utilized.

The frequency error detector as shown in figure 5 is constituted by a subtraction means 23a for subtracting an output of the holding means 7c from an output of the holding means 7a, a subtraction means 23b for subtracting an output of the holding means 7d from an output of the holding means 7b, a subtraction

means 23c for subtracting an output of the holding means 7d from
an output of the holding means 7a, polarity decision means
24a-24c for deciding which are polarities of outputs of the
subtraction means 23a-23c among positive, negative and zero,
5 a selection means 25 for removing information at a discontinuous
point of the phase curve on the basis of outputs of the polarity
decision means 24a-24c and selecting information of an
inclination where frequency information can be stably obtained,
a balancing means 26 for balancing an output of the subtraction
10 means 23c only when the selection means 25 decides that a
corresponding phase error is data of a linear and continuous
area of the phase curve, and a gain stage 27 for arbitrarily
adjusting a gain of an output of the balancing means 26 and
outputting a frequency error signal.

15 Accordingly, the correct frequency error is assumed using
only the phase error in the linear and continuous area of the
phase curve. Therefore, the capture range is extended as well
as the response speed of the frequency control is increased,
whereby the phase locking can be performed at a high speed.

20 In addition, in this first embodiment, the phase
controlling loop filter 9 as shown in figure 8 is provided.
However, when the frequency error detector has the selection
means for selecting the inclination information as the
frequency error detector as shown in figure 5, a phase
25 controlling loop filter having a structure as shown in figure

6 can be provided.

The phase controlling loop filter as shown in figure 6 is constituted by a phase error absolute value conversion means 28 for converting an output of the phase error detector 6 into an absolute value, a phase decision unit 29 for deciding a magnitude of the absolute value obtained by the phase error absolute value conversion means 28, by using prescribed thresholds, a start time setting means 30 for manipulating a control start time so as to start an operation of a loop filter 31 from the vicinity of a zero phase as a stable point of the phase curve when the loop filter 31 performs control using the phase error signal on the basis of an output of the selection means 25 in the frequency error detector 8 and an output of the phase decision unit 29, and the loop filter 31 for outputting an oscillator control signal on the basis of an output of the start time setting means 30.

As shown in figure 7, the phase decision unit 29 starts the phase control in an area between the thresholds 32a and 32b and immediately after a phase error having continuity is detected.

According to this construction, the time for performing the phase locking can be made equal to a case where the zero phase start is performed, i.e., the phase of the reproduction clock is adjusted so that the clock component included in the reproduction signal and the reproduction clock are in phase,

and the phase locking is started.

[Embodiment 2]

Figure 10 is a block diagram illustrating a frequency detection type of phase-locked loop apparatus according to a second embodiment of the present invention.

In this frequency detection type phase-locked loop apparatus of the second embodiment, the frequency error detector of the frequency detection type phase-locked loop apparatus of the first embodiment is replaced with a frequency error detector as shown in figure 11 and the HPF is omitted.

To be specific, a phase error information detection means 1001 for detecting phase error information from a random signal area in digital data is constituted by a waveform equalization means 1, an A/D converter 2, a gate generator 3, a low-band component suppression circuit 11, a zero cross detector 5, and a phase error detector 6. A frequency error information detection means 2001 for detecting frequency error information from a single frequency data area comprising a single frequency in the data format is constituted by the waveform equalization means 1, the A/D converter 2, the gate generator 3, the low-band component suppression circuit 11, the zero cross detector 5, the phase error detector 6, holding means 7a-7f, and a frequency error detector 8. A feedback loop 3001 for locking a phase of the reproduction clock and a phase of a clock component included in a reproduction digital signal on the basis of the phase error

information and the frequency error information is constituted by a phase controlling loop filter 9, an oscillator 10, and the A/D converter 2.

Figure 11 is a block diagram illustrating the frequency error detector according to the second embodiment.

As shown in figure 11, the frequency error detector of the second embodiment is constituted by a subtraction means 37a for subtracting an output of the holding means 7c from an output of the holding means 7a, a subtraction means 37b for subtracting an output of the holding means 7d from an output of the holding means 7b, a subtraction means 37c for subtracting an output of the holding means 7e from an output of the holding means 7c, a subtraction means 37d for subtracting an output of the holding means 7f from an output of the holding means 7d, polarity decision means 38a-38d for deciding which are polarities of outputs of the subtraction means 37a-37d among positive, negative and zero, a selection means 39 for removing information at a discontinuous point of a phase curve on the basis of outputs of the polarity decision means 38a-38d, and selecting information of an inclination where frequency information is stably obtained, a balancing means 40 for balancing only data which is decided by the selection means 39 that the phase error is data in a linear and continuous area of the phase curve, among the outputs of the subtraction means 37a-37d, and a gain stage 41 for arbitrarily adjusting a gain of an output of the balancing

means 40, thereby outputting an output of the gain stage 41 as a frequency error signal.

Hereinafter, the operation will be described.

A reproduction signal from an optical disk or the like is
5 corrected by the waveform equalization means 1 so as to emphasize high-band frequency components. Thereafter, this reproduction signal is sampled by the A/D converter 2 to obtain a multi-bit digital signal.

The multi-bit digital signal obtained by the sampling by
10 the A/D converter 2 is input to the low-band component suppression circuit 11 and its low-band noises are suppressed. Thereafter, this signal is output to the zero cross detector 5 and the phase error detector 6.

When the digital signal whose low-band noises are
15 suppressed by the low-band component suppression circuit 11 is input to the zero cross detector 5, the detector 5 detects a zero cross flag as a signal indicating a zero cross position, and outputs the zero cross flag to the phase error detector 6 and the holding means 7a-7f.

20 When the zero cross flag output by the zero cross detector 5 and the digital signal output by the low-band component suppression circuit 11 are input to the phase error detector 6, the detector 6 detects a phase error from data in the vicinity of the zero cross, and outputs the phase error to holding means
25 7a-7f and the phase controlling loop filter 9.

The phase error output by the phase error detector 6 is held by the holding means 7a on the basis of the zero cross flag output by the zero cross detector 5. At the same time, a phase error which is held by the holding means 7a immediately before is held by the holding means 7b, a phase error which is held by the holding means 7b immediately before is held by the holding means 7c, a phase error which is held by the holding means 7c immediately before is held by the holding means 7d, a phase error which is held by the holding means 7d immediately before is held by the holding means 7e, and a phase error which is held by the holding means 7e immediately before is held by the holding means 7f.

These holding means 7a-7f are connected in series with each other and hold continuous six phase errors.

The frequency error detector 8 detects an inclination of the phase error curve from the phase errors held by the respective holding means 7a-7f, converts the inclination into a frequency error, and outputs the frequency error to the phase controlling loop filter 9.

The phase controlling loop filter 9 locks the phase of the reproduction clock and the phase of the clock component included in the reproduction digital signal, using the phase error signal output by the phase error detector 6 and the frequency error signal output by the frequency error detector 8, and outputs the signal to the oscillator 10.

The oscillator 10 generates a reproduction clock on the basis of an output of the phase controlling loop filter 9, and outputs the reproduction clock to the A/D converter 2.

As described above, according to the second embodiment,
5 even when a pattern recorded on the recording medium is random data which includes no VFO pattern and the frequency of the reproduction clock is significantly different from the frequency of the clock component included in the reproduction digital signal, a balanced frequency error is assumed using only
10 the phase error in the linear and continuous area of the phase curve. Therefore, the capture range is extended, and the phase of the reproduction clock and the phase of the clock component included in the reproduction digital data are locked at a high speed and with good stability. In addition, also when re-
15 locking of phase is required because of defects of the recording medium or the like, the re-locking time is reduced. Therefore, the deterioration in the quality of reproduced data due to burst errors or the like can be minimized.

In this second embodiment, six holding means 7a-7f are
20 provided. However, "n" pieces ("n" is a positive integer) of holding means connected in series can be provided. The larger the "n" is, the more correctly the phase curve is reproduced.
[Embodiment 3]

Figure 12 is a block diagram illustrating a digital
25 phase-locked loop circuit according to a third embodiment, as

a phase-locked loop apparatus applied to an optical disk apparatus.

In figure 12, an acquisition phase error information detection means 1002 for detecting acquisition phase error information from a single frequency data area comprising a single frequency in a data format, is constituted by a waveform equalization means 101, an A/D converter 102, a low-band component suppression circuit 103, a gate generator 113, a BPF 104, a zero cross detector 105, a cycle counter 106, and an acquisition phase error detector 107. A tracking phase error information detection means 2002 for detecting tracking phase error information from a random signal data area comprising random signals in the digital data, is constituted by the waveform equalization means 1, the A/D converter 2, the low-band component suppression circuit 103, the gate generator 113, the zero cross detector 105, and a tracking phase error detector 108. A feedback loop 3002 for locking a phase of a reproduction clock and a phase of a clock component included in a reproduction digital signal on the basis of the acquisition phase error information and the tracking phase error information, is constituted by a switching unit 109, the gate generator 113, a loop filter 110, an D/A converter 111, an oscillator 112, and the A/D converter 102.

The waveform equalization means 101 is constituted by a high-order ripple filter or the like, which can arbitrarily set

a boost amount and a cut-off frequency of an input signal, and it subjects an input optical disk reproduction signal to correction so as to emphasize its high-band. An output signal of the waveform equalization means 101 is supplied to the A/D converter 102. The A/D converter 2 samples the output signal of the waveform equalization means 101 (analog signal) using a reproduction clock generated by the oscillator 112, to obtain a multi-bit digital signal.

The multi-bit digital signal obtained by the sampling by the A/D converter 102 is input to the low-band component suppression circuit 103 for suppressing low-band noise components. As the low-band component suppression circuit 103, a unit having a structure of inputting amplitude information in the vicinity of a zero cross of the reproduction signal to a low-pass filter, and subtracting obtained low-band components from the input signal considering correlation of data, to suppress low-band noises can be used.

The digital phase-locked loop circuit as shown in figure 12 includes the gate generator 113 for generating a gate signal indicating whether a signal which is reproduced at present is a VFO pattern signal or not. As the gate generator 113, a unit for starting counting from the head of a sector by a counter with the reproduction clock as a reference signal, and outputting the gate signal which distinguishes between a VFO pattern area and a data area at a predetermined place in

according with a count number can be utilized. The VFO pattern is the one where 4T patterns (T is a minimum recording unit) are continuously repeated, like a DVD-RAM (DVD random access memory).

5 When an output signal of the gate generator 113 indicates that a VFO pattern is reproduced at present, an output signal of the low-band component suppression circuit 103 is input to the BPF (band-pass filter) 104 for removing DC (direct current) components. The BPF 104 is a digital filter which nulls the
10 DC components in cycles of the VFO pattern. As the digital filter, a filter which is constituted by a delay means 114 for delaying an input signal for a time corresponding to 4T when the VFO pattern is a 4T continual waveform, and a subtraction means 115 for subtracting an output of the delay means 114 from
15 present data, as shown in figure 13, can be utilized.

 An output signal of the BPF 104 is input to the zero cross detector 105. The zero cross detector 105 is a circuit for detecting a position where an input signal crosses the zero level. Therefore, when the output signal of the BPF 104 is input
20 to the zero cross detector 105, the zero cross detector 105 outputs a zero cross flag indicating a zero cross position of the output signal of the BPF 104.

 The zero cross flag obtained by the zero cross detector 105 is supplied to the cycle counter 106. The cycle counter
25 106 performs counting continuously in an arbitrary cycle "n"

which is proportional to the cycle of the VFO pattern signal with the zero cross flag as a starting point, and generates a timing when a phase error signal is to be extracted. When the VFO pattern is a 4T continual waveform as shown in figure 14, the zero cross detector 105 can simultaneously output characteristics when the phase error signal is generated from a signal amplitude, considering that directions of the input signal crossing the zero level of the reproduction signal are alternately switched between the leading and the trailing every 4T.

The timing signal obtained by the cycle counter 106 and the output signal of the BPF 104 are input to the acquisition phase error detector 107, and a phase error signal is detected from data which is essentially to be at the zero cross position by the acquisition phase error detector 107. Here, the acquisition phase error detector 107 has a function of generating continuous phase error signals of $\pm 720^\circ$ in the VFO pattern comprising 4T continual signals, as shown in figure 15(a). On the other hand, in the prior art phase error detector, only the continuity of approximately $\pm 180^\circ$ is ensured as shown in figure 15(b).

Figure 16 shows a phase error signal which is output by the acquisition phase error detector 7 when the frequency of the reproduction clock is different from the frequency of the clock component included in the reproduction digital data. As

shown in figure 16, sampled data which is essentially at the zero cross position at the phase locking can be securely tracked also when the frequencies are different from each other, and therefore the continuous area of the phase error signal is
5 expanded.

On the other hand, when the output signal of the gate generator 113 indicates that data other than the VFO pattern is reproduced at present, an output signal of the low-band component suppression circuit 103 is input to the zero cross
10 detector 105. Then, the zero cross detector 105 outputs a zero cross flag indicating a zero cross position. In this case, the obtained zero cross flag and the output signal of the low-band component suppression circuit 103 are input to the tracking phase error detector 108, whereby the phase error signal is
15 always detected from data in the vicinity of the zero cross.

The phase error signal output by the acquisition phase error detector 107 and the phase error signal output by the tracking phase error detector 108 are input to the switching unit 109, switched according to the output signal of the gate generator
20 113, and supplied to the loop filter 110. The loop filter 110 receives either of these phase error signals as an input signal, and operates so that the phase of the reproduction clock and the phase of the clock component included in the reproduction digital signal are locked.

25 An output signal of the loop filter 110 is converted into

an analog signal by the D/A converter 111, and this analog signal is supplied to the oscillator 112. The oscillator 112 generates a reproduction clock with the analog signal as a reference. In this case, the oscillator 112 can be constituted by a VCO
5 (Voltage Controlled Oscillator) for controlling an oscillated frequency by the voltage. When the VCO is constituted by a digital element, the D/A converter is not required.

In the digital phase-locked loop circuit having the above construction, a correct phase error is detected even when the
10 reproduction signal includes the DC components in the VFO pattern area, whereby the VFO pattern area can be effectively utilized. In addition, the continuous area of the phase error curve is expanded, whereby the capture range can be significantly extended. Accordingly, even when the frequency
15 of the reproduction clock is substantially different from the frequency of the clock component included in the reproduction signal, the phase of the reproduction clock and the phase of the clock component included in the reproduction digital data can be locked at a high speed and with good stability. Therefore,
20 the clock reproduction which is required for the reproduction of digital data recorded on a recording medium can be performed.
[Embodiment 4]

In the case of data where no VFO pattern is included in patterns recorded on an optical disk medium such as DVD-ROM and
25 CD-ROM, the reproduction signal is a random signal. In such

data, when only the phase error detection is performed, a capture range is narrow when a phase of a clock component included in the reproduction signal and a phase of a reproduction clock are locked. Therefore, when the both
5 frequencies are quite different from each other, the phase locking cannot be performed surely or the phase locking utilizing the VFO pattern cannot be performed when the phase locking is restored immediately after a burst error. A fourth embodiment of the present invention is directed to solve these
10 problems. A structure of a phase-locked loop apparatus according to the fourth embodiment is shown in figure 17.

In figure 17, a waveform equalization means 101, an A/D converter 102, and a low-band component suppression circuit 103 are the same as those in the third embodiment as shown in figure
15 12. To be specific, the waveform equalization means 101 for receiving an optical disk reproduction signal is constituted by a high-order ripple filter or the like, which can arbitrarily set a boost amount and a cut-off frequency of the input signal and it subjects the input optical disk reproduction signal to
20 the correction so as to emphasize its high-band.

A first phase error information detection means 1003 for obtaining first phase error information by prediction of a zeros cross position in a random signal area of digital data is constituted by the waveform equalization means 101, the A/D
25 converter 102, the low-band component suppression circuit 103,

a loop gain controller 116, a zero cross position prediction unit 117, and an acquisition phase error detector 107. A second phase error information detection means 2003 for detecting second phase error information from a random signal in the digital data is constituted by the waveform equalization means 101, the A/D converter 102, the low-band component suppression circuit 103, the loop gain controller 116, a zero cross detector 105, and a tracking phase error detector 108. A feedback loop 3003 for locking a phase of the reproduction clock and a phase of a clock component included in the reproduction digital signal on the basis of the first phase error information and the second phase error information is constituted by a switching unit 109, a loop filter 110, a D/A converter 111, an oscillator 112, and the A/D converter 102.

15 An output signal of the waveform equalization means 101 is supplied to the A/D converter 102. The A/D converter 102 samples the output signal of the waveform equalization means 101 (analog signal) using a reproduction clock generated by the oscillator 112, to obtain a multi-bit digital signal.

20 The multi-bit digital signal obtained by the sampling by the A/D converter 102 is input to the low-band component suppression circuit 103 for suppressing low-band noises. As the low-band component suppression circuit 103, a unit having a structure of inputting amplitude information in the vicinity
25 of the zero cross of the reproduction signal to a low-pass filter,

and subtracting obtained low-band components from the input signal considering correlation of data, thereby to suppress the low-band noises can be utilized as the third embodiment.

In the fourth embodiment, the loop gain controller 116 is
5 provided to obtain a strong phase-locking capacity in an arbitrary section from phase-locking start. The loop gain controller 116 supplies a control gate signal of the loop gain. As the loop gain controller 116, a unit for starting counting from the head of a sector by a counter with the reproduction
10 clock as a reference signal, and outputting the gain control signal for selecting an acquisition area where emphasis is laid on high-speed locking or a tracking area where emphasis is laid on stability, according to the count number at a predetermined place can be utilized. In addition, as the loop gain controller
15 116, a unit which has a function of self-detecting that the frequency of the reproduction clock and the frequency of the clock component included in the reproduction digital data become closer to each other, and performing gain switching can also be utilized.

20 In this fourth embodiment, the zero cross position prediction unit 117 is provided for, when an output signal of the loop gain controller 116 indicates that the acquisition area is reproduced at present, deciding polarity of the output signal of the low-band component suppression circuit 103, predicting
25 data which is at an original zero cross position on the basis

of multi-valued level information which is obtained by adding results of the polarities at different times, and outputting a timing signal for deciding a position where the phase error signal is output. Then, the timing signal obtained by the zero cross position prediction unit 117 and the output signal of the low-band component suppression circuit 103 are input to the acquisition phase error detector 107, and the phase error signal is detected from the data which is essentially to be at the zero cross position.

- 10 In this case, as a method for processing a PRML signal, the zero cross position prediction unit 117 utilizes a PR (a,b, b,a) ML method having a transmission characteristic where four continuous times are given by an expression of $a+b*D+b*D'+a*D''$ (D'' is a signal which is delayed for nT from a reference time).
- 15 The zero cross position prediction unit 117 can have a structure as shown in figure 18, when there is no signal of less than $3T$ as a data format, like DVDs or CDs.

The zero cross position prediction unit 117 as shown in figure 18 is constituted by a delay means 118 for delaying an input signal for $1T$, an addition means 119 for adding the input signal and an output signal of the delay means 118, a conversion means 120 for outputting 1 when polarity of an output signal of the addition means 119 is positive and outputting 0 when the polarity is negative, delay means 121a, 121b, and 121c for each

20

25 delaying an output signal of the conversion means 120 for $1T$,

and an addition means 122 for adding output signals of continuous times of $4T$ from the conversion means 120 and the delay means 121a, 121b, and 121c. On the basis of level information of 5 levels (i.e., 0 to 4) obtained from the addition means 122, which information has correlation with the input signal, the zero cross position prediction unit 117 specifies that a position of 2 is the zero cross position, for example and outputs a timing signal.

When the output signal of the loop gain controller 116 indicates that the tracking area is reproduced at present, the output signal of the low-band component suppression circuit 103 is input to the zero cross detector 105, thereby to obtain a zero cross flag as a signal indicating the zero cross position. Then, the obtained zero cross flag and the output signal of the low-band component suppression circuit 103 are input to the tracking phase error detector 108, whereby the phase error signal is always detected from data in the vicinity of the zero cross.

The phase error signal output by the acquisition phase error detector 107 and the phase error signal output by the tracking phase error detector 108 are input to the switching unit 109, switched according to the output signal of the loop gain controller 116, and supplied to the loop filter 110. The loop filter 110 receives the phase error signal as an input signal, and operates so that the phase of the reproduction clock and

the phase of the clock component included in the reproduction digital signal are locked.

An output signal of the loop filter 110 is converted into an analog signal by the D/A converter 111 and this analog signal
5 is supplied to the oscillator 112. The oscillator 112 generates a reproduction clock on the basis of the analog signal. Here, the oscillator 112 can be constituted by a VCO (Voltage Controlled Oscillator) controlling an oscillated frequency by the voltage, or can be constituted by a digital element. When
10 the VCO is constituted by the digital element, the D/A converter is not required.

According to the fourth embodiment, a continuous area of the phase error curve is expanded also for digital data which includes no pattern signal comprising a single frequency in a
15 data format, whereby the capture range is substantially extended. Therefore, even when the frequency of the reproduction clock is substantially different from the frequency of the clock component included in the reproduction signal, the phase of the reproduction clock and the phase of
20 the clock component included in the reproduction digital data is locked at a high speed and with good stability, whereby the clock reproduction required for the reproduction of digital data recorded on a recording medium can be realized. In addition, when re-locking of phase is required because of
25 defects or the like, the re-locking time can be reduced.

Therefore, the deterioration in the quality of reproduced data due to burst errors or the like can be minimized.

Industrial Availability

- 5 As described above, a phase-locked loop apparatus according to the present invention is suitable for extension of a capture range when a phase-locked loop which is used to reproduce a clock for reproducing digital data recorded on recording media such as optical disk media, magneto-optical
- 10 disk media, and magnetic media, is made as a digital circuit.

CLAIMS

1. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

phase error information detection means for detecting phase error information from a signal area other than a single frequency data area comprising a single frequency in the data format;

frequency error information detection means for detecting frequency error information from the single frequency data area comprising the single frequency in the data format; and

a feedback loop for locking a phase of the reproduction clock and a phase of a clock component included in the reproduction digital signal, on the basis of the phase error information and the frequency error information.

2. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

waveform equalization means for emphasizing a predetermined frequency band of a reproduction signal;

A/D conversion means for sampling the reproduction signal,



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the predetermined frequency band of which is emphasized by the waveform equalization means, using a reproduction clock at a time when a digital signal is reproduced, to obtain a digital signal;

5 high-pass filter (HPF) means for removing DC components from the digital signal obtained by the sampling when the obtained digital signal is a VFO pattern signal;

low-band component suppression means for suppressing low-band noises of the digital signal obtained by the sampling
10 when the obtained digital signal is a signal other than the VFO pattern signal;

zero cross detection means for detecting a position where an output of the HPF means or low-band component suppression means crosses a zero level, and outputting a zero cross flag;

15 phase error detection means for detecting a phase error from data in the vicinity of a zero cross, using the zero cross flag and the output of the HPF means or low-band component suppression means;

"n" pieces of holding means for holding continuous "n" ("n" is a positive integer) pieces of the phase errors on the basis
20 of the zero cross flag, which holding means are connected in series with each other;

frequency error detection means for detecting an inclination of a phase error curve from outputs of the
25 respective "n" pieces of holding means, and converting the



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inclination into a frequency error;

phase controlling loop filter means for receiving a phase error signal which is an output of the phase error detection means and a frequency error signal which is an output of the frequency error detection means as input signals when the digital signal obtained by the sampling is the VFO pattern signal, and receiving the phase error signal which is the output of the phase error detection means as an input signal when the obtained digital signal is a signal other than the VFO pattern signal; and

oscillator means for generating a reproduction clock on the basis of an output of the phase controlling loop filter means.

3. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

phase error information detection means for detecting phase error information from a random signal area in the digital data;

frequency error information detection means for detecting frequency error information from the random signal area in the digital data; and

a feedback loop for locking a phase of the reproduction



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clock and a phase of a clock component included in the reproduction digital signal on the basis of the phase error information and the frequency error information.

- 5 4. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

10 waveform equalization means for emphasizing a predetermined frequency band of a reproduction signal;

A/D conversion means for sampling the reproduction signal, the predetermined frequency band of which is emphasized by the waveform equalization means, using a reproduction clock at a time when a digital signal is reproduced, to obtain a digital
15 signal;

low-band component suppression means for suppressing low-band noises of the digital signal obtained by the sampling;

20 zero cross detection means for detecting a position where an output of the low-band component suppression means crosses a zero level, and outputting a zero cross flag;

phase error detection means for detecting a phase error from data in the vicinity of a zero cross, using the zero cross flag and the output of the low-band component suppression means;

25 "n" pieces of holding means for holding continuous "n" ("n" is a positive integer) pieces of the phase errors on the basis



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of the zero cross flag, which holding means are connected in series with each other;

frequency error detection means for detecting an inclination of a phase error curve from outputs of the
5 respective "n" pieces of holding means, and converting the inclination into a frequency error;

phase controlling loop filter means for receiving a phase error signal which is an output of the phase error detection means and a frequency error signal which is an output of the
10 frequency error detection means, as input signals; and

oscillator means for generating a reproduction clock on the basis of an output of the phase controlling loop filter means.

15 5. The phase-locked loop apparatus of Claim 2 or 4 wherein the phase error detection means comprises:

first holding means and second holding means for holding amplitudes of reproduction signals at adjacent zero cross positions for each zero cross, on the basis of the zero cross
20 flag;

subtraction means for receiving an output of the first holding means and an output of the second holding means as inputs;

polarity decision means for deciding whether a
25 reproduction waveform at a timing when the amplitude is held



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by the first holding means is a leading edge or a trailing edge,
on the basis of previous and subsequent data; and

sign manipulation means for manipulating a sign of an output
of the subtraction means on the basis of an output of the polarity
5 decision means.

6. The phase-locked loop apparatus of Claim 2 or 4 wherein
the frequency error detection means comprises:

plural subtraction means each obtaining a difference
10 between the phase errors output by predetermined two holding
means among the "n" pieces of holding means;

polarity decision means for deciding which is a polarity
of an output of each of the plural subtraction means among
positive, negative, and zero;

15 selection means for removing information at a
discontinuous point of the phase error curve on the basis of
plural inclination information output by the plural subtraction
means, and selecting information of an inclination where
frequency information is obtained stably;

20 balancing means for balancing the inclination information
selected by the selection means; and

a gain stage for arbitrarily adjusting a gain of an output
of the balancing means, and outputting the adjusted gain to the
phase controlling loop filter means.

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7. The phase-locked loop apparatus of Claim 2 or 4 wherein the frequency error detection means of Claim 6 is included and

the phase controlling loop filter means comprises:

5 phase error absolute value conversion means for converting the output of the phase error detection means into an absolute value;

phase decision means for deciding a magnitude of the obtained absolute value with a predetermined threshold;

10 start time setting means for manipulating a control start time so as to start an operation of a loop filter from the vicinity of a zero phase as a stable point of a phase curve when control is executed using the phase error signal on the basis of an output of the selection means of the frequency error
15 detection means of Claim 6 and an output of the phase decision means; and

loop filter means for outputting a control signal for the oscillator means on the basis of an output of the start time setting means.

20

8. The phase-locked loop apparatus of Claim 2 or 4 wherein the phase controlling loop filter means comprises:

frequency error absolute value conversion means for converting the output of the frequency error detection means
25 into an absolute value;



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frequency decision means for deciding a magnitude of the obtained absolute value with a predetermined threshold;

error selection means for performing switching on the basis of an output of the frequency decision means, so that control
5 is executed using only the phase error signal when a frequency of the reproduction clock is within a phase locked range, and using only the frequency error signal when the frequency of the reproduction clock is outside the phase locked range; and

loop filter means for outputting a control signal for the
10 oscillator means on the basis of an output of the error selection means.

9. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format,
15 and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

acquisition phase error information detection means for detecting acquisition phase error information from a single frequency data area comprising a single frequency in the data
20 format;

tracking phase error information detection means for detecting tracking phase error information from a random signal data area comprising a random signal in the digital data; and

a feedback loop for locking a phase of the reproduction
25 clock and a phase of a clock component included in the



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reproduction digital signal on the basis of the acquisition phase error information and the tracking phase error information.

- 5 10. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

A/D conversion means for sampling digital data in the data
10 format with a reproduction clock, to obtain a digital data signal;

band-pass filter means for removing direct current components from the digital data signal obtained by the sampling, during reproduction of a single frequency data area in the data
15 format;

zero cross detection means for detecting positions where an output signal of the band-pass filter and the digital data signal cross a zero level, and outputting respective zero cross flags;

20 cycle counter means for starting counting with the zero cross flag as a start point;

acquisition phase error detection means for detecting a phase error from the output signal of the band-pass filter at a timing when a timing signal is obtained by the cycle counter
25 means;



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tracking phase error detection means for detecting a phase error of the digital data signal on the basis of the zero cross flag;

loop filter means for receiving a phase error signal which
5 is an output of the acquisition phase error detection means as an input signal when the digital signal obtained by the sampling is a VFO pattern signal, and receiving a phase error signal which is an output of the tracking phase error detection means as an input signal when the obtained digital signal is a signal other
10 than the VFO pattern signal;

D/A conversion means for converting an output signal of the loop filter means into an analog signal; and

oscillator means for generating the reproduction clock on the basis of the analog signal output by the D/A conversion
15 means.

11. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction
20 digital signal, comprising:

first phase error information detection means for obtaining first phase error information from prediction of a zero cross position in a random signal area in the digital data;

second phase error information detection means for
25 detecting second phase error information from a random signal



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in the digital data; and

a feedback loop for locking a phase of the reproduction clock and a phase of a clock component included in the reproduction digital signal on the basis of the first phase error information and the second phase error information.

12. A phase-locked loop apparatus which reads digital data recorded on a recording medium in a predetermined data format, and generates a reproduction clock for obtaining a reproduction digital signal, comprising:

loop gain control means for outputting a loop gain control signal for increasing a phase-locking capacity for a predetermined period from a phase-locking start;

A/D conversion means for sampling the digital data with a reproduction clock, to obtain a digital data signal;

zero cross position prediction means for predicting a zero cross position of random data in the digital data signal obtained by the sampling;

acquisition phase error detection means for detecting phase error information of the random data, from an output signal of the zero cross position prediction means and the digital data signal;

zero cross detection means for detecting a position where the obtained digital data signal crosses a zero level, and outputting a zero cross flag;



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tracking phase error detection means for detecting a phase error of the digital data signal on the basis of the zero cross flag;

loop filter means for receiving a phase error signal which
5 is an output of the acquisition phase error detection means as an input signal, and receiving a phase error signal which is an output of the tracking phase error detection means as an input signal;

D/A conversion means for converting an output signal of
10 the loop filter into an analog signal; and

oscillator means for generating the reproduction clock on the basis of the analog signal output by the D/A conversion means.



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