

Claims

1. (Currently amended) A layered structure, comprising:
a monolithic substrate having a continuous portion and a porous portion;
a first epitaxial metal layer over the monolithic substrate; and
a first semiconductor layer over the first epitaxial metal layer,
wherein the first epitaxial metal layer is directly over the monolithic substrate, and wherein the first epitaxial metal layer is in direct contact with the porous portion of the monolithic substrate,
or
further comprising a first rare earth oxide layer, wherein the first rare earth oxide layer is between the monolithic substrate and the first epitaxial metal layer and directly over the monolithic substrate, and wherein the porous portion of the monolithic substrate borders ~~[[a]]~~ the first rare earth oxide layer ~~that is directly over the monolithic substrate~~ without any transition layer in between.
2. (Original) The layered structure of claim 1, wherein the monolithic substrate includes one or more group IV elements selected from a group of silicon (Si), germanium (Ge), silicon on insulator (SOI), and SiGe.
3. (Canceled)
- ~~34.~~ (Original) The layered structure of claim 1, wherein the porous portion has at least a first region and a second region that are distributed at different locations horizontally, vertically or at another dimension, and wherein the first region and the second region have different porosities.
5. (Canceled)
- ~~46.~~ (Currently amended) The layered structure of claim ~~[[5]]~~1, wherein the first epitaxial metal layer covers a portion of an upper surface of the first rare earth oxide layer, and
wherein the first epitaxial metal layer aligns with the porous portion of the monolithic substrate with the first rare earth oxide layer in between.
- ~~57.~~ (Original) The layered structure of claim 1, further comprising:

a second semiconductor layer over the first semiconductor layer; and
a second metal layer over the second semiconductor layer.

68. (Currently amended) The layered structure of claim 1, further comprising:
a non-continuous rare earth oxide layer over the monolithic substrate,
wherein the non-continuous rare earth oxide layer has at least an empty region among other
portions of the non-continuous rare earth oxide layer, and
wherein the first epitaxial metal layer is filled within the empty region.

79. (Previously presented) The layered structure of claim 68, wherein the first semiconductor
layer is over the empty region filled with the first epitaxial metal layer and the other portions of the
non-continuous rare earth oxide layer, and the layered structure further comprises a second
semiconductor layer over the first semiconductor layer.

~~108~~. (Original) The layered structured of claim 86, wherein the first semiconductor layer is
located within the empty region and over the first metal epitaxial layer, and the layered structure
further comprises a second semiconductor layer over the empty region filled with the first
semiconductor layer on top of the first epitaxial metal layer, and the other portions of the non-
continuous rare earth oxide layer.

~~119~~. (Previously presented) The layered structure of claim 68, wherein the porous portion of the
monolithic substrate aligns with the first epitaxial metal layer.

~~1210~~. (Original) The layered structure of claim 1, further comprising:
a second semiconductor layer over the first semiconductor layer, and
a third semiconductor layer over the second semiconductor layer.

~~1311~~. (Previously presented) The layered structure of claim ~~1210~~, wherein an interface between the
first semiconductor and the second semiconductor, or between the second semiconductor layer and

third semiconductor layer includes a first rare earth oxide sublayer, an epitaxial metal layer, or an epitaxial metal layer over a first rare earth oxide layer.

1412. (Previously presented) The layered structure of claim **1311**, wherein the interface further includes a second rare earth oxide layer over the epitaxial metal layer.

1513. (Original) The layered structure of claim **1210**, wherein the first semiconductor layer and the second semiconductor layer jointly form a first device layer, and
wherein the second semiconductor layer and the third semiconductor layer jointly form a second device layer.