

CATALYST INFLUENCED PATTERN TRANSFER TECHNOLOGY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 62/591,326 filed November 28, 2017 entitled "Forming Three-Dimensional Memory Architectures Using Catalyst Mesh Patterns," U.S. Provisional Patent Application No. 62/665,084 filed on May 1, 2018 entitled "Multilayer Electrochemical Etch process for Semiconductor Device Fabrication," U.S. Provisional Patent Application No. 62/701,049 filed on June 20, 2018 entitled Catalyst-Based Electrochemical Etch Process for Semiconductor Device Fabrication," and U.S. Provisional Patent Application No. 62/729,361 filed on September 10, 2018 entitled "Catalyst Assisted Chemical Etching Technology: Applications In Semiconductor Devices," all of which are incorporated herein by reference in their entirety for all purposes.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0002] This invention was made with government support under Grant No. EEC1160494 awarded by the National Science Foundation and Grant No. FA8650-15-C-7542 awarded by the Air Force Research Laboratory. The U.S. government has certain rights in the invention.

TECHNICAL FIELD

[0003] Various embodiments of the present technology generally relate to semiconductor device architectures and manufacturing techniques. More specifically, some embodiments of the present technology relate to silicon etching using catalyst influenced chemical etching technology with application to three-dimensional memory architectures and transistors.

BACKGROUND

[0004] Semiconductor manufacturing of various types of transistors, memories, integrated circuits, photonic devices and other semiconductor devices have led to the proliferation of modern computing devices and other electronic systems. For example, computers, mobile phones, automobiles, consumer electronics, and the like are all a direct product of advancements in semiconductor manufacturing. An integral part of fabrication of these devices is pattern transfer. Dry plasma etching processes, which are used in the semiconductor industry for anisotropically etching highly controlled nanopatterns, require expensive vacuum equipment and cannot retain

1 cross-section shape easily when patterning high aspect ratios. They suffer from etch challenges
2 such as Aspect Ratio Dependent Etching (ARDE) and etch taper.

3 SUMMARY

4 **[0005]** Various embodiments of the present technology generally relate to memory
5 architectures and manufacturing techniques. More specifically, some embodiments of the present
6 technology relate to silicon etching using catalyst influenced chemical etching technology with
7 application to three-dimensional memory architectures and transistors.

8 **[0006]** In one embodiment of the present technology, a method for preventing substantial
9 collapse of high aspect ratio semiconducting structures by catalyst influenced chemical etching
10 comprises patterning a catalyst layer on a surface of a semiconducting material, where the
11 catalyst layer comprises an intended design and lithographic links. Furthermore, the lithographic
12 links substantially connect one or more isolated features of the catalyst layer and/or the
13 semiconducting material. The method further comprises exposing the patterned catalyst layer on
14 the surface of the semiconducting material to an etchant, where the patterned catalyst layer
15 causes etching of the semiconducting material to form interconnected high aspect ratio structures.

16 **[0007]** In another embodiment of the present technology, a method for preventing
17 substantial collapse of high aspect ratio semiconducting structures comprises creating a structure
18 with a capping material deposited on either a patterned catalyst layer or on top of low height
19 structures. The method further comprises exposing the structure to an etchant. The method
20 additionally comprises forming high aspect ratio semiconducting structures by using catalyst
21 influenced chemical etching on the structure with the capping material to prevent substantial
22 collapse of the high aspect ratio semiconducting structures.

23 **[0008]** In a further embodiment of the present technology, an apparatus for catalyst
24 influenced chemical etching comprises a plurality of sensors configured to detect an etch state of
25 a semiconducting material.

26 **[0009]** In another embodiment of the present technology, a method for making substantially
27 non-collapsing alternating multi-layer stacked nanostructures comprises creating a material stack
28 comprising two or more layers of alternating semiconducting films, where each of the two or more
29 layers of alternating semiconducting films is different from another in at least one of the following
30 properties: material, doping concentration and dopant material. The method further comprises
31 etching the material stack by catalyst influenced chemical etching such that layers differing in the

properties produce etched nanostructures differing in at least one of the following: morphology, porosity, etch rates and thermal processing rates.

[0010] In a further embodiment of the present technology, a method for making substantially non-collapsing alternating multi-layer stacked features comprises creating a material stack comprising two or more layers of alternating semiconducting films, where each of the two or more layers of alternating semiconducting films is different from another in at least one of the following properties: material, doping concentration and dopant material. The method further comprises etching the material stack by a crystallographic orientation dependent etch to form a taper along a crystal plane. The method additionally comprises etching the taper along the crystal plane to reveal one of the two or more layers of alternating semiconducting films while etching part of another layer to create a staircase structure.

[0011] Embodiments of the present technology also include computer-readable storage media containing sets of instructions to cause one or more processors to perform the methods, variations of the methods, and other operations described herein.

[0012] While multiple embodiments are disclosed, still other embodiments of the present technology will become apparent to those skilled in the art from the following detailed description, which shows and describes illustrative embodiments of the technology. As will be realized, the technology is capable of modifications in various aspects, all without departing from the scope of the present technology. Accordingly, the drawings and detailed description are to be regarded as illustrative in nature and not restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Embodiments of the present technology will be described and explained through the use of the accompanying drawings in which:

[0014] Fig. 1A illustrates a jet and flash imprint lithography (J-FIL) enabled catalyst influenced chemical etching (CICE) for shaped nanowires according to one or more embodiments of the present technology;

[0015] Fig. 1B depicts the cross-sectional views of fabricating nanowires using the steps described in Fig. 1A in accordance with one or more embodiments of the present technology;

[0016] Fig. 2 illustrates a SiSE (Silicon Superlattice Etch) process control according to one or more embodiments of the present technology;

1 **[0017]** Figs. 3A-3B show the steep interface between porous and non-porous layers after
2 SiSE on a substrate with alternating layers of epitaxial silicon with different doping concentrations
3 according to one or more embodiments of the present technology;

4 **[0018]** Fig. 4 shows an SEM cross-section of silicon nanowires created with gold and
5 platinum catalysts, and zoomed in images of the catalyst meshes at the bottom of the
6 nanostructures, according to one or more embodiments of the present technology;

7 **[0019]** Fig. 5A shows how connecting links in the catalyst material as well as the
8 semiconductor structures can be used to connect one or more isolated catalysts and high aspect
9 ratio (HAR) nanostructures simultaneously according to one or more embodiments of the present
10 technology;

11 **[0020]** Fig. 5B provides a top view illustrating disconnected regions representing the
12 geometry of the catalyst features and connected regions that define the high aspect ratio
13 structures that remain after SiSE according to one or more embodiments of the present
14 technology;

15 **[0021]** Figs. 6A-6E illustrate process chamber configurations for CICE according to one or
16 more embodiments of the present technology;

17 **[0022]** Figs. 7A-7B illustrate an embodiment of MSP-CICE process chamber with a
18 horizontal substrate according to one or more embodiments of the present technology;

19 **[0023]** Fig. 8A illustrates an embodiment of MSP-CICE tool setup according to one or more
20 embodiments of the present technology;

21 **[0024]** Fig. 8B illustrates an example of a detailed process chamber layout according to
22 one or more embodiments of the present technology;

23 **[0025]** Fig. 8C illustrates an example of a process flow according to one or more
24 embodiments of the present technology;

25 **[0026]** Fig. 9 illustrates a genetic algorithm based controller which can be used to determine
26 optimum process parameters for a targeted output according to one or more embodiments of the
27 present technology;

28 **[0027]** Figs. 10A-10E illustrate catalyst mesh examples according to one or more
29 embodiments of the present technology;

1 **[0028]** Fig. 11 shows a process flow for HAR etch of channels and slits with a catalyst mesh
2 pattern similar to that shown in Fig 10;

3 **[0029]** Fig. 12 illustrates a sacrificial process flow for vertical channel 3D NAND according
4 to one or more embodiments of the present technology;

5 **[0030]** Fig. 13 shows the process flows and various pathways to make 3D NAND arrays
6 with SiSE according to one or more embodiments of the present technology;

7 **[0031]** Figs. 14-16 show some of the process flows for processing alternating layers of
8 porous and non-porous silicon layers that are created by SiSE to create vertical channel 3D NAND
9 arrays according to one or more embodiments of the present technology;

10 **[0032]** Fig. 17 depicts an embodiment of the 3D NAND architecture with vertical gates and
11 horizontal silicon channels according to one or more embodiments of the present technology;

12 **[0033]** Fig. 18A-18C show layouts and dimensions of 3D NAND according to one or more
13 embodiments of the present technology;

14 **[0034]** Figs.19A-19C show an exemplary fabrication template for making patterns shown
15 in Figs. 18A-18C;

16 **[0035]** Fig. 19D provides an example of a pattern with lithographic links where the links are
17 made with imprint lithography (whose template is made with electron beam lithography), and the
18 dots are aligned and printed using imprint or photolithography or vice versa;

19 **[0036]** Figs. 20A-20J illustrate exemplary photolithography process steps to pattern the
20 CICE catalyst according to one or more embodiments of the present technology;

21 **[0037]** Figs. 21A-21H show the process flow for making a catalyst pattern with substantially
22 connected catalyst features using self-assembly and lithography according to one or more
23 embodiments of the present technology;

24 **[0038]** Fig. 22 illustrates an example of a 3D NAND staircase etch according to one or more
25 embodiments of the present technology;

26 **[0039]** Fig. 23 illustrates a process of staircase etch on bulk silicon with alkaline etchants
27 or angled plasma etch to create contact pads for word lines according to one or more
28 embodiments of the present technology;

1 **[0040]** Fig. 24 illustrates an exemplary DRAM design with transistor, capacitor and
2 interconnect material on nanowires etched by CICE according to one or more embodiments of
3 the present technology;

4 **[0041]** Figs. 25A-25B illustrate two process flows for CICE wet anisotropic etch to create
5 high aspect ratio pillars without collapse according to one or more embodiments of the present
6 technology;

7 **[0042]** Fig. 26 illustrates a SEM image showing collapse of unsupported features vs
8 supported features after CICE on silicon according to one or more embodiments of the present
9 technology;

10 **[0043]** Fig. 27A illustrates a 14nm FinFET with a taper angle of $\sim 85^\circ$, and a physical Half
11 Pitch (HP) of 24nm (Ref: TechInsights);

12 **[0044]** Fig. 27B depicts the maximum fin height for different fin widths and etch taper angles
13 according to one or more embodiments of the present technology.

14 **[0045]** Fig. 28 is a plot illustrating a maximum height of a fin with no taper before lateral
15 collapse along the length of a 50nm long fin, without any support/assist features;

16 **[0046]** Fig. 29 illustrates an example of a process flow for making finFETs with CICE
17 according to one or more embodiments of the present technology;

18 **[0047]** Figs. 30A-30E illustrates an example of FinFET fabrication process steps after CICE
19 according to one or more embodiments of the present technology;

20 **[0048]** Fig. 31 illustrates an example of a process flow for making nanosheet FETs and
21 lateral nanowire FETs with CICE according to one or more embodiments of the present
22 technology;

23 **[0049]** Fig. 32A illustrates connecting links when number of fins is greater than 1;

24 **[0050]** Fig. 32B illustrates links connecting all the fins with isolated catalysts (top) or with
25 connected links and connected catalysts (bottom);

26 **[0051]** Fig. 32C is a plot illustrating critical heights before collapse along the length of the
27 connected fin structure is shown for different fin widths f and for number of fins ranging from 1 to
28 10; and

1 **[0052]** Fig. 32D is a plot illustrating the critical heights before collapse along the width of
2 the connected fin structure is shown for different fin widths f and for number of fins ranging from
3 1 to 10.

4 **[0053]** The drawings have not necessarily been drawn to scale. Similarly, some
5 components and/or operations may be separated into different blocks or combined into a single
6 block for the purposes of discussion of some of the embodiments of the present technology.
7 Moreover, while the technology is amenable to various modifications and alternative forms,
8 specific embodiments have been shown by way of example in the drawings and are described in
9 detail below. The intention, however, is not to limit the technology to the particular embodiments
10 described. On the contrary, the technology is intended to cover all modifications, equivalents,
11 and alternatives falling within the scope of the technology as defined by the appended claims.

12 DETAILED DESCRIPTION

13 **[0054]** Various embodiments of the present technology describe a novel anisotropic
14 etching process. A fabrication tool for this purpose is also disclosed. This shall enable adoption
15 of this technology in making semiconductor devices. Some embodiments use a catalyst
16 influenced chemical etching (CICE) for manufacture of transistors and various memory
17 architectures. Moreover, various embodiments of the CICE process have demonstrated
18 extremely high aspect ratios without loss of feature size.

19 **[0055]** Various embodiments of the present technology also provide various control
20 schemes in catalyst based chemical etching. A wafer scale Multi Scale Precision Catalyst
21 Influenced Chemical Etching (MSP-CICE) fabrication tool for this purpose is also disclosed.
22 Some embodiments use various control schemes and tool designs to extend the capabilities of
23 CICE from small area (sub-150mm substrates) with no etch depth control in literature today, to
24 large area (e.g. 300mm Si wafers) with local and global control and metrology. This shall enable
25 adoption of this technology in making semiconductor devices such as 3D NAND Flash, DRAM,
26 FinFETs and Nanosheet transistors.

27 **[0056]** Various embodiments of the present technology generally relate to memory
28 architectures and manufacturing techniques. More specifically, some embodiments of the present
29 technology relate to silicon etching using catalyst influenced chemical etching technology with
30 application to three-dimensional memory architectures and transistors. Scalability of advanced
31 memory architectures by current pattern transfer techniques is limited by non-zero taper, sidewall
32 damage and etch mask degradation due to high aspect ratio plasma etching. Nonvolatile

1 semiconducting memories, such as three-dimensional (3D) NAND flash, need extremely high
2 aspect ratio etching of > 64 layers of alternating material to increase the storage capacity of flash
3 drives. With increasing layers, the cost and reliability of anisotropic high aspect ratio channel and
4 trench etching, as well as a staircase etch for defining contacts to each layer, becomes a major
5 limiting factor for scaling. A non-zero plasma etch taper angle limits the maximum number of tier
6 stacking that can be reliably achieved.

7 **[0057]** Dry plasma etching processes, which are used in the semiconductor industry for
8 anisotropically etching highly controlled nanopatterns, require expensive vacuum equipment and
9 cannot retain cross-section shape easily when patterning high aspect ratios. They suffer from
10 etch challenges such as Aspect Ratio Dependent Etching (ARDE) and etch taper. For the 3D
11 NAND Flash designs, etching circular channels and rectangular slits simultaneously cannot be
12 achieved reliably with plasma etching with accurate control of sidewalls. Similarly, for the features
13 with connecting links, the sub-10nm links between pillars cannot be retained over high aspect
14 ratios.

15 **[0058]** Furthermore, DRAM scaling is limited by the area occupied by the capacitor and the
16 cell size factor. Hence, the current techniques in scaling memory architectures are limited due to
17 the high number of lithography and high aspect ratio etch steps. Various embodiments provide
18 improved techniques for DRAM manufacturing.

19 **[0059]** In the following description, for the purposes of explanation, numerous specific
20 details are set forth in order to provide a thorough understanding of embodiments of the present
21 technology. It will be apparent, however, to one skilled in the art that embodiments of the present
22 technology may be practiced without some of these specific details.

23 **[0060]** The techniques introduced here can be embodied as special-purpose hardware
24 (e.g., circuitry), as programmable circuitry appropriately programmed with software and/or
25 firmware, or as a combination of special-purpose and programmable circuitry. Hence,
26 embodiments may include a machine-readable medium having stored thereon instructions which
27 may be used to program a computer (or other electronic devices) to perform a process. The
28 machine-readable medium may include, but is not limited to, optical disks, compact disc read-
29 only memories (CD-ROMs), magneto-optical disks, ROMs, random access memories (RAMs),
30 erasable programmable read-only memories (EPROMs), electrically erasable programmable
31 read-only memories (EEPROMs), magnetic or optical cards, flash memory, or other type of media
32 / machine-readable medium suitable for storing electronic instructions.

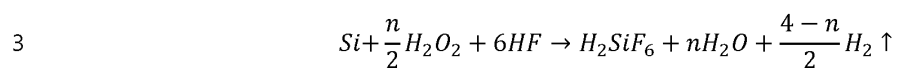
1 **[0061]** The phrases "in some embodiments," "according to some embodiments," "in the
2 embodiments shown," "in other embodiments," and the like generally mean the particular feature,
3 structure, or characteristic following the phrase is included in at least one implementation of the
4 present technology, and may be included in more than one implementation. In addition, such
5 phrases do not necessarily refer to the same embodiments or different embodiments.

6 **[0062]** Various embodiments of the present technology use catalyst influenced chemical
7 etching (CICE) for manufacture of transistors and various memory architectures. CICE is a
8 catalyst based etching method that can be used on semiconductors such as Si, Ge, $\text{Si}_x\text{Ge}_{1-x}$, GaN,
9 InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. as well as multilayers of the semiconductors. CICE
10 uses a catalyst to etch semiconducting substrates and it has been used to fabricate high aspect
11 ratio features with patterning techniques such as photolithography, electron beam lithography,
12 nanosphere lithography, block co-polymers, laser interference lithography, colloidal lithography,
13 double patterning, quad patterning, nanoimprint lithography and anodized aluminum oxide (AAO)
14 templates to pattern the catalyst. The catalyst can be used in conjunction with etch-retarding
15 materials such as polymer, Cr, etc.

16 **[0063]** In some embodiments, this setup can be immersed in a solution containing an
17 etchant (e.g., fluoride species HF, NH_4F , Buffered HF, H_2SO_4 , H_2O) and an oxidant (H_2O_2 , V_2O_5 ,
18 KMnO_4 , dissolved oxygen, etc.). Other chemicals such as alcohols (ethanol, isopropyl alcohol,
19 ethylene glycol), materials to regulate etch uniformity (surfactants, soluble polymers, dimethyl
20 sulfoxide-DMSO), solvents (DI water, DMSO etc.), and buffer solutions can also be included in
21 the etch composition. The chemicals used can depend on the semiconducting substrate to be
22 etched. Non-aqueous etchants can also be used if needed. The etchants can be in liquid or
23 vapor phase. An embodiment of such an etchant for silicon substrates comprises DI H_2O , H_2O_2 ,
24 Ethanol and HF.

25 **[0064]** Materials such as metals (e.g., Ag, Au, Pd, Pt, Cu, W, Ru, Ir), compounds such as
26 TiN, TaN, RuO_2 , IrO_2 and other conductive metal oxides and nitrides, Graphene, carbon etc. can
27 act as catalysts for CICE. The mechanism for the CICE process for etching Si may involve the
28 reduction of the oxidant by a catalyst, thereby creating positively charged holes h^+ . These holes
29 are then injected through the metal to the metal-semiconductor interface thereby oxidizing the
30 semiconductor underneath the metal. The oxidized silicon is dissolved by the fluoride component
31 of the etchant that diffuses from the sides of and through the catalyst and the soluble products
32 diffuse away. For CICE of silicon with HF and H_2O_2 , this redox reaction can also produce

1 hydrogen gas. The variable $n=2$ to 4 is determined by the ratio of oxidant to HF which determines
 2 the etch regime that occurs:



4
 5 **[0065]** The etch rate and resulting morphology of this process depends on dopant type,
 6 concentration, catalyst film thickness and etchant concentrations. Both electric and magnetic
 7 fields have been used to achieve greater uniformity/control of porosity due to diffusion of holes
 8 during the etch process. The resulting substrate with the catalyst mesh is placed in an etchant
 9 solution and etched precisely to a certain depth actively controlled by electrical fields, temperature
 10 gradients and optical imaging systems that can determine the etch depth in situ. After CICE, the
 11 catalyst can be removed using chemical or plasma etching, such as with aqua regia, chlorine-
 12 based plasmas, etc.

13 **[0066]** Diamond-shaped cross-section silicon nanowires made using Jet and Flash Imprint
 14 Lithography (J-FIL) and CICE with gold catalyst have been successfully demonstrated (see, e.g.,
 15 Fig. 1). Capacitors made with diamond shaped silicon nanowires show a 90% higher specific
 16 capacitance than NWs with circular cross section of same pitch, and highest specific capacitance
 17 per area of NWs in literature. J-FIL and CICE have the potential to fabricate Si nanostructures at
 18 fabrication costs of <\$1/wafer based on standard cost models.

19 **[0067]** Fig. 1A illustrates a J-FIL enabled catalyst influenced chemical etching (CICE)
 20 process 100 for making nanowires according to one or more embodiments of the present
 21 technology. As illustrated in Figs. 1A-1B, in process step 110, nano-features 111 (e.g., resist
 22 material) can be imprinted on silicon substrate 112. The material (e.g., resist) may remain in the
 23 trenches 113 after the imprint process. In process step 120, "descum" etching can be performed
 24 to remove the resist residual layer thickness (RLT) as well as remove the resist in the trenches
 25 113. One example of a descum etch uses oxygen and argon plasma to etch the resist material.
 26 In process step 130, gold (Au) 131 can be deposited in trenches 113 and on top of nano features
 27 111 using a directional deposition process such as electron beam evaporation. An adhesion layer
 28 such as Ti may also be deposited prior to deposition of Gold. In process step 140, CICE can be
 29 used to form trenches 141, where gold 131 is located at the bottom of trenches 141 and on top of
 30 nano features 111. In process step 150, gold (Au) 131 and resist 111 can be removed and the
 31 structure can be cleaned using plasma etching or chemical etchants such as aqua regia,
 32 potassium iodide, and piranha in liquid or vapor form. Fig. 1B depicts the cross-sectional views

1 of fabricating nanowires using the steps described in Fig. 1A in accordance with one or more
2 embodiments of the present technology.

3 **[0068]** CICE is a superset of a process called Metal Assisted Chemical Etching (MACE).
4 Apart from metals, there are certain non-metallic catalysts such as Graphene or TiN, TaN, RuO₂,
5 IrO₂ etc. that can also be potentially be used as catalysts. Further, while the catalysts usually
6 locally assist in the chemical etching by digging into the substrate in the presence of etchants and
7 oxidants, they can also locally inhibit the etch, as in the case of InP. To encompass all such
8 processes, various embodiments refer to the process Catalyst Influenced Chemical Etching
9 (CICE).

10 **[0069]** However, the CICE anisotropic wet etch method used in the high aspect ratio etch
11 steps does not currently have precise etch depth control and wafer scale fabrication.
12 Discontinuous catalyst features tend to wander during the CICE process and cause defects.
13 Catalysts used are not easy to etch with plasma or wet etch without re-deposition or undercut.
14 Lift-off process, currently used to pattern noble metal catalyst, has high defectivity. Various
15 embodiments of the present technology enable etching of arbitrary nanopatterns with feature
16 sizes ranging from mm to nm by precisely controlling various sensors and actuators such as the
17 chemistry of the etchant solution, electric field, the optical/ spectral properties of the
18 nanostructures etc.

19 **[0070]** In accordance with various embodiments, CICE can be used to create
20 nanostructures of bulk material or alternating layers of material such as superlattices. CICE of
21 bulk material can be used in devices such as finFETs and nanowire sensors. Superlattice
22 nanostructures have applications such as 3D NAND Flash memory devices and nanosheet
23 transistors. Superlattices can be created by performing CICE on bulk semiconducting substrates
24 with time-varying electric fields, or on substrates with alternating layers of semiconducting
25 material differing in doping concentration, material, dopant type, etc. For an embodiment using
26 silicon as at least one of the materials in the substrate, the process of CICE to create superlattices
27 is described as Silicon Superlattice Etching (SiSE), described below.

28 **Silicon Superlattice Etching (SiSE)**

29 **[0071]** SiSE can be used on bulk silicon wafers as well as alternating layers of silicon with
30 different doping concentrations. An etchant (such as Hydrofluoric acid HF), an oxidant (such as
31 Hydrogen peroxide H₂O₂), and optionally a low surface tension liquid (such as Ethanol) and DI
32 water can etch semiconducting substrates preferentially at the location of a catalyst (such as Ag,

1 Au, Pd, Pt, Cu, W, Ru, TiN, RuO₂, IrO₂, Graphene, etc.). Non-aqueous etchants can also be used
2 if needed. Lithography techniques (such as photolithography, electron beam lithography, double
3 patterning, quad patterning, nanoimprint- lithography etc.) can be used to define the catalyst
4 features. The resulting substrate with the catalyst mesh is placed in the MSP-CICE tool and
5 etched precisely to a certain depth actively controlled by electrical fields, thermal actuators and
6 optical imaging systems that can determine the etch depth based on the electrical and optical
7 properties during etch.

8 **[0072]** Other semiconductors such as IVs, II-VIs, III-Vs, alloys and heterojunction materials
9 that can be etched with superlattice etching are Ge, SixGe_{1-x}, GaN, InP, GaAs, InAs, GaP, InGaS,
10 InGaP, SiC, and the like. They can also be included in the material design space but are not
11 further discussed herein for various reasons such as high cost of material and deposition, lack of
12 commercially available methods of deposition and characterization, etc. Various embodiments of
13 the SiSE process containing silicon can be utilized. Reliable and large area wafer scale etching
14 with SiSE process is currently not present in traditional technologies. Various embodiments shall
15 incorporate various technologies to enable this.

16 **[0073]** Silicon superlattice etching (SiSE) uses the catalyst to etch a semiconducting
17 substrate while simultaneously creating a superlattice with alternating layers where at least one
18 of the layers is porous. The alternating layers are formed by electric field parameter modulation
19 and/or etching through layers with alternating doping characteristics. Fig. 2 illustrates a SiSE
20 process control 200 according to one or more embodiments of the present technology. As
21 illustrated in Fig. 2, patterning operation 210 can generate a patterned catalyst on the silicon
22 substrate. In accordance with various embodiments, a bulk substrate (as illustrated in 212) may
23 be used or a substrate with alternating doping layers (as illustrated in 214) may be used. Either
24 the bulk substrate or the substrate with alternating doping layers may be loaded into a silicon
25 superlattice etch tool in loading operation 230. The SiSE process 240 can be precisely controlled
26 to generate high-aspect ratio nanostructures 250. In accordance with various embodiments, the
27 high-aspect ratio nanostructures 250 may have a ratio of height to critical dimension (e.g.,
28 average of the diameter of the base and the top for nanowire) of 4:1, 5:1, or more.

29 **[0074]** Various feedback parameters 260 can be directly measured directly or estimated
30 from direct measurements. These parameters can include, but are not limited to etchant
31 performance parameters (e.g., concentration, volume, flow rate, Reynolds number, refractive
32 index, etc.), electric field parameters, (current, voltage, resistance, capacitance, etc.), optical
33 variations across the whole wafer (e.g., reflectance, intensity, etc.), ambient environmental

1 parameters (e.g., temperature, pressure, inert gas flow rate, vapor pressures, etc.), and/or other
2 parameters. These can be used to generate a feedback signal which can be used in conjunction
3 with an input etch control signal to control various system parameters (e.g., flow rates, etchant
4 turbulence, temperature, pressure, concentrations, illuminations, electric field parameters such
5 as current, voltage, resistance, capacitance, frequency, duty cycle, amplitude, waveform type,
6 distance between electrodes, and the like).

7 **[0075]** In the case of bulk silicon (as illustrated in 212) that is etched by the patterned
8 catalyst along with a modulated electric field, the alternating layers differ in porosity. Modulation
9 in parameters such as current density and illumination density with time can create porous
10 semiconductor multilayers. The current density can be modulated such that, for a p-type silicon
11 substrate, a positive current density causes porosity as the catalyst sinks into the silicon, and a
12 zero or negative current density gives crystalline layers with only the catalyst etch, as shown in
13 Fig. 2. This is unique compared to processes where only modulated electric field is used without
14 the presence of a catalyst, since such cases cannot produce alternating layers where the porosity
15 of one of the alternating layers is very low. Some embodiments of such a multilayer stack can
16 include one set of alternating layers with a porosity of less than 20% and another set comprising
17 layer with a porosity greater than 30%.

18 **[0076]** When epitaxial layers with alternate high and low doping concentrations are
19 deposited at sub-micron thickness per layer (e.g., as illustrated in 214), the concentration gradient
20 across the interface of the two layers is shallow due to limitations of the deposition process at
21 high deposition rates, as well as due to diffusion of dopants across the interface. This gives a
22 non-abrupt change of doping across the thickness of the stack, such as a shallow gradient across
23 the interface. With SiSE, the etch is tuned to ensure that the morphology changes from porous
24 to non-porous at a specific doping concentration, thereby changing the shallow doping
25 concentration gradient into an abrupt step function of porous/non-porous interfaces.

26 **[0077]** As SiSE progresses, the catalyst mesh etches the semiconductor material stack to
27 reveal high aspect ratio features with holes and slits for 3D NAND channels and word line
28 separation, and fins and trenches for nanosheet FETs. SiSE can be stopped by using an etch
29 stop layer and/or a timed etch. The etchant composition as well as hole-generation during the
30 process results in alternating films of differing morphologies based on their material and doping
31 concentrations. Also, the exact time at which the morphology changes can be detected by
32 measuring electrical parameters such as resistance, voltage, current, capacitance, and the like.

1 across the epitaxial layers. This information can then be used to precisely modulate the current
2 across the stack.

3 **[0078]** Figs. 3A-3B show the steep interface between porous and non-porous layers after
4 SiSE on a substrate with alternating layers of epitaxial silicon with different doping concentrations
5 according to one or more embodiments of the present technology. In Fig. 3A, interface 310
6 between layer A of porous film 320 and layer B of non-porous film 330 can be seen. In Fig. 3B
7 several collapsing walls 340 with porous and non-porous sections can be seen.

8 **CMOS Compatibility of Catalyst material for CICE**

9 **[0079]** Various embodiments of the CICE process can use a patterned catalyst that sinks
10 into the substrate as the etch progresses, leaving behind un-patterned areas as high aspect ratio
11 nanostructures. For semiconductor applications such as in transistors and memory devices, the
12 catalyst material should be CMOS-compatible to enable adoption by industry and to prevent deep-
13 level defects in silicon. Materials such as Au, Ag, Pt, Cu, Pd, W, Ni, Ru, Graphene, TiN, RuO₂
14 can be used as SiSE catalysts. The deep-level defects appear when metals such as Au and Cu
15 are processed at high temperature. As SiSE is a room- to low-temperature process, the effect of
16 such defects might be minimal. Further, CMOS compatible catalysts such as Pt, Pd, Ru, TiN etc.
17 can be used.

18 **[0080]** Fig. 4 shows an SEM cross-section of silicon nanowires created with gold and
19 platinum catalysts, and zoomed in images of the catalyst meshes at the bottom of the
20 nanostructures, according to one or more embodiments of the present technology. For a CMOS
21 compatible catalyst like platinum (Fig.4), the deposition and patterning must have high yield.
22 Platinum can be etched using plasma etching with Cl₂ to form PtCl₂. At temperatures above 210C,
23 PtCl₂ is volatile, and thus can be used as a viable method of etching the metal after deposition
24 and lithography. Similar etch methods can be used for Palladium. Another method of deposition
25 is via electrodeposition after lithography, where the metal is deposited only in areas of the
26 substrate that are not covered by resist. Alternatively, the metal is deposited on top of the
27 lithographed areas and the substrate, such as by electron beam deposition, but only the areas in
28 contact with the substrate are etched by MACE, without requiring liftoff.

29 **[0081]** To prevent wandering of the catalyst mesh and for reliable transport of etchant
30 solution: electric fields, ceilings and/or continuous patterns with connecting links can be used in
31 various embodiments. The resulting high aspect ratio features can be prevented from collapse
32 by mitigation techniques such as using low surface tension gradients, super critical drying and

1 connected features. Wandering and collapse can also be prevented by using a patterning
2 technique comprising of connecting links between desired features of both catalyst and substrate,
3 and by using controlled deposition or etch after the SiSE process to convert the high aspect ratio
4 linked features into the desired device structure.

5 **[0082]** A problem that arises during high aspect ratio etching of disconnected features is
6 that of collapse. This is extremely detrimental to yield of the device. Various embodiments solve
7 this problem by creating an interconnected nanostructure with sub-10nm assist features that can
8 prevent collapse and provide stability to the structures during and after etching. For instance, in
9 Figs. 5A-5B, a catalyst design for 3D NAND Flash is shown. After SiSE, the resulting structures
10 may be >20 microns height with sub-40nm feature size.

11 **[0083]** Fig. 5A shows how connecting links 510 in the catalyst material as well as the
12 semiconductor structures can be used to connect various isolated catalysts 520 and High Aspect
13 Ratio (HAR) nanostructures 540 simultaneously according to one or more embodiments of the
14 present technology. Fig. 5B provides a top view illustrating disconnected regions representing
15 the geometry of the catalyst features 530 and connected regions 540 that define the high aspect
16 ratio structures that remain after SiSE according to one or more embodiments of the present
17 technology. In accordance with various embodiments, isolated catalyst portions can be
18 connected using a pattern that can be generated from an algorithm used for connecting isolated
19 features using links to ensure that the HAR nanostructures stay standing, and also helps prevent
20 wandering of the catalyst mesh and creates pathways for diffusion of etchant reactants and
21 products to ensure uniform and controlled etch rates. (Fig. 5A) Since the catalyst features are
22 disconnected, wandering can occur, but may be prevented in some embodiments using electric
23 fields. The free standing features are connected to prevent collapse by buttressing the high
24 aspect ratio lines (Fig. 5B).

25 **[0084]** In accordance with various embodiments, connected link generation can be done
26 by defining nodes of catalyst material or semiconductor that would be isolated in an ideal intended
27 design. The links can be then generated to ensure that the structures etched by CICE are
28 mechanically stable. The links can also be optimized to ensure that the catalyst does not wander
29 during CICE. Optimizing for such process excursions in the design of the catalyst can be done
30 using standard algorithms such as graph theory based and recursive division methods.

31 **[0085]** The catalyst can include one or more of the following: a) lithographic links to prevent
32 wandering – these features result in gaps in the etched structures, which can be filled with material
33 using various deposition processes such as atomic layer deposition, chemical vapor deposition,

1 electroplating, etc.; and/or b) lithographic gaps to prevent collapse of the etched structures – these
2 features result in stabilizing links in the etched structures. Based on the design requirements,
3 these links may be removed using lithography and etching, selective oxidation, selective oxidation
4 and etching, etc. This can be done after deposition of stabilizing material in other areas as needed.

5 **[0086]** If the catalyst mesh comprises both lithographic links and gaps, then a linked
6 structure results. Fabrication of sub-30nm features with even smaller link connections is
7 extremely challenging. Patterning methods such as electron beam lithography can write sub-
8 10nm features but suffers from large overlay, whereas photolithography has superior overlay but
9 poor resolution. Photolithography and imprint lithography (whose template is made with electron
10 beam lithography) may be used to get the final linked structure that can then be made into a
11 nanoimprint template. Examples of such patterns are described in the 3D NAND and transistor
12 device sections.

13 **[0087]** Apart from using isolated or linked structures for catalysts, another method to extend
14 the maximum aspect ratio that may be used by various embodiments is by using ceilings.
15 Collapse prevention using a ceiling can be done by etching the features with plasma etching or
16 SiSE to a short, stable height; depositing the ceiling, and continuing the SiSE process. The
17 “ceiling” can also be at a height that is along the length of the short pillars, such as at $L/2$, where
18 L is the height of the short stable pillar. This gives additional support as the features are further
19 etched and extends the maximum aspect ratio to greater than that with the ceiling on top of the
20 short pillars. This gives structural stability to the high aspect ratio pillars and prevents collapse.

21 **[0088]** The ceiling can be deposited by angled deposition; polymer fill, etch back and ceiling
22 deposition; or methods such as spin coating. Materials that can be used for the ceiling include
23 polymers, sputtered/deposited semiconductors, metals and oxides that do not react with the CICE
24 etchants. For Si CICE etchants, materials such as Cr, Cr_2O_3 , carbon, silicon, Al_2O_3 , polymers, etc.
25 can be used. In some embodiments, the ceiling can also be made porous by an additional low
26 resolution lithography step or by a reaction to induce porosity to the ceiling material. Once the
27 substrate is etched and the catalyst is removed using a liquid or vapor chemical etch, deposition
28 of memory film or dielectric filler by methods like atomic layer deposition can be done before
29 removal of the porous ceiling. The ceiling material could also be tuned to be non-selective to
30 Atomic Layer Deposition (ALD) thereby preventing the pores from closing and blocking the
31 deposition pathways. After filling the features, the ceiling is etched or polished away. ALD can
32 also be used to close off high-aspect ratio shapes after etch to create deep holes without the use
33 of isolated catalysts.

1 **Etch Tool**

2 **[0089]** Various embodiments of the present technology provide for a unique, high-fidelity
3 nanoscale manufacturing system (Multi-scale Precision CICE or MSP-CICE) that can achieve
4 wafer-scale etching of high aspect ratio nanostructures in semiconducting materials with features
5 such as: 1) high-speed (real-time), high spatial resolution functional or geometric metrology as
6 the etch progresses for precision process monitoring and control; and/or 2) a system that enables
7 multi-scale precision control of the CICE process based on real-time metrology, and based on an
8 array of independently addressable actuators that can locally control the etch process to allow
9 controlled fabrication of devices with diverse arrays.

10 **[0090]** Figs. 6A-6E illustrates process chamber configurations for CICE according to one
11 or more embodiments of the present technology. Fig. 6A shows a system with inkjets 605, etchant
12 circulation system 610, front-side electrodes 615, electric field supply 620, polymer walls 625, and
13 backside electrode contacts and thermal actuators 630. In the embodiments illustrated in Fig. 6A,
14 silicon wafer 635 can be positioned between front-side electrodes 615 and back-side electrodes
15 630 to allow for electric field control. Fig. 6B illustrates some embodiments of the electric field
16 configurations for CICE with the use of wafer chuck 640. Fig. 6C shows a setup for bulk delivery
17 of etchants with backside contact of local electrical and thermal actuators, and micromirror arrays
18 for additional thermal control that may be used in some embodiments of the present technology.
19 Fig. 6D shows a setup for bulk delivery of etchants with front side electrode needles 645,
20 backside contact of local electrical and thermal actuators, micromirror arrays for additional thermal
21 control that may be used in some embodiments of the present technology. Fig. 6E illustrates a
22 setup with a thermal chuck and embedded electrodes and thermal actuators 650 on the back of
23 the substrate.

24 **[0091]** The embodiments illustrated in Fig. 6A and 6B use inkjets 605 coupled with local
25 top electrodes 615 and backside electrode contacts 630 to provide local control of etchant
26 concentrations and electric fields. The different regions for etching can be isolated from each
27 other on the top of the wafer using polymer walls 625 that are patterned using low resolution
28 lithography. In one embodiment, the walls can be made of a different etchant resistant material
29 such as silicon nitride, aluminum oxide, amorphous carbon, silicon or chromium. In Fig. 6A, the
30 backside electrode 630 includes both electric and thermal actuators, and the electric contact is
31 made using conductive substances such as metal, silicon, silicon carbide etc. which may or may
32 not be doped to improve conductance. In Fig. 6B, the backside electric contact 630 is made using
33 an electrolyte which is locally contained between the wafer 635 and the chuck 640. The electrolyte

1 may be the same as the etchant or is a different conductive liquid such as dilute acids, bases or
2 salts which are CMOS compatible. In both Fig. 6A and 6B, the backside electrode 630 can also
3 include temperature control integrated in the electrode itself (Fig. 6A) or in the chuck (Fig. 6B).

4 **[0092]** In the embodiments illustrated in Fig. 6C, the backside electrode contact 630 and
5 the chuck 640 are similar to the configuration in Fig. 6B. The etchant, on the other hand, is
6 dispensed globally on the wafer using an inlet, and may be circulated using an outlet for flow
7 control. An optional diffuser (not shown) may be used to ensure uniform distribution of etchant
8 over the wafer. The different components of the etchant may be mixed in a separate mixing
9 chamber or dynamically mixed in by flowing through the inlet and diffuser. Electrode 615 can be
10 made of a metal mesh, doped silicon wafer, ITO (Indium Tin Oxide) or other such materials and
11 can be coated with etchant resistant material such as polymer, PTFE, aluminum oxide, and the
12 like, and the coated material can be doped to improve conductivity. Local heating can be
13 implemented on either side of the wafer, either by a micromirror array on the topside of the wafer
14 or by embedded thermal actuators in the chuck 640.

15 **[0093]** In the embodiments illustrated in Fig. 6D, the wafer 635 can face either top or bottom
16 of the setup. The chuck 640 can be used to create an electric field using an electrode and an
17 electrolyte. The electrolyte can be a very thin film, thereby enabling local temperature control via
18 embedded actuators in chuck 640. Alternatively, micromirrors can be used. An optional diffuser
19 (not shown in Fig. 6D) can be used for both distributing the etchant uniformly and for optical
20 metrology using embedded optical fibers. Local electric field control can be created via sharp
21 electrode tips 645 or by embedded electrodes in the chuck 640.

22 **[0094]** Fig. 6E shows an embodiment where the wafer 635 faces the base of the setup.
23 The base comprises an electrode and an etchant at low temperatures. The wafer can be held
24 upside down using a head chuck that comprises electrical and thermal actuators. A thin film of
25 electrolyte may also be present in the head chuck for better electrical contact. The wafer can be
26 spun using the head chuck, and an overflow chamber can be used for transport of excess etchant
27 while spinning the wafer. An optional diffuser (not shown in figure) can be used in the base to
28 enable uniform distribution of the etchant. The diffuser can also include optic cables for metrology.

29 **[0095]** CICE can be performed using various methods of etchant delivery in conjunction
30 with catalysts and electric, magnetic, temperature actuators, and the like for different applications,
31 such as: electrochemical etching, electroless chemical etching, catalyst influenced vapor etching,
32 catalyst influenced plasma etching, "digital" layer electrochemical/electroless chemical etching
33 (e.g., alternately pulse H_2O_2 vapor and HF vapor, alternately pulse H_2O_2 liquid and HF liquid,

1 alternately pulse H_2O_2 vapor and HF liquid, alternately pulse H_2O_2 vapor and HF liquid, H_2O_2 ,
2 Plasma and fluoride ion flow/pressure alternated for alternating porosities, using stronger oxidant
3 for porous layers and weaker oxidant for non-porous layers, etc.), magnetic field
4 electrochemical/electroless chemical etching, gel-based etching (e.g., by adding a thick polymeric
5 substance and bringing into local contact on top/bottom of wafer for local thermal control and
6 electric field control or changing gel consistency with temperature), and the like.

7 **[0096]** In some embodiments, prior to the CICE process, the wetting properties of the
8 etchant chemicals on the catalyst patterned substrate can be modified to make it more
9 hydrophobic or hydrophilic. This helps improve the uniformity of the etch process by ensuring
10 that the initiation of the etch starts in all locations of the substrate at the same time. Exposing the
11 substrate to vapor HF, Piranha (sulfuric acid and hydrogen peroxide in different ratios), buffered
12 oxide etch, hydrofluoric acid, etc.; rinsing it with DI water, isopropyl alcohol, acetone, etc., and
13 then drying it to prevent water stains can improve wetting of the etchant on the substrate.

14 **[0097]** After the CICE process is completed, the substrate can be rinsed in DI water,
15 isopropyl alcohol, acetone, etc. to ensure that the etchant is completely removed from the
16 substrate, thereby avoiding any extraneous etching locally. A rinsing station can be the same as
17 the process chamber, where the wafer is flushed with DI water after removal of the etchant. It
18 can also comprise a spinning system to dry the wafer after rinsing. Alternatively, the wafer can
19 be moved to a separate rinsing and drying station after the CICE process using automated
20 handling.

21 **[0098]** Fig. 7A illustrates the cross-section of an embodiment of MSP-CICE process
22 chamber 700 with automated handling using a Z-motion actuator 710. The Z-motion actuator
23 may comprise voice coils in the head assembly, bearings 715 in the base assembly, and a
24 compliance in the actuator system to ensure creation of a good seal to prevent leaks using
25 sensors for leak checks 720. This Z-motion actuator is used to lower the head assembly 725
26 towards the base assembly 730. The Z-motion actuator may be controlled using motion sensors,
27 force sensors, or a combination thereof to ensure the head assembly, the wafer, and the base
28 assembly can be assembled to form the appropriate seals required for the electrolyte in the head
29 assembly and the etchant in the base assembly. In this embodiment, the Si wafer substrate 735
30 faces the base.

31 **[0099]** The base comprises a base electrode 740, power supply 745 to the base electrode,
32 sealing rings 750 which could be an O-ring (circular cross-section polymeric ring) or a rectangular
33 cross-section ring made of etchant resistant materials such as fluoropolymer, Al_2O_3 , SiC, Teflon-

1 coated material etc. that are used to seal the etchant from the electrode and the Si wafer. The
2 base also comprises inlets 755 and outlets 760 for etchant flow and circulation, and a diffuser 765
3 that may comprise optic fibers for optical sensing of the etch process in-situ. The base may also
4 comprise an overflow chamber (not depicted in figure) to ensure the etchant is filled to the brim
5 before loading of the Si wafer. The head assembly comprises pin chuck zones 770, electrolyte
6 zones 785 and power supply 795. The pin chuck zones are connected to one or more vacuum
7 ports 775.

8 **[00100]** Thermal actuators 780 can be embedded behind the pin chuck zones. An
9 embodiment that uses thermal actuators comprising proportional-integral controlled
10 thermoelectric heating/cooling elements such as thermistors and heat sinks is incorporated herein
11 by reference. (Ajay, P. et al., 2016. Multifield sub-5 nm overlay in imprint lithography.
12 *Journal of vacuum science and technology. B, Nanotechnology & microelectronics:*
13 *materials, processing, measurement, & phenomena: JVST B*, 34(6), p.061605.) An
14 electrolyte port 790 for both inlet and outlet is used to pump in electrolyte into one or more
15 electrolyte zones and seal it during the etch. This can enable a configuration where the head
16 assembly along with the Si wafer can spin while the base remains stationary. The electrolyte may
17 be different from the etchant, such as dilute acids, bases and salts with sufficient conductivity to
18 create an electric field across the Si wafer with the base electrode. An exemplar electrolyte
19 comprises dilute sulphuric acid.

20 **[00101]** Fig. 7B shows a cross-sectional view and a top view of an embodiment of the head
21 chuck. The pin chuck zones 770 are used to hold the Si wafer 735, and the electrolyte zones 785
22 are used to create contact between the Si wafer and the electrolyte. A liquid electrolyte is used
23 in this embodiment to create reliable ohmic contacts with the Si wafer. In other embodiments,
24 metal or SiC pads may be used instead of liquid electrolytes in the “electrolyte zones”. The pin
25 chuck and electrolyte zones are separated from one other using sealing elements 771 machined
26 into the chuck. Local electric field boundaries at the edges of the electrolyte zones are discrete at
27 the back of the Si wafer. However, due to the thickness of the Si wafer and its electronic properties,
28 the electric fields lines between different electrolyte zones may merge at the front of the Si wafer.

29 **[00102]** Electromagnetic simulations can be done to determine optimal placement of
30 electrolyte zones and pin chuck zones for effective local and global electric field control and edge
31 uniformity. In one embodiment, the sealing elements are 1mm wide and the pin chuck and
32 electrolyte zones are concentric, with a width of 9mm each, ending with a circular region in the
33 middle as shown in Fig. 7B. Vacuum ports 775 may use pneumatic elements to ensure that the

pin chuck zones are under vacuum, and the wafer is held against the pins 772. Electrolyte flow ports 790 are used to flow in electrolyte after the Si wafer is held by the chuck. Discrete thermal actuators 780 can be integrated behind the pin chuck regions of the Si wafer to facilitate local temperature control. In one embodiment, the head assembly comprises pin chuck elements made with aluminum oxide material.

[00103] In Fig. 7, automated handling can be achieved by starting with a separation between the head and base. The base is stationary and is filled to the brim with etchant, and this can be ensured by using an overflow chamber and etchant level monitors. The etchant in the base can be recirculated using the inlet and outlet valves. A robotic arm is used to load the Si wafer onto the head chuck with the surface to be etched facing the base. In one embodiment, the robotic arm contacts the front of Si wafer at the edge (only in the exclusion zone which is ~1-2mm zone at the edge of the wafer, where there are no functional devices fabricated) and aligns the back of the wafer to the outer sealing ring of the head chuck, which then holds the Si wafer using vacuum in the pin chuck zones. In an alternate embodiment, the head chuck may include “fingers” around the edge of the wafer that protrude out and hold onto the edge of the wafer after the robotic arm holding the wafer facing the base brings the wafer underneath the head chuck. The fingers hold onto the edge of the wafer and then pull the wafer towards the pins in the head chuck. The vacuum zones then hold onto the wafer, which can be detected using vacuum sensors in the chuck vacuum lines. The fingers then retract into the head away from the edge of the wafer.

[00104] Once a seal is created, electrolyte is pumped into the one or more electrolyte zones. This portion may be thin to ensure low volumes of electrolyte need to be pumped in. The head assembly along with the Si wafer is then lowered using a Z-motion actuator towards the base. To ensure smooth contact with the etchant in the base and to minimize bubble formation at the etchant-wafer interface, the head assembly is tilted slightly as it is lowered using elements in the z-motion actuator such as voice coils. Once it makes contact with the etchant at one end, the head assembly is tilted back to a horizontal configuration. This ensures that there is no trapping of air bubbles at the interface of the wafer and the base. An optional bearing in the base then clamps the assemblies together and uses force sensors to check whether an adequate seal has been created between the base and the Si wafer.

[00105] Alternatively, any excess etchant may flow into the overflow chamber near the edge of the wafer. Sensors for leak tests then ensure that the wafer is ready to be processed. CICE may be performed by starting an electric field across the wafer. In processes requiring an oxidant such as H_2O_2 , the oxidant may be pumped into the etchant at the base after the wafer is clamped

1 to make sure that any initial contact does not prematurely start the etch. In an alternate
2 embodiment, the volume of the etchant in the base is slightly less than the amount required to
3 contact the front of the Si wafer. Once the head assembly has completed its z-motion towards
4 the base, a small amount of etchant is added to the base chamber to bring the etchant into contact
5 with the Si wafer. To prevent air bubbles from affecting the etch, the head may be tilted slightly
6 to let the air bubbles escape and then brought back to horizontal position, thereby creating a
7 uniform etchant-wafer interface for CICE.

8 **[00106]** Unloading of the wafer after the CICE process in Fig. 7 may also be handled in an
9 automated fashion. Once the CICE process is completed, the head assembly including the wafer
10 is separated from the base. The etched side of the wafer is then rinsed to remove any etchant
11 on the surface. This can be done by spinning the head and spraying DI water, wherein a rinsing
12 system is moved into the area below the head and above the base. The rinsing system comprises
13 a drain, a spray for DI water and a source for heated air or nitrogen gas to dry the etched surface.
14 Once the front surface of the Si wafer is clean, the electrolyte in the head is drained and the wafer
15 is placed face down on an edge contact on the rinsing station. The back of the wafer is then
16 rinsed and dried in a similar fashion. A robotic arm then unloads the Si wafer and the rinsing
17 system is moved away from the middle of the head and base. In an alternate embodiment, the
18 head may move laterally and place the Si wafer on a separate rinsing station.

19 **[00107]** Wafer-scale etching of semiconductor bulk or superlattice nanostructures using
20 CICE can use monitoring and control of various parameters such as the etch depth variation,
21 porosity of the alternating layers, stability of the high aspect ratio nanostructures, anisotropy of
22 the etch, wafer edge effects, electric field uniformity, illumination uniformity, etc. This can enable
23 monitoring of etch parameters layer by layer during SiSE. This can use local control of pattern
24 geometries and a measurement of electric current and voltage across the stack to determine
25 number of layers etched etc. to high levels of precision over the entire wafer.

26 **[00108]** Additionally, the areas of the wafer that are used for peripheral circuitry and non-3D
27 NAND array circuits must be protected from the SiSE process. This can be done by masking the
28 non-array areas. Etch variation near the edges of these features can be regulated using actuators.

29 **[00109]** The flow of etchants through a sub-40nm hole as it etches to depths >10 microns
30 (A.R >250) is enabled by electric fields and by creation of alternating porous layers. The porous
31 layers enhance lateral etchant flow and regulate the etch uniformity. Another way to boost etchant
32 flow, in accordance with various embodiments, is by using a connected link pattern to connect
33 the holes.

1 **[00110]** The etch rate may decrease due to slower diffusion of etchants as the etch
2 progresses due to increase in aspect ratio. Such changes can be detected through a change in
3 the electrical properties across the stack, as each etched layer of the superlattice can result in a
4 step change in the electrical property such as current or voltage across the electrodes or the
5 resistance of the stack. To prevent this decrease in diffusion, some embodiments utilize the
6 alternating porous layers to ensure that there are multiple pathways for the etchant to reach the
7 etch front, i.e., the catalyst location. Spinning the substrate during the CICE process can be done
8 in some embodiments at optimized speeds to improve uniformity of the etchant concentrations
9 from the center of the wafer to the edge.

10 **[00111]** Wandering of the catalyst is primarily due to an imbalance in the concentration of
11 holes underneath the catalyst. To prevent wandering of the catalyst and to ensure vertical
12 anisotropy of the etch, an electric field can be applied to direct the diffusion of holes towards the
13 bottom of the wafer. The electric field required changes as SiSE progresses due to a change in
14 the resistivity across the electrodes with change in the number of alternating doped layers to be
15 etched. By using a current control power supply circuit, the changes in voltage can be
16 compensated for.

17 **[00112]** Various embodiments of the SiSE tool system enable multi-scale precision control
18 of the SiSE process based on real-time metrology, and based on an array of independently
19 addressable actuators that can locally control the etch process to allow controlled fabrication of
20 devices with diverse geometries and multilayers. Parameters like the resistivity and doping of the
21 substrate material, geometry and aspect ratio required, the etchant ratios, electric-field,
22 temperature and illumination of the process chamber can be modified to control etch. Once the
23 SiSE process is complete as detected by inline metrology, the solution in the machine has to be
24 flushed out and replaced with a wet etchant for the catalyst. Next, since the high aspect ratio
25 nanostructures can collapse due to capillary forces as the device is being dried, use of efficient
26 and highly controlled fluid exchange coupled with advanced drying techniques and novel mesh
27 architectures and/or ceilings to prevent pattern collapse is described.

28 **[00113]** Inline electrical metrology and electrochemical etch stops may be used in various
29 embodiments. For example, an electric bias when applied to a semiconductor substrate can
30 control the etching profile in real-time. Excessive etching due to migration of excess holes
31 generated below the catalyst can be controlled by an external electric field. A negative bias on
32 the backside of the wafer will attract the excess holes and prevent unwanted pores in the Si. A
33 wide range of current, bias and polarity settings including high speed pulse and periodic reverse

1 waveforms will control the electric field across the wafer in real-time. Electric field parameters
2 such as current, voltage, resistance, capacitance, waveform frequency, duty cycle, amplitude,
3 distance between electrodes etc. are used both to detect changes in the etch state as well as
4 control the porosities of the alternating layers while preventing wandering of the catalysts.

5 **[00114]** Measurement of the current and voltage across the substrate as the etch progresses
6 can be used to determine the number of alternating layers etched in the 3D NAND Flash process.
7 Also, the exact time at which the morphology changes can be detected by measuring electrical
8 parameters such as resistance, voltage, current, capacitance etc. across the epitaxial layers. This
9 information can then be used to precisely modulate the current across the stack.

10 **[00115]** Electric fields can be used for various functions during the CICE process such as
11 for making alternating porous/non-porous layers, preventing wandering of the catalyst during etch,
12 maintaining uniformity across the wafer and detecting etch depth variations in a die, die-to-die
13 variations, and center-to-edge variations. Applying electric fields across the substrate, both
14 locally and globally, requires designing the tool and process to ensure compatibility with different
15 CMOS processing equipment and constraints such as front and back contact, edge width contact,
16 electric back contact materials etc. Some embodiments of this design are shown in Figs. 6A-6E.

17 **[00116]** To perform multiple functions, more than one electric field can be applied across the
18 wafer, such as: 1) DC voltage across the wafer to prevent wandering of the catalyst; 2) alternating
19 electric fields with a certain waveform, frequency, wavelength and duty cycle to create alternating
20 porous/non-porous layers; 3) detection of local variations of etch from center to edge via pulsed
21 electric fields at frequencies and voltages that do not affect the porosity of the substrate being
22 etched; and/or 4) etch depth monitoring by measurement of current, voltage, resistance,
23 capacitance etc. in each local electrode.

24 **[00117]** Apart from Electric Fields, temperature can also influence the CICE etch rates. For
25 instance, it has been demonstrated in literature that the etch rates of CICE depend on the
26 temperature of the etchant, and drop off exponentially near 0°C. (Ref: Backes, A. et al., 2016.
27 Temperature Dependent Pore Formation in Metal Assisted Chemical Etching of Silicon. *ECS*
28 *Journal of Solid State Science and Technology*, 5(12), pp. 653–P656 is hereby incorporated by
29 reference in its entirety for all purposes.) Various embodiments take advantage of this property
30 by locally controlling the etch temperature by maintaining the global etchant temperature near
31 zero degrees using coolants such as liquid nitrogen and dry ice, and locally modifying the
32 temperature of the substrate. This can be done using thermal chucks, micromirrors or electrodes
33 near the wafer that can locally heat the solution. Alternatively, etchant temperatures can be

1 controlled locally by using individual wells for each die which are filled with finite and temperature
2 controlled etchant volume and are pumped out or circulated. In some embodiments, the
3 temperature can be mapped with precision across the wafer using thermal cameras,
4 thermocouples, and the like.

5 **[00118]** An optical imaging system will be used to measure the reflectance over large sample
6 areas in real-time. The samples will be illuminated with light with known spectral content. The
7 light can be white light, colored light, single wavelength, in a narrow or wide spectral band, etc. A
8 camera can then image the samples reflecting this light. The camera may be monochrome, color
9 (RGB), multi-spectral, hyperspectral, etc. Multi-megapixel resolutions found in modern cameras
10 make it possible to observe millions of points on a sample simultaneously. Video framerates
11 enable in-situ real-time measurement. Each image can be divided by an image of a reference to
12 calculate reflectance images of the samples or used as they are. An image processing algorithm
13 will determine process completion and gather data about uniformity of MSP-CICE both within
14 samples and sample to sample. In an embodiment where CICE is used to create Si nanowires
15 (NWs), the optical properties of Si NWs of variable geometries lead to a wide spectrum of colors
16 under white light illumination. In our preliminary experiments with CICE, samples exhibit profound
17 changes in hue during the CICE etch. Since the pitch and diameter of the nanowires remain
18 relatively fixed, observing changes in the hue of samples is a useful indicator of the height of the
19 nanowires, and thus the etch depth. Changes in hue can be characterized by measuring the
20 reflectance of the sample as a function of the spectral content of the light being.

21 **[00119]** The spectral properties of the alternating layers can also be used to enable detection
22 of number of layers and porosity during the etch process. Infrared (IR) spectroscopy can be used
23 to determine the etch layers in-situ, using metrology similar to that used to characterize Bragg
24 reflectors and Rugate filters in literature. In one embodiment, optic cables in a diffuser plate in
25 the etch chamber can be used to incorporate such metrology elements.

26 **[00120]** Visible wavelengths of light from the backside of the wafer cannot detect the etch
27 depth during CICE. Infrared (IR) spectroscopy can be used instead, as is it a rapid, non-
28 destructive and in-situ method of etch state detection. Silicon is transparent in IR wavelengths,
29 while a catalyst such as Pt or Pd is not. This differentiation can be used to determine both the
30 etch rate and the etch depth at any particular instance of the CICE process.

31 **[00121]** The concentration of the etchant can be measured using a variety of techniques.
32 For example, in some embodiments, a conductivity measurement may be used since the HF has
33 a linear dependence between concentration and conductivity. In some embodiments, a refractive

1 index measurement may be used. For example, an optical metrology system can be used to
2 measure the refractive index (RI) via a reflection-type geometry using an optical window in contact
3 with the solution, thus avoiding turbidity, diffraction and absorption.

4 **[00122]** To ensure etchant concentration uniformity across the wafer, the wafer can be spun
5 using a wafer chuck, wherein local electric fields can be provided by connecting the spinning
6 arrays of local electrodes on the chuck to a stationary patterned conductor disc. The local
7 electrodes can be connected to the stationary patterned conductor disc using slip rings.
8 Compatibility with the etchant chemicals can be ensured by using Teflon coating.

9 **[00123]** In some embodiments, a “send-ahead” wafer can be used to optimize the etch, and
10 the send-ahead wafer can be inspected using various in-situ (online) and ex-situ (offline) methods.
11 Offline metrology comprises of various destructive and non-destructive inspection methods such
12 as scatterometry, ellipsometry, optical feature size measurement, laser scanning, Scanning
13 Electron Microscopy (SEM), Atomic Force Microscopy (AFM), Transmission electron microscopy
14 (TEM), x-ray diffraction (XRD), etc. The data collected is then analyzed using image processing
15 algorithms to determine sources of defects and process excursions.

16 **[00124]** Magnetic fields, pressure variations, electromagnetic fields, solvents to improve
17 uniformity and prevent sticking of bubbles, spinning of the wafer, edge effects, spraying of
18 etchants, atomizing etchants can also be included in some embodiments of the CICE tool as
19 necessary.

20 **Overall tool designs and control schemes**

21 **[00125]** Some embodiments provide for a wafer-scale system for high aspect ratio etching
22 of semiconductor substrates. The multi-scale precision (MSP) CICE system used in some
23 embodiments can have a modular architecture to allow for installation of sensors and actuators
24 such as a large array electrodes and real-time optical imaging systems. Figs. 8A-8C illustrate
25 and example of an MSP-CICE tool setup, an example of a detailed process chamber layout, and
26 an example of a process flow that may be used in one or more embodiments. Nonlinear optimal
27 process control schemes can be used in some embodiments to achieve controlled wafer scale
28 nano-manufacturing based on large array of independently controlled electrodes.

29 **[00126]** Fig. 8A shows a cross-sectional view of a complete etching tool, with automated
30 substrate, electrode and etch cell loading. Fig. 8B shows a detailed cross-sectional view of some
31 embodiments of the process chamber 815. As illustrated in Fig. 8B, the etching tool can include
32 loading dock 805, robotic arm 810, process chamber 815, top electrode 820, tunable light source

1 825, wafer chuck 830, wafer chuck holder 835, stirrer 840, power supply 845, sensors 850, drain
2 pipe 855, optical metrology system 860, high resolution camera 865, bottom electrode 870,
3 circulation setup 880, exhaust 885, and inlet flow 890. In the embodiments illustrated, process
4 chamber 815 can include robotic arm 810 that places a wafer on wafer chuck 830. Wafer chuck
5 830 can sit upon wafer chuck holder 835. The wafer chuck holder and the wafer chuck assembly
6 separate the electrolytes in contact with the bottom electrode 870 and the top electrode 820. This
7 ensures that the electric field is applied across the wafer. Process chamber 815 can also include
8 in-line optical metrology system 860 which can include high resolution camera 865 and tunable
9 light source 825. Process chamber 815, in accordance with various embodiments, can also
10 include an etching flow system with an inlet flow 890, drain pipe 855, and circulation setup 880
11 for both the bottom electrolyte and the top electrolyte/etchant. The etching flow system may also
12 include stirrer 840 (e.g., a magnetic stirrer). An electric field can be applied across the wafer
13 using first electrode 820 and second electrode 870 with power supply 845. The inline metrology
14 can be done using embedded sensors 850 (e.g., temperature, electric field properties, fluid
15 concentration properties, etc.). Exhaust 885 can be used to dispense of fumes. Processor 890
16 can use one or more algorithms to control the processing.

17 **[00127]** In the embodiments illustrated in Figs. 8A-8B, a wafer with a patterned catalyst will
18 be loaded into the loading dock 805. A robotic arm 810 can be used to transfer the wafer into the
19 process chamber 815. The transparent top electrode 820 can then be placed on the rails above
20 the wafer holder. When the processing is complete, the top electrode array 820 can be removed
21 and the wafer will be unloaded back to the loading dock 805. A key challenge in building this tool
22 is that all the elements of the system be HF (Hydrofluoric Acid)-compatible. Various embodiments
23 propose to do this by coating all equipment that comes in contact with HF with polymers such as
24 Teflon PTFE, Epoxy, TPX (or PMP), polypropylene(PP) and PVDF, which are compatible with
25 H₂O₂ as well. TPX and epoxy are transparent and easy to process.

26 **[00128]** Based on the requirements of the application, the wafer chuck can be a Bernoulli
27 chuck with no backside contact with the wafer, or have O-rings to contain the wet etchant to the
28 front of the wafer. Flow valves and actuators can be used to control relative ratios of the etchant
29 components (such as HF, H₂O₂, Ethanol, Isopropyl alcohol and DI water) in the chamber. The
30 etchant can be dispensed locally by inkjets or over the whole wafer by flow valves. After etch and
31 catalyst mesh removal, the etchants will be flushed with DI water, and may be replaced with low
32 surface tension liquids. A drain valve will safely dispose of the fluids or store them for use in a
33 subsequent etch.

1 **[00129]** Fig. 8C depicts an example of various processes that the wafer goes through in the
2 etch tool. The wafer can be loaded into the tool using a loading dock 812 which can comprise of
3 the FOUP (Front Opening Universal Pod) of wafers. A robotic arm (or other transport mechanism)
4 can transport the wafer from the loading dock 805 to the process chamber 815. The process
5 chamber 815 may comprise of one or more chambers for pre-processing 816, etching 818, post-
6 processing 828 and rinsing steps 830.

7 **[00130]** The pre-processing step 816 may be a lift-off process or a surface modification step
8 such as dispensing of piranha (sulphuric acid and hydrogen peroxide), vapor HF, diluted HF,
9 Buffered Oxide Etch, Ethanol, Acetone, Isopropyl Alcohol, DI water. The pre-processing step
10 may also be via plasma activation using oxidizing plasmas such as oxygen, carbon dioxide
11 plasma, or hydrogenating plasmas such as hydrogen, ammonia plasma. A helium or argon
12 plasma can also be used.

13 **[00131]** The etch process 818 can be then done on the wafer, with sensors and actuators
14 for in-situ monitoring and control, such as:

- 15 • Flow control 824 can include etchant concentration measurement. In accordance with
16 various embodiments, the concentration of the etchant will be measured using two
17 techniques: a) Conductivity measurement - HF has a linear dependence between
18 concentration and conductivity. b) Refractive Index measurement - An optical metrology
19 system will measure the Refractive Index (RI) via a reflection-type geometry using an
20 optical window in contact with the solution, thus avoiding turbidity, diffraction and
21 absorption.
- 22 • Local temperature control 822: The etch rate is dependent on the local temperature and
23 mesh profile. Using a temperature actuator wafer chuck, various embodiments can control
24 the local temperature variations for process control.
- 25 • Process chamber environment control (not illustrated in Fig. 8C): The tool will be enclosed
26 and have inert gas flow. Pressure and global temperature will be monitored and controlled.
27 A computer interface will promote operator safety and will be used to monitor the etch
28 using image processing, and to control temperature and electric fields.
- 29 • Electric field 826: An electric bias when applied to a semiconductor substrate can control
30 the etching profile in real-time. Excessive etching due to migration of excess holes
31 generated below the catalyst can be controlled by an external electric field. A negative
32 bias on the backside of the wafer will attract the excess holes and prevent unwanted pores

1 in the Si. Although etch rates decrease with increase in electric bias, higher temperatures
2 can be used to keep them high enough for high throughput. Since MSP-CICE will be used
3 for varying pattern densities and shapes on different areas of the wafer, an electrode array
4 will be used to locally control and attenuate the electric field above different patterns to
5 ensure uniformity in etch. A wide range of current, bias and polarity settings including high
6 speed pulse and periodic reverse waveforms will control the electric field across the wafer
7 in real-time. A transparent top electrode such as ITO film on a glass or sapphire wafer, a
8 doped Si wafer (transparent to IR), a platinum mesh or optic fibers can be used above or
9 below the wafer to allow for optical measurements. The bottom electrode can be an array
10 for local control, and a modular design will be chosen to allow easy installation and
11 investigation of various bottom electrode arrays. The top and bottom electrodes and
12 electrolytes are isolated from each other using the wafer chuck and wafer chuck holder
13 assembly. Cross-talk will be minimized using simulations. Measurement of the current
14 and voltage across the substrate as the etch progresses can be used to determine the
15 number of alternating layers etched in the 3D NAND Flash process or as an etch stop
16 indicator for nanostructure etching, for example if the substrate has a buried epi layer.

- 17 • Inline optical metrology 820: An optical imaging system comprising RGB cameras, optical
18 fibers, spectral imaging setups, will be used to measure the reflectance over large sample
19 areas in real-time. An image processing algorithm will determine process completion and
20 gather data about uniformity of MSP-CICE both within samples and sample to sample.

21 **[00132]** Post-processing 828 may include etching of the catalyst metal and rinsing and
22 drying of the substrate. In order to prevent collapse of high aspect ratio etched nanostructures,
23 fluid transfer can be used to enable a surface tension gradient (Marangoni-effect), low surface
24 tension fluid transfer or preparation of the wafer for transfer into a critical point drying tool.

25 **[00133]** In one embodiment, based on the resistivity and doping of the silicon, and the
26 geometry and aspect ratio required, the etchant ratios can be tuned to get the desired results.
27 Factors such as electric-field, temperature and illumination of the process chamber can also be
28 modified to control etch. Once the CICE process is complete as detected by inline metrology, the
29 solution in the machine has to be flushed out and replaced with a wet etchant for the catalyst.
30 Next, since the high aspect ratio nanowires can collapse due to capillary forces as the device is
31 being dried, use of efficient and highly controlled fluid exchange coupled with advanced drying
32 techniques and novel mesh architectures and/or ceilings to prevent pattern collapse is used.

1 **[00134]** Once the MSP-CICE system has been designed and fabricated (including the optical
2 imaging system and electrical parameter measurements), it is necessary to develop optimal
3 control techniques to operate the MSP-CICE system to fabricate wafer-scale device-specific VA-
4 NSs. As discussed earlier, it is important to have the ability to monitor the etch progression over
5 different layers of the 3D NAND Flash stack or the shaped nanowires for DRAM. This requires
6 local control of pattern geometries and a measurement of electric current and voltage across the
7 stack to determine number of layers etched etc. to high levels of precision over the entire wafer.

8 **[00135]** A key challenge is that the forward model of the full system – that provides a
9 relationship between control variables and sensed output over the full wafer – is expected to be
10 highly nonlinear making it difficult to obtain comprehensive experimentally validated models due
11 to the complexity of the MSP-CICE system. However, certain aspects of the process can be
12 modeled through established physical models. For example, the control variables, in various
13 embodiments, can include temperature, chemical composition, and electric field, in which the
14 variation of chemical composition can be analytically modeled with the help of equations
15 governing transport. Electric field and temperature control could be distributed over a large array
16 of actuators—consisting of as high as hundreds to thousands of actuators – providing local control
17 over the etching process, and their distribution can also be modeled through physical models.

18 **[00136]** However, models establishing their influence on the etching process is less clear.
19 The optical imaging system is expected to provide spectral information with spatial resolution of
20 as high as 1mm^2 or higher and wavelength resolution of as high as 1nm or better. The optical,
21 thermal and electrical outputs of the system provide a large volume of sensed information which
22 can be used to automatically control the system's process using the control variables mentioned
23 previously. Automatic process control for the MSP-CICE system can be divided into two distinct
24 categories: (i) offline optimization and tuning of process parameters to obtain a targeted output,
25 and (ii) real-time adjustment of process parameters to minimize defects and maximize yield. The
26 latter relies on a process that is well-established and provides large volume of data, and the former
27 relies on optimizing for process parameters in the absence of a large amount of data. In the next
28 paragraph, a scheme is described which enables the optimization of process parameters for
29 establishing a baseline process for a given pattern geometry with the help of in-situ and offline
30 measurements.

31 **[00137]** Fig. 9 illustrates a learning algorithm-based controller 900 which can be used to
32 perform the first category of automatic process control in the absence of large amounts of data,
33 i.e., determining optimum process parameters for a targeted output with the help of learning

1 algorithms that include evolutionary algorithms such as genetic algorithm, neural networks, etc.
2 This scheme relies on both, in-situ electrical and optical feedback, as well as offline
3 measurements such as ellipsometry, CD-SEM, etc. on send-ahead wafers. Because of the
4 presence of this offline component, the cycle time for each experiment with a send-ahead wafer
5 may be too high, thereby requiring that the number of experiments be low or each send-ahead
6 wafer representing a combinatorial set, rather than an individual experiment. This embodiment
7 is further described in the context of genetic algorithms. The first step 910 of the scheme is to
8 define the targeted output and the corresponding objective function for the optimization. Then, an
9 initial "population" 920 is generated. Genetic algorithms rely on the interactions between
10 individuals in a population, where each individual is a set of the control variables or model
11 parameters 925. In one embodiment, each population may be a design of experiments and
12 confined to a single wafer.

13 **[00138]** For example, if each wafer consists of 10x10 sq. mm zones that can provide
14 electrical and optical feedback, there can be O(700) such zones on each wafer, thereby providing
15 a population size of as high as 700 in each experiment. In another embodiment, the population
16 size may be kept to a lower number, such as 20, with each individual experiment having 35 copies
17 on the full wafer. Then, this population is used to perform the CICE process 930. Sensors are
18 then used to extract information about the substrate before, during and after CICE as shown in
19 step 940. The sensed information for this scheme can include the output of both inline metrology
20 sensors such as the imaging system as well as offline measurements (e.g., CD-SEM, optical,
21 electrical, etc.) on the wafer (945). The sensed information is then fitted against the desired output
22 or objective function, 950.

23 **[00139]** The desired output parameters include the spectral signature of the etched
24 structures, electrical parameters such as resistance and capacitance across the wafer during the
25 etch process, CD-SEM and optical images of one or more portions of the wafer, etc. Based on
26 the objective function calculated using the sensed information, a new batch of control variables is
27 generated, using population interaction parameters (965). CICE is then performed using the new
28 batch and the result is evaluated using sensors. If the sensed information is within the limits of
29 the desired result, then the tuning of control variables is completed. If not, then the control
30 variables optimization process is repeated till a final number of wafers may be reached (960). In
31 one embodiment, the genetic algorithm controller is purposely designed to get close to the desired
32 optimum process parameters for an actual process run, with the final achievement of desired

1 process performance being taken over by a real-time in-situ process control scheme 935,
2 described next.

3 **[00140]** The second category of automatic process control relies on data analytics for real-
4 time adjustment of process parameters to achieve the desired process performance. Current
5 advanced manufacturing factories, such as semiconductor manufacturing, heavily rely on these
6 concepts to maximize manufacturing yield with high levels of automation. Several concepts exist
7 in this category of automatic process control, ranging from run-to-run control to predictive
8 maintenance. The key concept underpinning this scheme is the use of a high volume of sensory
9 information, such as the in-situ optical output, to run real-time analytics based on heuristics (e.g.,
10 neural networks to determine the mapping between the control and sensed variables), statistics
11 (e.g. statistical process control), as well as any physical or heuristic model to arrive at optimum
12 process parameters. An example of a situation that benefits from such models is the ability to
13 accurately predict a time delay between a change in the control variable to a corresponding
14 change in the sensed output. Moreover, such techniques can also be used to construct a virtual
15 MSP-CICE tool, i.e., a constantly adapting simulation of the actual tool that can be a proxy for a
16 physical forward model, and which can be used for offline process tuning as per the first category.
17 Such virtual tool models be tool-specific and specific to the lithographic pattern being etched, and
18 they may vary from one tool to another even though they are of the same design as tolerances in
19 manufacturing in electrical and thermal controllers etc. can cause distinct process signatures in
20 different tools.

21 **[00141]** Various embodiments of the CICE system may support various substrates, such as,
22 but not limited to Si, Ge, $\text{Si}_x\text{Ge}_{1-x}$, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. as well as
23 multilayers of semiconductors. In addition, various catalyst such as, but not limited to, Ag, Au,
24 Pd, Pt, Cu, Ni, Ti, Al, W, TiN, TaN, RuO_2 , IrO_2 , Graphene, and the like may be used. Some
25 embodiments of the MSP-CICE system may use various patterning techniques, such as, but not
26 limited to plasma etching, chemical vapor etching, electrodeposition (selective), and the like.
27 Removal techniques that may be used in some embodiments include, but are not limited to
28 chemical vapor etching, electrolytic etching, and/or wet chemical etching. Some embodiments
29 may use various etchants (e.g., HF, H_2SO_4 , HCl, H_2O , etc.), oxidants (e.g., H_2O_2 , V_2O_5 , KMnO_4 ,
30 O_2 , HNO_3 , electric fields etc.), solvents, additions (e.g., H_2O , Ethanol, IPA, DMSO, polymers (PVA,
31 PLA etc.), H_2SO_4 , etc.), etchant states (e.g., liquid, vapor, solid-gel, plasma), and/or catalyst
32 assisted etch processes (e.g., electrochemical etching, electroless chemical etching, vapor
33 etching, plasma etching, "digital" layer electrochemical/electroless chemical etching, magnetic

1 field electrochemical/electroless chemical etching, gel-based etching). In addition, various local
2 and global etch monitoring techniques may be used. Examples include, but are not limited to
3 electric field (e.g., current, voltage, capacitance, inductance, impedance, conductance, etc.),
4 optical metrology (e.g., using a camera, spectrophotometer, image processing, etc.),
5 concentration measurements (e.g., refractive index, conductance of solution), pressure (e.g.,
6 vapor pressure), temperature (e.g., using thermocouples, IR camera, etc.). Some embodiments
7 may use local and/or global etch control based on electric fields (e.g., current, voltage, waveforms,
8 wavelength, frequency, duty cycles, pulsed electric fields, etc.), optical metrology (e.g.,
9 illumination), concentration (e.g., etchant concentrations, mixing and diffusion), and/or
10 temperature (e.g. using thermal chucks, micromirrors, etc.). Various embodiments of the setup
11 can etch industry standard wafers or wafers that can go through standard CMOS processes. A
12 such some embodiments may be compatible with the etchant. Some embodiments may also
13 provide for automated handling of all substrates and etch components and chemicals.

14 **[00142]** In one embodiment, the etchant can be in the form of vapor. The apparatus for vapor
15 based CICE comprises: control of local temperatures using a thermal chuck, monitoring of vapor
16 pressure of each component, and/or applying an electric field in the form of a plasma. Vapors can
17 be used to facilitate “digital” layer electrochemical/electroless chemical etching by methods: 1)
18 alternately pulse H_2O_2 vapor and HF vapor, 2) alternately pulse H_2O_2 liquid and HF liquid, 3)
19 alternately pulse H_2O_2 vapor and HF liquid, 4) alternately pulse H_2O_2 vapor and HF liquid, 5) H_2O_2 ,
20 Plasma and fluoride ion flow/pressure alternated for alternating porosities, and/or 6) using
21 stronger oxidant for porous layers and weaker oxidant for non-porous layers.

23 **3D NAND Flash**

24 **[00143]** Scalability of advanced memory architectures made by current pattern transfer
25 techniques is limited by non-zero taper, sidewall damage and etch mask degradation due to high
26 aspect ratio plasma etching. Non-Volatile Memory architectures such as 3D NAND Flash need
27 extremely high aspect ratio etching of >64 layers of alternating material to increase the storage
28 capacity per unit area. With increasing layers, the cost and reliability of (1) multilayer deposition,
29 (2) anisotropic high aspect ratio channel and trench etch, and (3) staircase etch for defining
30 contacts to each layer becomes a major limiting factor for scaling. Various embodiments provide
31 for vertical 3D memory architectures and semiconductor process integrations using an anisotropic
32 and highly selective etch technique.

1 **[00144]** Various embodiments of the present technology define novel lithography patterns,
2 material stacks and process flows that incorporate various interdisciplinary technologies to get
3 improvement in memory performance and scalability. The 3D NAND Flash process flows
4 incorporate semiconducting material stacks that can enable metal or crystalline silicon gates,
5 angled staircase etch, crystalline silicon channels and low-k porous dielectrics while reducing the
6 number of lithography and high aspect ratio etch steps. In some embodiments, a wafer scale
7 Multi Scale Precision Silicon Superlattice Etching (MSP-SiSE) fabrication tool for this purpose is
8 also disclosed. The high selectivity and anisotropy of this etch technique can enable an indefinite
9 number of 3D NAND Flash layers.

10 **[00145]** The ITRS Roadmap for 3D NAND Flash predicts that the number of memory layers
11 will increase steadily from 48 layers in 2016 to 512 in 2030, at 80nm half-pitch. This requires
12 significant development in highly anisotropic ($\sim 90^\circ$) high aspect ratio etching of layers of
13 alternating material. The current plasma etching methods involve expensive and time consuming
14 alternating deposition and etch steps to ensure that this anisotropy and selectivity is maintained.
15 A non-zero plasma etch taper angle limits the maximum number of tier stacking that can be
16 reliably achieved. Also, due to a non-zero taper the channels etched by plasma etching limit the
17 number of layers that can reliably be scaled as the bottom most layer has a much smaller critical
18 dimension than the lithographically defined top layer. A workaround to overcome this limitation
19 by stacking multiple wafers with 64 memory layers each is inefficient, expensive and increases
20 the device volume. Separate lithography and etch steps are required for the circular channels
21 and the rectangular slits, as different geometries cannot be etched simultaneously and reliably
22 with plasma etching due to Aspect Ratio Dependent Etch (ARDE). Fabrication of the "staircase"
23 for contacts to individual layers requires multiple lithography and etch steps while trying to
24 preserve the etch masks. Various embodiments of the present technology aim to solve that by
25 enabling an inexpensive high aspect ratio etch with high selectivity and anisotropy that can be
26 extended to future demands of 3D NAND Flash.

27 **[00146]** Two of the most popular architectures in industry are BiCS and TCAT. Both
28 architectures use the basic concept of Stack (multilayers of plates and dielectrics), Punch (etch
29 holes in entire multilayer stack), Plug (deposit memory films and pillar electrodes in the etched
30 holes). A staircase etch is then performed to create contacts to each of the plates. BiCS uses a
31 silicon oxide/poly-Si stack, while TCAT uses a silicon oxide/silicon nitride stack where the silicon
32 nitride is later replaced with lower resistivity material for conducting lines such as Tungsten. P-
33 BiCS is a variant of BiCS with better lower source gate performance.

1 **[00147]** For both the vertical channel as well as vertical gate architectures, a new material
2 stack and process flow is suggested that can be etched using SiSE. The catalyst pattern is
3 lithographically defined such that both the circular channels and rectangular slits can be etched
4 simultaneously with high aspect ratio anisotropic etching. The material stack will be made of
5 either bulk Si or alternating layers of semiconducting material like Si, Ge with different dopant
6 types and/or doping concentrations. The CICE etch will result in layers with different etch and
7 oxidation rates for layer-selective processing. This shall enable both increase in number of layers
8 as well as a decrease in half pitch resulting in many-fold increase in storage capacity per die.
9 Also, by combining both the channel and slit lithography and high aspect ratio etch steps,
10 significant gains in cost per wafer shall be realized. An optional alkaline crystal-plane dependent
11 etch can also be done for a taper that can be converted into a staircase with a plasma etch.

12 **[00148]** Some embodiments can be used both for Charge Trap (CT) as well as Floating Gate
13 (FG) NAND Flash memories. The Lower Select Gates (LSG) can be fabricated before or after
14 the deposition of the alternating material stack. The memory material can be either CT or FG. A
15 timed etch can be used to create a recess in the oxidized porous layers for 3D FG NAND.
16 Polysilicon and core filler deposition in the channel can be done before (channel last process) or
17 after (dielectric last process) the CICE Etch. In an embodiment of the gate last approach, Si and
18 Ge layers can be etched, and Ge can be removed prior to filling with a low-k dielectric.

19 **[00149]** The final device thus is a 3D NAND Flash memory array with more than 20
20 alternating layers of conducting (or doped semiconducting) and insulating material, where the
21 vertical gate or vertical channel is extremely vertical and has an angle of $>89.5^\circ$ which is measured
22 by taking a cross-sectional image using a scanning electron microscope (SEM) and then using
23 an image analysis software such as ImageJ. The average taper angle is measured using a
24 straight line approximately conformal using a linear-fit algorithm between any difference in the
25 feature size of the top and bottom of the critical feature. The critical dimensions of the vertical
26 gate architectures can be the width of the channel or the width of the trenches between the
27 channels. For the vertical channel embodiment, the critical dimensions are the diameter of the
28 channel or the width of the trenches between blocks of memory. Since the vertical sidewall angle
29 is greater than 89.5° for CICE processes, center-to-center distance between critical features such
30 as the circular channels or rectangular slits can be sub-20nm. The dimensions of the critical
31 features can be measured using metrology techniques such as SEM, CD-SEM, transmission
32 electron microscopy (TEM) and atomic force microscopy (AFM). The arrangement of circular
33 channels can be hexagonal to create more compact 3D NAND cells.

[00150] The complete fabrication process to create 3D NAND arrays for both vertical channel and vertical gate architectures with SiSE is shown in Fig. 13. Since 3D NAND devices require alternating layers of conducting and insulating lines, the SiSE process is designed to get alternating layers of material that differ in processing parameters such as oxidation rates and etch rates to enable further processing via layer material replacement or modification. Various paths can be taken to get the alternating layers of conducting and insulating structures as described in Table 1. Paths I and II describe the initial substrates required to get superlattices. Path I uses bulk silicon wafers with no multilayer depositions, while Path II uses a stack of silicon layers with alternating doping concentrations. Paths A-G can be used in conjunction with both Path I and II, i.e. with either bulk SI or alternating layers of Si with different doping concentrations. Path A gives the option of including staircase etch by creating a taper using crystallographic or inclined etching, and the dashed lines represent some of the options where this step can be performed in the process flow. Paths B-G describe some of the methods of modifying or replacing the superlattices that are produced by the SiSE process to get final 3D NAND arrays.

Table 1: Paths I and II for 3D NAND array fabrication with SiSE, based on Fig. 13.

Paths	Initial Layers	Superlattice layers after SiSE
I, A-G	Bulk Silicon substrate	Porous Si/ Non-porous Si
II, A,C-G	p++ Si / p Si	
	n++ Si / n Si	
	n++ Si / p Si	
	p++ Si / n Si	
II, A,B	p++ Si / p Si	
	n++ Si / n Si	
	n++ Si / p Si	
	p++ Si / n Si	

[00151] The main purpose of this alternating stack etch is to get a large difference in etch or thermal processing (such as oxidation and nitridation) rates between the different layers (Layer A vs Layer B for bilayer stacks) and to use this difference to modify the stack and ultimately get insulating/conducting multilayer structures.

[00152] The porosity of the layers is a function of the etchant concentrations, the doping of the silicon substrate, and the current density across the wafer during SiSE. An embodiment of multilayers of porous and non-porous silicon made with SiSE consist of porous layers having a

1 porosity from 30% to 75%, while the non-porous layers have a porosity less than 10%. The
2 porosity is measured by cross-sectional SEM and TEM images and processed using an image
3 processing software such as ImageJ. Porosities of single layers may also be measured using gas
4 adsorption experiments such as by using the Brunauer–Emmett–Teller (BET) theory, wherein
5 CICE is performed on a bulk substrate with a patterned catalyst and exposed to a current density
6 to create a thick layer of porous silicon with porosity parameters corresponding to the porous set
7 of alternating layers.

8 **[00153]** Figs. 10A-10E illustrate catalyst mesh examples according to one or more
9 embodiments of the present technology. In Fig. 10A, isolated catalyst nanodots 1010 and
10 trenches 1020 are illustrated. In Fig. 10B, catalyst nanodots 1010 and trenches/slits 1020 can be
11 connected by lines 1030 (top figure) or by controlling the diameter and alignment of the dots and
12 trenches to ensure they are connected as illustrated in the bottom figure of Fig. 10B. In Fig. 10C,
13 staggered connected catalyst nanodots 1010 and trenches/slits 1020 are illustrated. In Fig. 10D,
14 connected links 1040 are patterned into the catalyst features for BiCS-type layout with sparse
15 word-line trenches/slits 1020 are illustrated. In Fig. 10E, connected links 1040 are patterned into
16 the catalyst features for P-BiCS-type layout with word line trenches/slits between every 2 rows of
17 channels are illustrated.

18 **[00154]** In another embodiment, features such as holes for VC 3D NAND or lines for VG 3D
19 NAND are etched in bulk silicon using plasma etching. Electrochemical etching without a catalyst
20 is then performed on the etched substrate to create alternating layers of silicon with highly porous
21 and lower porosity porous layers with a sufficient etch or thermal processing selectivity between
22 the layers. This results in a multilayer stack of high aspect ratio features, wherein one of the
23 layers may be oxidized or selectively replaced to create 3D NAND devices.

24 **[00155]** Path I – SiSE with Catalyst and Electrochemical Etching

25 **[00156]** The substrate, such as a bulk silicon wafer, is patterned with a catalyst and etched
26 with a solution containing fluoride species and (optionally) an oxidant species. During the SiSE
27 process, electric field parameters such as current density are modulated to create alternating
28 layers with different porosities. In one embodiment, the current density is modulated using a
29 square wave function with one zero and one non-zero value. This causes the “zero value” current
30 density etch to progress solely with the catalyst etch, while the non-zero value uses a combination
31 of catalyst etching as well as electric field etching to create porosity in the layers. Thus, the
32 resulting superlattice has alternating layers of zero and non-zero porosities along with high aspect
33 ratio etched features that correspond to the inverse of the catalyst pattern. In another embodiment,

1 the current density can be modulated using a square wave function with a negative and a positive
2 value. This causes the “negative value” current density etch to prevent wandering of the catalyst,
3 and the “positive value” current density etch to create porosity in the layers. This path does not
4 require expensive process such as the deposition and etch of multiple alternating layers of
5 material.

6 **[00157]** Path II – SiSE with Catalyst Etching

7 **[00158]** Path II requires alternating layers of semiconducting material that vary in at least
8 one of the following properties: material type, doping concentration and dopant material. These
9 layers are deposited via epitaxy, chemical vapor deposition (CVD), physical vapor deposition
10 (PVD) etc. to enable creation of superlattices during SiSE. Table 1 describes examples of various
11 combinations of semiconductor alternating multilayers that can be used in the process flows
12 described above, focusing on Silicon. In Table 1, Donor and Acceptor doping of silicon is denoted
13 by p- and n-Si, and the “++” denotes the doping concentrations. For example, p++ Si means highly
14 doped silicon with a Boron concentration of $1 \times 10^{18} \text{ cm}^{-3}$ or higher. More than 2 alternating layers
15 can be used (e.g. ABCABC) for higher degree of control over doping variations and diffusion. An
16 embodiment of this is using atomically thin layers of Ge between the doped Si layers to decrease
17 migration of dopants during deposition. The main feature of this alternating stack etch is to get a
18 large difference in processing parameters such as etch or oxidation rates between the different
19 layers (Layer A vs Layer B for bilayer stacks) and use this difference to modify the stack and
20 ultimately get insulating/conducting lines.

21 **[00159]** The etched stack of alternating materials with alternating morphologies as a result
22 of the SiSE process are post-processed with thermal oxidation and/or ALD to get the desired
23 stable configuration of etched channels and slits. Fig. 11 shows an embodiment of the process
24 flow 1100 for an alternating stack of highly doped and undoped (or low-doped) silicon. Highly p-
25 doped silicon becomes porous and this porosity can be controlled based on the etchant
26 concentrations and the doping of the silicon layer. The low doped silicon does not change
27 morphology after etch. The porous silicon can then be oxidized at a much higher rate than the
28 non-porous Si. A thermal step to transfer dopants from the oxidized porous silicon (OPS) and
29 flow more dopant gases will then modify the low doped silicon into a word line in the Vertical
30 Channel regime. A short anisotropic oxide etch and subsequent ALD of metal will make the word
31 lines continuous on both sides of the etched channel, and annealing will form low resistivity silicide
32 WLs. This process is termed “Dielectric/Gate first” as the material stack deposited (or grown
33 epitaxially) prior to the SiSE process is in the final etched and thermally processed stack.

1 **[00160]** Fig. 11 shows a process flow 1100 for high aspect ratio (HAR) etch of channels and
2 slits with a catalyst mesh pattern similar to that shown in Fig 10. The etched stack of alternating
3 materials with alternating morphologies as a result of the SiSE process are post-processed with
4 sacrificial layer removal and/or atomic layer deposition (ALD) to get the desired stable
5 configuration of etched channels and trenches/slits. As illustrated in Fig. 11, during process step
6 1110, deposition of alternating multilayers is performed. This step is not needed if the system
7 starts with a bulk silicon substrate. During process step 1120, a catalyst mesh is patterned and
8 then SiSE is performed to get alternating layers of porous and non-porous material. During
9 process step 1130, oxidation of porous layers is performed. The oxidation process can also
10 oxidize a thin edge of the non-porous layer that needs to be removed. Process Step 1140 is used
11 to remove the oxide using an anisotropic etch such as Atomic Layer Etching or plasma etching
12 after lithography to block of material that shouldn't be etched. Process Steps 1150 – 1160
13 comprise of multiple lithography, deposition and etch processes needed to create a 3D NAND
14 Flash memory array. In some embodiments, process step 1150 comprises selective deposition
15 of metal on the non-porous layers and subsequent silicide formation. Process step 1160
16 comprises lithography and deposition of memory film e.g., for charge-trap (CT) 3D NAND- a
17 trilayer of silicon Oxide, silicon Nitride, silicon Oxide (ONO), poly-Si, and deposition of low k
18 dielectric and core filler using ALD and CVD.

19 **[00161]** Fig. 12 illustrates a sacrificial process flow 1200 for vertical channel 3D NAND
20 according to one or more embodiments of the present technology. This process is similar to that
21 of Fig. 11 with the major difference being the post-processing steps after CICE. Instead of
22 modifying one set of alternating layers, they are etched away and then replaced with conducting
23 material such as tungsten, cobalt, titanium nitride, tantalum nitride. First, CICE is performed on
24 an alternating stack of highly doped and undoped (or low-doped) silicon during operation 1210.
25 The highly doped silicon becomes porous and this porosity can be controlled based on the etchant
26 concentrations and the doping of the silicon layer. The low doped silicon does not change
27 morphology after etch, i.e. it remains crystalline and non-porous. The alternating stack is not
28 required if bulk Si with time varying electric fields is being used to create layers with alternating
29 porosities. Poly silicon and core filler are deposited in operation 1220 in the cylindrical channels
30 and provide support during sacrificial etch 1230 of one of the alternating layers. Subsequent
31 deposition of metal (e.g. tungsten, cobalt, titanium nitride, tantalum nitride) using CVD, ALD or
32 electroplating in step 1240 will make the word lines. This process is termed "Dielectric/Gate last"
33 as the material stack deposited (or grown epitaxially) prior to the CICE process is replaced either

partially (one set of alternating layers replaces by metal) or completely (the second set is then etched away and replaced with low-k dielectric) during process 1240.

[00162] Table 2 describes some examples of layer modifications that are outlined in Fig. 13. Modifications where one layer is selectively “etched away” are sacrificial process flows where Gate and/or dielectric films are replaced. This is similar to the TCAT process flows for 3D NAND fabrication. Some embodiments of this are paths C, D, E, F, G, as well as the process shown in Fig. 12. In such process flows, vertical channels have to be filled with material to support the structure as one set of alternating layers is etched away. The etched stack of alternating materials with alternating morphologies as a result of the SiSE process are post-processed with sacrificial layer removal and/or ALD to get the desired stable configuration of etched channels and slits. In one embodiment, the high aspect ratio lines are stabilized by creating lithographic links between the lines and removing them later. Poly silicon and core filler material are deposited in the cylindrical channels and provide support during sacrificial etch of one of the alternating layers. Subsequent deposition of metal (e.g. Tungsten, cobalt, nickel, tantalum nitride, titanium nitride, copper) will make the word lines. This process is termed “Dielectric/Gate last” as the material stack deposited (or grown epitaxially) prior to the SiSE process is replaced either partially (one set of alternating layers replaces by metal) or completely (the second set is then etched away and replaced with low-k dielectric).

Table 2: Paths B-G for 3D NAND array fabrication by modifying the materials in the superlattices made with SiSE, based on Fig. 13.

Paths	Superlattice Layers after SiSE	Superlattice modification 1	Superlattice modification 2	Superlattice modification 3	Superlattice modification 4	Superlattice modification 5
B	Porous Si	Porous Oxide	-	-	-	-
	Non-porous Si	Non-porous Si				
C	Porous Si	Porous Oxide	Porous Oxide	Porous Oxide	-	-
	Non-porous Si	Non-porous Si	Etched away	Metal Fill		
D	Porous Si	Porous Oxide	Etched away	Metal Fill	Metal Fill	Metal Fill
	Non-porous Si	Non-porous Si	Non-porous Si	Non-porous Si	Etched away	Dielectric Fill
E	Porous Si	Porous Oxide	Etched away	Etched away	Metal Fill	-
	Non-porous Si	Non-porous Si	Non-porous Si	Oxidized Si	Oxidized Si	
F	Porous Si	Etched away	Etched away	Metal Fill	-	-
	Non-porous Si	Non-porous Si	Oxidized Si	Oxidized Si		
G	Porous Si	Etched away	Metal Fill	Metal Fill	Metal Fill	-
	Non-porous Si	Non-porous Si	Non-porous Si	Etched away	Dielectric Fill	

[00163] Fig. 14-16 show some of the process flows for processing alternating layers of porous and non-porous silicon layers that are created by SiSE to create vertical channel 3D NAND

1 arrays. Fig. 14 comprises one replacement step and represents Path C from Fig. 13. Fig. 15-16
2 comprises two replacement steps, where Fig. 15 represents Path D and Fig. 16 represents Path
3 G as depicted in Fig. 13.

4 **[00164]** In Fig. 14, there are multiple steps including 1) SiSE to create high aspect ratio
5 channels and slits with alternating layers of non-porous and porous Si, 2) Oxidation of porous
6 layers, where a thin edge of the non-porous layer as well as connecting links are also oxidized,
7 3) Lithography to block the slits by depositing material such as a polymer and etching away
8 material in areas around the slits, 4) Deposition of films that form the memory core, e.g. Oxide-
9 Nitride-Oxide layers, poly-Si and oxide core using ALD and CVD, 5) Removal of material from
10 slits and lithography to protect the channels. The selective removal of material from the slits such
11 as polymer and the oxidized connecting links is done using selective etches such as with oxygen
12 plasma to remove the polymer and atomic layer etching to remove the oxide links, 6) Selective
13 removal of silicon layers using etchants such as TMAH without affecting the oxidized porous
14 silicon layer, 7) Deposition of conducting material (e.g. W, Co, TiN) using chemical vapor
15 deposition (CVD), atomic layer deposition (ALD), sputtering or physical vapor deposition (PVD),
16 etc. and subsequent etch back to isolate the conducting lines, and 8) (not depicted in image) Fill
17 exposed areas with insulating material.

18 **[00165]** In Fig. 15, the steps include 1) SiSE to create high aspect ratio channels and slits
19 with alternating layers of non-porous and porous Si, 2) Oxidation of porous layers, where a thin
20 edge of the non-porous layer as well as connecting links are also oxidized, 3) Lithography to block
21 the slits by depositing material such as a polymer and etching away material in areas around the
22 slits, 4) Deposition of films that form the memory core, e.g. Oxide-Nitride-Oxide layers, poly-Si
23 and oxide core, 5) Removal of material from slits and lithography to protect the channels. The
24 selective removal of material from the slits such as polymer and the oxidized connecting links is
25 done using selective etches such as with oxygen plasma to remove the polymer and atomic layer
26 etching to remove the oxide links, 6) Selective removal of oxide layers using etchants such as HF
27 without affecting the silicon layers, 7) Deposition of a thin Oxide layer using ALD and conducting
28 material (e.g. W, Co, TiN) using chemical vapor deposition, atomic layer deposition, sputtering,
29 etc, followed by subsequent etch back to isolate the conducting lines, 8) Selective removal of
30 silicon layers using etchants such as TMAH without affecting the deposited conducting material,
31 and 9) Deposition of insulating material such as silicon oxide using ALD.

32 **[00166]** In Fig. 16, the steps include 1) SiSE to create high aspect ratio channels and slits
33 with alternating layers of non-porous and porous Si, 2) Lithography to block the slits by depositing

1 material such as a polymer and etching away material in areas around the slits, 3) Deposition of
2 films that form the memory core, e.g. Oxide-Nitride-Oxide layers, poly-Si and oxide core , 4)
3 Removal of material from slits and lithography to protect the channels. The selective removal of
4 material from the slits such as polymer and the silicon connecting links is done using selective
5 etches such as with oxygen plasma to remove the polymer and atomic layer etching to remove
6 the silicon links. 5) Selective removal of porous silicon layers using etchants such as HF or HF +
7 H₂O₂ without affecting the non-porous silicon layers , 6) Deposition of conducting material (e.g.
8 W, Co, TiN) using chemical vapor deposition (CVD), atomic layer deposition (ALD), sputtering,
9 etc. and subsequent etch back to isolate the conducting lines, 7) Selective removal of silicon
10 layers using etchants such as TMAH without affecting the deposited conducting material, and 8)
11 Deposition of insulating material such as silicon oxide using ALD.

12 **[00167]** Fig. 17 depicts an embodiment of the 3D NAND architecture with vertical gates and
13 horizontal silicon channels. As illustrated in Fig. 17, which represents Path F from Fig. 13, the
14 steps include 1) SiSE to create high aspect ratio channels and slits with alternating layers of non-
15 porous and porous Si, 2) Oxidation of porous layers, where a thin edge of the non-porous layer
16 as well as connecting links are also oxidized, 3) Deposition of films that form the memory core,
17 e.g. Oxide-Nitride-Oxide layers, poly-Si and oxide core using CVD, ALD, etc., 4) Lithography to
18 create a mask for subsequent etching of memory material, 5) Etching of memory material from
19 un-patterned areas using atomic layer etching, plasma etching, etc., 6) Deposition of Gate
20 material such as W, poly-Si, Co, TiN, etc. In an alternative embodiment, the gate material can be
21 patterned by removing the lithographed mask, depositing gate material over the entire structure,
22 performing lithography and etching away gate material in un-patterned areas, 7) Removal of
23 excess gate material and lithographed mask using plasma or chemical etching, and 8) (not
24 depicted in image) Fill exposed areas with insulating material such as silicon oxide.

25 **[00168]** Non-sacrificial paths are similar to BiCS 3D NAND fabrication process flows and do
26 not involve etching away any layers, such as in path B. The etched stack of alternating materials
27 with alternating morphologies as a result of the SiSE process are post-processed with oxidation
28 (thermal, anodic etc.) and/or ALD to get the desired stable configuration of etched channels and
29 slits. For example, highly p-doped silicon becomes porous and this porosity can be controlled
30 based on the etchant concentration, electric field and the doping of the silicon layer. The low
31 doped silicon does not change morphology after etch. The porous silicon can then be oxidized
32 at a much higher rate than the non-porous Si. A thermal step to transfer dopants from the oxidized
33 porous silicon (OPS) and flow more dopant gases will then modify the low doped silicon into a

1 word line in the Vertical Channel regime. An optional short anisotropic oxide etch and subsequent
2 ALD of metal will make the word lines continuous on both sides of the etched channel, and
3 annealing will form low resistivity silicide WLs. This process is termed "Dielectric/Gate first" as
4 the material stack deposited (or grown epitaxially) prior to the SiSE process is in the final etched
5 and thermally processed stack.

6 **[00169]** Note that the superlattices that used in various embodiments begin with in Table 2
7 (Porous Si/ Non-porous Si) can be fabricated using Paths I or II. Also, Path A, which describes
8 including staircase etching, can be added to the process flows of any of the paths. Other
9 embodiments of the superlattice can include alternating layers with differing porosities and/or
10 different materials such as such as Ge, $\text{Si}_x\text{Ge}_{1-x}$, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC
11 etc. All layers of the superlattice can be non-porous as well with the alternating layers still having
12 different processing rates of oxidation, chemical etch etc. An example is a p-doped Si/ n-doped
13 Si superlattice where alkaline etchants such as TMAH or KOH etch only the p-type Si under
14 electric bias. Path B can also be used to make Vertical Gate based 3D NAND Flash architectures,
15 with crystalline horizontal silicon channels.

16 **[00170]** Various embodiments of the CICE process use a patterned catalyst that sinks into
17 the substrate as the etch progresses, leaving behind un-patterned areas as high aspect ratio
18 features. The catalyst meshes can be patterned to etch both channels and word-line slits
19 (trenches) in one lithography step, and the CICE process can etch both these features
20 simultaneously. Some examples of the catalyst meshes are shown in Figs. 18A-18C. To prevent
21 wandering of the catalyst mesh and for reliable transport of etchant solution, electric fields,
22 ceilings and/or linked continuous patterns can be used. The resulting high aspect ratio features
23 can be prevented from collapse by mitigation techniques such as using surface tension gradient
24 chemicals (ethanol, isopropyl alcohol etc.), super critical drying and lithographically connected
25 features. These two constraints can also be met by using a patterning technique with features
26 connected by links, and by using controlled deposition or etch after the CICE process to convert
27 the high aspect ratio linked structure into the desired 3D NAND configuration.

28 **[00171]** Fabrication of the catalyst pattern for SiSE requires multiple lithography and etch
29 steps. The critical dimensions and overlay requirements are shown in Figs. 18A-18C for various
30 layout schemes for 3D NAND Flash arrays based on both Vertical Channel (VC) as well as
31 Vertical Gate (VG) Architectures. Figs. 18A-18C show the etched features. As illustrated in Figs.
32 18A-18C, "a" represents the width of a block of memory channels, "b" represents the width of the
33 lithographic links, "c" is the distance between blocks of width a, "d" represents the diameter of the

1 circular channels, “e” is the pitch between holes in the lateral direction, “f” is the shortest pitch of
2 the holes arranged hexagonally, and “g” is the shortest distance between the block of width “a”
3 and the circular channel. The thin connecting lines with width “b” are called lithographic links, and
4 they connect isolated semiconducting features to improve stability of subsequently etched
5 interconnected high aspect ratio multilayer semiconductor structures. The intended design of the
6 catalyst mesh depends on the layouts of the 3D NAND Flash arrays and incorporates lithographic
7 links to stabilize the etched structures and optionally improve diffusion of etchants and prevent
8 wandering of the catalyst features.

9 **[00172]** Fig. 18A-18C shows layouts and dimensions for embodiments of 3D NAND arrays.
10 Two sets of dimensions are described below: one with aggressive scaling limited by lithography
11 constraints, and the other by assuming the minimum channel diameter is 50nm for VC based
12 devices. VG based devices have more aggressive scaling possibilities as the lithography pattern
13 requires mainly lines and spaces (L/S) and not holes or pillars, and L/S can be made smaller by
14 multiple patterning.

15 **[00173]** Some embodiments for dimensions of features in Fig. 18 are: Fig. 18A shows a VC
16 3D NAND configuration with two rows of staggered holes per block. For a half pitch of 20nm (in
17 X-direction) and 25nm for dots and 35nm for blocks in Y-direction, a=60nm, b=10nm, c=10nm,
18 d=25nm, e=40nm, f=35nm and g=10nm. For a half pitch of 35nm (in X-direction) and 42nm for
19 dots and 85nm for blocks in Y-direction, a=110nm, b=10nm, c=20nm, d=50nm, e=70nm, f=60nm
20 and g=10nm. Fig. 18B shows a VC 3D NAND configuration with four rows of staggered holes per
21 block. For a half pitch of 20nm (in X-direction) and 25nm for dots and 65nm for blocks in Y-
22 direction, a=120nm, b=10nm, c=10nm, d=25nm, e=40nm, f=35nm and g=10nm. For a half pitch
23 of 35nm (in X-direction) and 42nm for dots and 120nm for blocks in Y-direction, a=220nm,
24 b=10nm, c=20nm, d=50nm, e=70nm, f=60nm and g=10nm. Fig. 18C shows a Vertical Gate 3D
25 NAND geometry where lines with width “a” denote silicon channel dimensions, with a=20nm,
26 b=10nm and c=20nm in one embodiment.

27 **[00174]** The examples of dimensions described for Fig.18 are limited by lithography and
28 electronic properties required for the memory arrays. The VC 3D NAND channel hole must be
29 filled with memory layer, e.g. Oxide-Nitride-Oxide (ONO) and poly-silicon channel material. The
30 minimal poly-Si channel diameter, which is constrained by the string read current and the tolerable
31 field enhancement, is around 20nm. The minimal ONO thickness, which is constrained by the
32 device performance and reliability, is around 15nm. Thus, the minimal hole diameter is around
33 50nm. For certain process flows, an oxidation step is performed after SiSE to create alternating

1 layers of porous silicon oxide and non-porous silicon. This oxidation step can also oxidize a thin
2 layer (<5nm) of the non-porous silicon at the edges. This thin layer can be retained as a memory
3 layer or removed. If it is removed, the effective dimensions of the pattern will change by twice
4 the dimension of the oxide. e.g., for oxidation and subsequent removal of 5nm of material, the
5 diameter of the channel will increase by 10nm, the width of the word line will decrease by 10nm,
6 and the width of the spacing between the lines increases by 10nm. The initial dimensions should
7 therefore be adjusted accordingly, based on the final desired parameters.

8 **[00175]** Fabrication of sub-30nm features with even smaller connections for structural
9 stability is extremely challenging, as electron beam lithography can write sub-10nm features but
10 suffers from large overlay, whereas photolithography has superior overlay but poor resolution.
11 Some embodiments can use photolithography and imprint lithography to pattern the films.

12 **[00176]** The 3D NAND feature designs shown in Figs. 18A-18C can be patterned using
13 lithography techniques such as photolithography with multiple patterning, imprint lithography,
14 electron beam lithography, directed self-assembly, laser interference lithography etc. The process
15 of making the masks for these various lithography techniques is described below.

16 **Patterning with Imprint Lithography**

17 **[00177]** Fig. 19D depicts a catalyst design that has a linked structure to prevent wandering
18 and improve diffusion. In one embodiment, the width of the link pattern is 10nm, the pitch is 25nm,
19 and the lines are not in a regular arrangement. To fabricate such patterns, a grid pattern is made
20 using electron beam lithography. Elements of the grid are then removed by patterning a linked
21 structure using electron beam lithography and etching away selected regions of the grid. The
22 resulting pattern can then be etched into the template substrate to create a master template for
23 imprint lithography.

24 **[00178]** Imprint lithography can be used to pattern aperiodic irregular patterns with high
25 resolution and tight pitch. For imprint lithography, a template can be made to print the catalyst
26 patterns shown in Figs. 18A-18C. The fabrication of a template is shown in Fig. 19A-19C. The
27 master templates 1910 and 1920 shown in 19A and 19B can be made using electron beam
28 lithography. In one embodiment, features in Fig. 19A can be made using two sets of L/S
29 perpendicular to each other create 20nm x 20nm blocks at a pitch of 100nm, and features in Fig.
30 19B can be made using 20nm diameter holes at 40nm pitch and 20nm lines at 80nm pitch.

31 **[00179]** The final master template 1930 shown in 19C can be made by imprinting with master
32 template 1910 shown in Fig. 19A, the imprinted features are etched into a hard mask, and then

1 master template 1920 shown in Fig. 19B can be patterned after aligning with the features
2 imprinted by master template 19A. In accordance with various embodiments, template alignment
3 can be done using an alignment method where, within a lithographic field, template 1920 shown
4 in Fig. 19B has features that are intentionally offset with varying magnitudes and directions from
5 one subfield to the next. After imprinting, the sub-field that has the ideal alignment requirements
6 is selected and used to create a final master template 1930 shown in Fig. 19C using a step-and-
7 repeat method. Based on overlay alignment requirements, the final master template 1930 shown
8 in Fig. 19C can also be made using photolithography. In this case, the second template 1920
9 shown in 19B is a photolithography mask with larger dimensions to take into consideration the
10 photolithography resolution. These larger dimensions can then be decreased using plasma etch
11 techniques. Fig. 19D is an example of a lithographically linked pattern where the lines are made
12 with imprint lithography (whose template is made with electron beam lithography), and the dots
13 are aligned and printed using imprint or photolithography or vice versa.

14 **[00180]** In another embodiment, fabrication of patterns such as in Fig. 19D is done using
15 photolithography and multiple patterning. Elements of the grid are then removed by patterning
16 and shrinking holes in selected areas and etching away the grid lines, thereby creating a linked
17 pattern. The patterning of holes may take multiple steps due to limitations of minimum pitch with
18 photolithography.

19 **[00181]** The current form of photolithography, 193nm wavelength with immersion, uses
20 trilayer resists and is limited to ~ 38nm half pitch for lines and spaces. Methods such as self-
21 aligned double (SADP)/quad (SAQP) patterning and Litho-Etch-Litho-Etch (LELE) are required to
22 go to smaller dimensions and tighter pitch. This requires multiple deposition and etch steps, and
23 is inherently suited towards periodic patterns. The minimum resolution and pitch for circles,
24 however, is larger. For VG 3D NAND architectures without circles, photolithography along with
25 trim etching can be used to create lines and spaces perpendicular to each other. The process of
26 making patterns for VC 3D NAND are more involved.

27 **[00182]** Figs. 20A-20J show a method of making such patterns using photolithography. In
28 the figure, the catalyst is deposited after the photolithography process, such that the exposed
29 regions (silicon) are now covered by the catalyst material. The catalyst deposited on top of the
30 patterned features can optionally be lifted off. Another embodiment can be used where the
31 photolithography is done on the catalyst film and then the catalyst is etched away in exposed
32 areas. In that case, the pattern is the inverse of that shown in Fig. 18.

1 **[00183]** Figs. 20A-20E show both cross-sectional views (top) and top-views of the
2 lithography steps. Figs. 20F-20J show the top views only. In Fig. 20A lithographic links are made
3 using squares of side 40nm and pitch 80nm (y direction) and 40nm (x direction) patterned with
4 first hard mask, poly-silicon (pink) on a silicon nitride (blue) layer. In Fig. 20B trim etch is done to
5 get squares of side 10nm. In Fig. 20C, the features are planarized with spin on glass and lines
6 of 40nm width, 80nm pitch are aligned and patterned. In Fig. 20D, spacer material is deposited to
7 increase the line width to 70nm. In Fig. 20E, the lines and squares are etched into a hard mask
8 layer such as silicon nitride. In Fig. 20F, LELE is performed: align and pattern 50nm holes with
9 80nm pitch (x direction), 80nm pitch (y direction); trim etch to decrease the diameter to 25nm and
10 etch into underlying silicon nitride. In Figs 20G, 20H, and 20I, step 20F is repeated with shifted
11 alignment. In Fig. 20J catalyst material can be deposited.

12 **[00184]** Density multiplication can be used using directed self-assembly instead of multiple
13 LELE steps in photolithography. Fig. 21 shows the process flow for making a catalyst pattern with
14 substantially connected catalyst features using self-assembly and lithography. In Fig. 21A, dots
15 are patterned using photolithography. In Fig. 21B, these dots are used to direct block copolymers
16 to multiply the density using directed self-assembly. Lines are then patterned to block off areas in
17 accordance to 3D NAND Flash catalyst designs (Fig. 21C). A subsequent etch transfers the dots
18 that are not blocked by lines into a hard mask such as silicon nitride or carbon (Fig. 21D). Another
19 lithography step is done to pattern lines (Fig. 21E), and etch into the hard mask (Fig. 21F). The
20 resist is then removed to reveal the final features in the hard mask. (Fig. 21G). In Fig. 21H, catalyst
21 material is deposited. Although the process does not depict lithographic links, they can be
22 made incorporated into the process flow similar to Fig. 20. Also, patterning with self-assembly
23 can be used to make an imprint lithography template as well.

24 **[00185]** For the 3D NAND Flash designs, etching circular channels and rectangular slits
25 simultaneously cannot be achieved reliably with plasma etching with accurate control of sidewalls.
26 Similarly, for the features with connecting links, the sub-10nm connections between pillars cannot
27 be retained over high aspect ratios. Dry plasma etching processes, which are used in the
28 semiconductor industry for anisotropically etching highly controlled nanopatterns, require
29 expensive vacuum equipment and cannot retain cross-section shape easily when patterning high
30 aspect ratios (>50:1). They suffer from etch challenges such as Aspect Ratio Dependent Etching
31 (ARDE) and etch taper.

32 **[00186]** The SiSE process, on the other hand, can anisotropically etch the required pattern
33 as well as create a superlattice without loss of resolution. However, there are various challenges

1 that need to be addressed to make SiSE a viable technology for commercialization. This section
2 describes these challenges and solutions for achieving wafer-scale etching of high aspect ratio
3 nanostructure stacks in semiconducting materials.

4 **[00187]** A step-by-step description of the various processes that could be used for this new
5 fabrication method is defined. Parameters that need to be optimized at each step for good
6 electrical performance of final device, mechanical stability at intermediate steps, CMOS
7 compatibility, and cost and throughput are also listed in the following sections.

8 **[00188]** Traditional 3D NAND processes use alternating layers of SiO/SiN or SiO/Poly-Si
9 which are etched and optionally replaced with conducting material such as W to get stacks of
10 alternating conducting and insulating lines that form the word lines and dielectrics of 3D NAND
11 cells. In various embodiments, alternating layers of semiconducting material may be used instead
12 of SiO/SiN or SiO/Poly-Si. Since SiSE can etch semiconducting material while simultaneously
13 changing their morphology depending on tailorable material properties such as doping
14 concentration and dopant type, the alternating layers are designed to ensure selective removal
15 or oxidation to get final conducting and dielectric lines.

16 **[00189]** This is not a problem for Path I (see, e.g., Fig. 13), where bulk silicon substrate is
17 used for SiSE and no alternating layer deposition has to be taken into account.

18 **[00190]** The method employed for deposition of the alternating layers or “superlattice”
19 depends on commercial availability, cost, throughput, growth rate, thermal budget, number of
20 layers, thicknesses of layers, mobility and resistivity of layers before and after etch, employability
21 of crystallographic etching etc. For example, poly-Si layers need higher thicknesses than epitaxial
22 silicon to overcome grain boundary issues and get good conductivity of etched word lines. Poly-
23 Si layers may also require a thin diffusion blocking layer between the alternatively doped layers
24 to suppress diffusion of dopants across layers, as diffusion of dopants is higher in poly-Si than
25 crystalline Si. In the case of epitaxial silicon, a taper etch to create staircase contacts can also
26 be done on the crystalline layers by using alkaline etchants like KOH, TMAH and EDP.

27 **[00191]** Epitaxial (epi) growth of silicon in production today is based on Chemical Vapor
28 Deposition (CVD), a process whereby a thin solid film is synthesized from the gaseous phase by
29 a chemical reaction. High temperature epi growth of silicon, above 1000C, offers high throughput,
30 in situ doping and prevents contamination, whereas Molecular Beam Epitaxy (MBE) enables
31 abrupt steps in doping profile but with very low growth rates. Low temperature epitaxy using CVD
32 at around 650-850C offers a compromise for the growth of the silicon superlattices described in

Table 1. Temperature, pressure, gas flow rates, substrate preparation, surface treatment and oxidation prevention are the main parameters that determine the epi superlattice quality. The partial pressure of the gas used for doping, such as B_2H_6 or PH_3 , determines the doping concentration in the epi layer. Having a low total pressure during growth will allow for better junctions due to decreased contamination from gases of the previous layer. While all these parameters play a critical role in the epi growth, temperature, dopant concentrations and epi layer thicknesses are the most important as they determine what the results of the next process steps will be, as explained further below.

- Temperature: The temperature of epi growth depends on various factors. The crystallinity of the epi films can be achieved at temperatures ranging from 500C onwards. At low temperatures the diffusion of dopants is reduced and some embodiments can get abrupt profiles, but the growth rate is low. Depending on the dopant type and its diffusivity in silicon, some embodiments can calculate the diffusivity across a high-doped/low-doped interface.
- Dopant concentrations: Simulations of Fick's Laws with appropriate modifications for electric field effects, concentration values and gradients etc. are used to determine what the doping material and concentration for each alternating layer can be to get the required final diffusion profiles. This depends on the temperature of the reaction chamber, the required thermal budget of the subsequent process steps, the concentration gradient across the layers and the presence of any defects during epi growth. The diffusion coefficients of common dopants in silicon depend exponentially on the temperature. ($D = D_0 \cdot \exp(-E_a/kT)$) Slow diffusers (As and Sb) are preferred over fast diffusers (P, B and In) and the dopant selection also depends on the solid solubility limits in silicon.
- Layer Thickness: Depending on the width of the final word lines, the thickness of the conducting layer has to be tuned to minimize resistivity, while the thickness of the dielectric layer has to be tuned to reduce parasitic capacitance and maximize resistivity. If the word-line layers are made of polycrystalline silicon then the increase in resistance due to grain boundaries has to be taken into consideration.

[00192] Let us consider an example of a P++/P superlattice where one layer has Boron with a concentration of $1E18$ while the other layer has a Boron concentration of $1E15$. For epitaxial growth at 650C and a pressure of 10Pa mixture in an ultraclean environment, the deposition rate can be $\sim 100nm/min$. At this temperature, the diffusion constant for B is $7.7E-20 \text{ cm}^2/s$. To determine the diffusion profile, some embodiments need to know the thickness of each layer and

1 the amount of time the wafer is in the chamber, i.e. the number of layers that need to be grown.
2 At a Boron concentration of $1E18$, the resistivity of the word line is 0.04 ohm-cm. This can be
3 decreased further by incorporating a metal to form a silicide or by annealing after the subsequent
4 SiSE process to transfer all the dopants from the oxidized porous layer to the crystalline silicon
5 layer. For a layer thickness of 100nm, the total growth time for 256 layers is ~5hrs. The maximum
6 diffusion will then occur at the first layer grown, and the diffusion length is given by $x_j=2*\sqrt{Dt}$.
7 This gives the maximum diffusion length of 0.8nm. Thus, since the diffusivity is very low at 650C,
8 the impact of temperature on the diffusion length is minimal. Further factors such as multilevel
9 concentration gradients and electric fields can be factored in using simulations. Slow deposition
10 rates such as 100nm/min cannot be justified from a cost perspective. At 1000C, the deposition
11 rate is 10 microns/min, and 256 layers can be deposited in less than 3 minutes.

12 **[00193]** However, the diffusion constant for Boron at this temperature is $1.39E-14$ cm²/s,
13 and the diffusion length is 31nm. To achieve a compromise between the 2 parameters, some
14 embodiments pick a temperature of, or around, 800C, where a deposition rate of 1 micron/min is
15 obtained. This will make the process of depositing 256 layers take ~30min, and 100 layers take
16 10min. The diffusion length of B is then ~6nm at the bottommost layer (worst case scenario) for
17 256 layers, and is 3nm for 100 layers. Having a sub-5nm junction for 100nm thick layers should
18 be sufficient. However, the above junction lengths denote the distance from the interface where
19 the concentration has changed by 1/e. This is not sufficient to make a reliable process. The SiSE
20 process is therefore tuned to ensure that the dopant concentration at which the morphology
21 changes from solid to porous is sharp, and this can be done by tuning the etchant concentrations.

22 **[00194]** Plasma enhanced ALD can be used in some embodiments to seal the pores of the
23 porous layers. ALD of SiO₂ is used to fill up the holes and slits that are etched using SiSE. The
24 substrate is then planarized to enable the next process steps including lithography and plasma
25 etching. In accordance with various embodiments, lithography can be performed to open up the
26 channels and prevent deposition of films in the slits. Memory layers (such as Oxide-Nitride-Oxide),
27 poly-Si channel and core filler material can be then deposited into these channels (vertical holes).

28 **[00195]** For epitaxially grown crystalline layers of silicon, alkaline etchants such as KOH and
29 TMAH can be used to anisotropically etch the <100> crystal plane. This would reduce the number
30 of etch and lithography steps required for the staircase etch to create contacts to each word line
31 layer in the vertical channel structure. This alkaline wet etch can be done on the as-grown
32 epitaxial material stack before or after CICE. If one of the alternating layers is highly p-doped,

1 TMAH can be used instead of KOH depending on relative etch rates along crystal planes and at
2 different dopant concentrations.

3 **[00196]** Fig. 22 illustrates an example of a 3D NAND staircase etch according to one or more
4 embodiments of the present technology. After epitaxial growth of doped/undoped Si, a taper etch
5 process is done using alkaline etchants to create contact regions for word lines. The length of
6 the projection for contact regions depends on the thickness of the insulating layer. Another
7 embodiment of this process involves use of electrochemical etching to create alternating layers
8 of silicon with differing porosities based on the doping of the individual layers, without the use of
9 CICE. This stack could then be etched with plasma etching, and angled etch prior to
10 electrochemical etch to create the staircase.

11 **[00197]** Fig. 23 is similar to Fig. 22, with the main difference being that the taper etch is done
12 on bulk Si instead of alternating semiconducting layers. SiSE is then performed on the taper-
13 etched bulk Si, and then after 3D NAND memory fabrication steps, selective plasma etching is
14 done to reveal contact regions on the conducting lines.

15 **[00198]** For Path I, bulk silicon is etched, whereas for Path II, epitaxially grown crystalline
16 layers of silicon are etched. Crystallographic etchants such as KOH, EDP and TMAH can be used
17 to create a taper. For instance, 30% KOH or 10% TMAH at a temperature of 60C.

18 **[00199]** Some embodiments use the process of staircase etch on bulk silicon with alkaline
19 etchants or angled plasma etch to create contact regions for word lines. The length of the
20 projection for contact pads depends on the thickness of the insulating layer since crystallographic
21 etching creates a taper of 54.74° . This would reduce the number of etch and lithography steps
22 required for the staircase etch to create contacts to each word line layer in the vertical channel
23 structure. However, the taper does not create vertical sidewalls for the stairs, and this might affect
24 the reliability of placement of metal contacts to the word lines. This can be corrected by increasing
25 the thickness of the dielectric layers or the width of the word lines depending on area consumed
26 by the stair-stepping features. Alternatively, an angled plasma etch with faraday cages can also
27 be used to create a taper.

28 **[00200]** As the SiSE progresses, the catalyst mesh etches the semiconductor material stack
29 to reveal high aspect ratio features with holes and slits for 3D NAND channels and word line
30 separation. SiSE can be stopped by using an etch stop layer, a timed etch, or by monitoring and
31 controlling electric field parameters. The etchant composition as well as electronic hole-
32 generation during the process results in alternating films of differing morphologies based on their

material and doping concentrations. After SiSE, one of the layers can be selectively removed or modified (e.g. oxidized) to make 3D NAND layers. The volume change during oxidation of porous silicon can be suppressed by controlling the porosity and density of pores in the porous silicon layers, thereby reducing the mechanical stress on the structures. The porous layer oxidation rate is much greater than that of single crystal silicon, and can be done at lower temperatures to increase selectivity. For instance, at 700C, the surface and bulk of porous silicon layers (for individual layers thinner than 1 micron) get oxidized in 3min, while only 3nm of the surface of crystalline silicon is oxidized in dry O₂.

[00201] Oxidation rate differences between porous silicon layers and crystalline silicon layers and etch rate differences between porous oxide and silicon or porous silicon and crystalline silicon has to be very high. This is to ensure that there is no undercut and to increase the number of memory layers that can be made with the SiSE process. Table 3 lists etchants that can be used to selectively remove one layer from a superlattice for various superlattice modifications to get 3D NAND flash arrays with alternating layers of insulating and conducting films. Surfactants and other such chemicals can be added to the etchants to improve etch selectivity of Layer A to Layer B at all crystallographic orientations where applicable. The etchants may be in liquid or vapor form.

Table 3: List of etchants that can be used to remove one layer from a superlattice with a selectivity	
Layer A/Layer B	Etchants to selectively remove Layer A
Porous Si/Non-porous Si	Dil. Hydroxide solutions (KOH, NH ₄ OH, NaOH, TMAH etc.), photoresist developer, ethylene di-amine pyro-catechol (EDP), HF, Buffered HF, HF + oxidants (H ₂ O ₂ , dissolved oxygen, DMSO, KMnO ₄ , K ₂ S ₂ O ₈), HF + illumination, HF + alcohols, NH ₄ F etc.
Porous Oxide/Non-porous Si	HF, Buffered HF, Vapor HF
Non-porous Si/Porous Oxide	Dil. Hydroxide solutions (TMAH, KOH), EDP
Non-porous Si/Tungsten	Si iso etch (126 parts HNO ₃ : 60 parts H ₂ O : 5 parts NH ₄ F), KOH, TMAH
SiGe/Si	HCl
Ge/Si	H ₂ O ₂

[00202] Table 4 describes examples of various combinations of semiconductor alternating multilayers with process steps required to ensure selective removal or oxidation of one of the alternating layers to get final metal lines and dielectric layers. Donor and Acceptor doping of silicon is denoted by p- and n-Si, and the “++” denotes the doping concentrations. For example, p++ Si means highly doped silicon with a Boron concentration of 1e18 cm⁻³ or higher. More than 2 alternating layers can be used (e.g. ABCABC) for higher degree of control over doping variations.

An embodiment of this is using atomically thin layers of Ge between the doped Si layers to prevent migration of dopants during epitaxial growth. A staircase etch can also be done if the layers are grown epitaxially to get crystalline morphology by using alkaline etchants like KOH, TMAH and EDP to etch the <100> planes selectively over micron-scale range. The main feature of this alternating stack etch is to get a large difference in etch or oxidation rates between the different layers (Layer A vs Layer B for bilayer stacks) and use this difference to modify the stack and ultimately get insulating/conducting lines.

Table 4: Examples of various combinations of semiconductor alternating multilayers with process steps required to ensure selective removal or oxidation of one of the alternating layers to get final metal lines and dielectric layers.

Process	Initial Layers		Selectivity	Layer Modifications	Final Layers 11
Sacrificial (Similar to TCAT process)	Si	Ge	Selective etching of Ge, e.g. with peroxide	Oxidation of remaining layer	Dielectric and conducting layers (e.g. porous SiO ₂ and W)
	n-Si	p-Si	Alkaline etchants with electric bias etches only p-Si		
	p++ Si	p-Si	1 layer becomes porous by tuning MACE etchant ratio, dil.		
	n++ Si	n Si	Alkaline solutions etch only porous layer;		
	n++ Si	p Si	Alternatively, after oxidation of porous silicon,		
	p++ Si	n Si	Alkaline etch of only Si		
Non-sacrificial (Similar to BiCS process)	p++ Si	p-Si	1 layer becomes porous by tuning MACE etchant ratio	Oxidation of porous layer, Anneal and dope to get dopant diffusion from the porous oxide	Dielectric and conducting layers (e.g. porous SiO ₂ and highly doped Si/Silicide)
	n++ Si	n Si			
	n++ Si	p Si			
	p++ Si	n Si			

[00203] Various embodiments of the present technology may be used to create 3D NAND VC with no replacement steps, similar to the BiCS process. For example, in some embodiments a substrate may be provided. Then, alternating layers of a semiconductor material (e.g., doped

1 or undoped Si) may be deposited. Then, lithography and taper etch using a crystallographic
2 anisotropic etchant may be performed. The catalyst can then be patterned. For example, some
3 embodiments may use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst
4 or selective electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the
5 catalyst may be removed using a wet etch (e.g. aqua regia) or isolate with insulator. The layers
6 can be selectively processed (e.g., oxidize porous layers and connecting links) and the pores
7 sealed with Atomic Layer Deposition (ALD). Lithography can be used to block areas between
8 word lines before deposition of memory material such as Oxide-Nitride-Oxide (ONO) along with
9 poly-Si core and/or oxide core filler. Material can then be removed from word line slits and a low-
10 k dielectric can be deposited in slits. To create a staircase along the etched taper, the taper can
11 be etched using a plasma etch that is selective to one set of alternating layers.

12 **[00204]** In some embodiments, a process for 3D NAND VC with Oxidation and Replacement
13 can be utilized, similar to the TCAT process. For example, in some embodiments a substrate
14 may be provided. Then, alternating layers of a semiconductor material (e.g., doped or undoped
15 Si) may be deposited. Then, lithography and taper etch using crystallographic anisotropic etchant
16 may be performed. The catalyst can then be patterned. For example, some embodiments may
17 use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective
18 electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the catalyst may
19 be removed using a wet etch (e.g. aqua regia) or isolate with insulator. The layers can be
20 selectively processed (e.g., oxidize porous layers and connecting links) and the pores sealed with
21 ALD. Lithography can be used to block areas between word lines and a stabilizing core (e.g.,
22 poly-Si core and oxide core filler) can be deposited.

23 **[00205]** The material can be removed from the word line slits. Atomic Layer Etching is used
24 to remove the thin oxide layer surrounding the porous-oxide/crystalline Si structures. The next
25 set to processes to make 3D NAND Flash arrays may include one replacement step (e.g., etch
26 crystalline Si selective to porous oxide, pore sealing with ALD, deposit memory material ONO,
27 deposit W and etch back to isolate word lines, etc.); or two replacement steps (e.g., etch porous
28 oxide selective to crystalline Si, deposit memory material ONO, deposit W and etch back to isolate
29 word lines, etch Si selective to W, deposit SiO₂, etc.) or (e.g., etch porous oxide selective to
30 crystalline Si, deposit SiO₂ and etch back to isolate, etch crystalline Si selective to deposited SiO₂,
31 deposit memory material ONO, deposit W and etch back to isolate word lines, etc.). And so forth
32 and so on. Then, a low-k dielectric can be deposited in slits. To create a staircase along the

1 etched taper, the taper can be etched using a plasma etch that is selective to one set of alternating
2 layers.

3 **[00206]** In some embodiments, a process for 3D NAND VC with Replacement can be utilized
4 similar to the TCAT process. For example, in some embodiments a substrate may be provided.
5 Then, alternating layers of a semiconductor material (e.g., doped or undoped Si, Si/SiGe, Si/Ge,
6 etc.) may be deposited. Then, lithography and taper etch using crystallographic anisotropic
7 etchant may be performed. The catalyst can then be patterned. For example, some embodiments
8 may use deposition of discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective
9 electrodeposition of Pt, Pd or Ru. The SiSE process can then be performed and the catalyst may
10 be removed using a wet etch (e.g. aqua regia) or isolate with insulator. The pores can be sealed
11 with ALD. Lithography can be used to block areas between word lines and a stabilizing core (e.g.,
12 poly-Si core and oxide core filler) can be deposited. The material can be removed from the word
13 line slits. The next set to processes to make 3D NAND Flash arrays may include one replacement
14 step (e.g., etch porous silicon selective to crystalline Si, deposit memory material ONO, deposit
15 W and etch back to isolate word lines, etch Si selective to W, deposit SiO₂, etc.); or two
16 replacement steps (e.g., etch porous silicon selective to crystalline Si, oxidize crystalline Si,
17 deposit memory material ONO, deposit W and etch back to isolate word lines, etc.) or (e.g., etch
18 porous silicon selective to crystalline Si, deposit SiO₂ and etch back to isolate, etch crystalline Si
19 selective to SiO₂, deposit memory material ONO, deposit W and etch back to isolate word lines,
20 etc.). And so forth and so on. Then, a low-k dielectric can be deposited in slits. To create a
21 staircase along the etched taper, the taper can be etched using a plasma etch that is selective to
22 one set of alternating layers.

23 **[00207]** In some embodiments, a process for 3D NAND with Vertical Gate can be utilized.
24 For example, in some embodiments a substrate may be provided. Then, alternating layers of a
25 semiconductor material (e.g., doped or undoped Si, Si/SiGe, Si/Ge, etc.) may be deposited. Then,
26 lithography and taper etch using crystallographic anisotropic etchant may be performed. The
27 catalyst can then be patterned. For example, some embodiments may use deposition of
28 discontinuous catalyst – Pt, Pd, Ru, CMP/Lift-off of catalyst or selective electrodeposition of Pt,
29 Pd or Ru. The SiSE process can then be performed and the catalyst may be removed using a
30 wet etch (e.g. aqua regia) or isolated with insulator. The layers can be selectively processed (e.g.,
31 oxidize porous layers and connecting links). The pores can be sealed with ALD. Lithography can
32 be used to block areas between layers and ONO memory material can be deposited. Word lines
33 can also be deposited perpendicular to the horizontal channel lines. Then, a low-k dielectric can

1 be deposited in slits between the word lines. To create a staircase along the etched taper, the
2 taper can be etched using a plasma etch that is selective to one set of alternating layers.

3 **[00208]** In one embodiment, 3D NAND can be fabricated using silicon nanowires as the
4 channel material followed by deposition of alternating layers of conducting and insulating material.
5 MSP-CICE and novel connecting links- or ceiling-based collapse mitigation techniques are used
6 to pattern arrays of NWs instead of Deep Reactive Ion Etching processes. DRIE uses processes
7 such as the Bosch process which creates a scalloped sidewall, with surface damage, which
8 degrades FET performance. Various embodiments of the CICE process proposed here should
9 be significantly less damaging, offering smooth sidewalls and more sophisticated cross-section
10 geometries, thereby leading to superior performance. The high aspect ratio vertical NWs created
11 using CICE can be used for vertical 3D NAND flash memory. This involves deposition of memory
12 material including a high-k dielectric with large trap density for charge storage by conformal ALD
13 on the vertical NWs. A sequence of conducting material, separated by insulating material is then
14 deposited to form the word lines and create a NAND string leading to multi-layer ultra-high density
15 3D NAND Flash memory.

16 **DRAM**

17 **[00209]** DRAM products are approaching fundamental limitations as scaling DRAM
18 capacitors and transistors is very difficult with 2D structures. The current workaround is to use
19 stack or trench capacitors to increase capacitance per cell without compromising on real estate.
20 However, this method has limitations of high aspect ratio trench etching for trench capacitors, and
21 stability for stack capacitors. Also, decreasing feature sizes affect the reliability of planar and
22 recessed channel or fin-based DRAM transistors. Certain DRAM cell configurations also use a
23 cell size factor of $5\text{-}6F^2$ instead of the ideal $4F^2$ cell. As feature sizes decrease from the current
24 20nm half pitch to sub 10nm by 2025, there is a need for incorporating vertical cell access
25 transistors with high aspect ratio capacitors in a self-aligned fashion.

26 **[00210]** Fig. 24 illustrates an exemplary DRAM design with deposition of transistor, capacitor
27 and interconnect material on nanowires etched by CICE according to one or more embodiments
28 of the present technology. The top of Fig 24 illustrates a sectional view of the capacitor region;
29 Bit lines run perpendicular to the figure and connect the top N+ doped silicon regions. Various
30 embodiments use a vertical nanowire based DRAM architecture that incorporates both Gate-All-
31 Around transistors as well as self-aligned capacitors to produce a $4F^2$ cell size factor. This can
32 enable scaling of DRAM to sub-10nm half pitch. Since the vertical sidewall angle is greater than
33 89.5° for CICE processes, center-to-center distance between pillars can be sub-20nm, sub-15nm,

1 sub-10nm, etc. The arrangement of pillars can be hexagonal to create more compact DRAM cells.
2 The etched pillars can be aligned perpendicular to the substrate or at an angle based on the CICE
3 etchant concentrations. The cross-sections of the pillars can be optimized to give maximum
4 surface area, depending on whether they can be fabricated by traditional photolithography and
5 nanoimprint lithography with acceptable defect levels.

6 **[00211]** To isolate the nanowires for each DRAM cell, an SOI (silicon-on-insulator) substrate
7 can be used, where the insulator acts as an etch stop for CICE and it isolates the individual
8 nanowires. Alternatively, the base of the nanowires can be made porous using electric fields.
9 Selective oxidation of the porous base can then be performed to electrically insulate the
10 nanowires.

11 **[00212]** Figs. 25A-25B illustrate two process flows for CICE wet anisotropic etch to create
12 high aspect ratio pillars without collapse according to one or more embodiments of the present
13 technology. Fig. 25A depicts a method of collapse prevention using ceilings to extend the
14 maximum aspect ratio that may be used. Collapse prevention using a ceiling can be done by
15 etching the features with plasma etching or SiSE to a short, stable height; depositing the ceiling,
16 and continuing the SiSE process. The "ceiling" can also be at a height that is along the length of
17 the short pillars, such as at $L/2$, where L is the height of the short stable pillar. This gives additional
18 support as the features are further etched and extends the maximum aspect ratio to greater than
19 that with the ceiling on top of the short pillars. This gives structural stability to the high aspect
20 ratio pillars and prevents collapse. The ceiling can be deposited by electron beam deposition at
21 an angle; polymer fill, etch back and ceiling deposition; or methods such as spin coating.
22 Materials that can be used for the ceiling include polymers, sputtered/deposited semiconductors,
23 metals and oxides that do not react with the CICE etchants, such as Cr, Cr_2O_3 , carbon, silicon,
24 Al_2O_3 , etc. In some embodiments, the ceiling can also be made porous by an additional low-
25 resolution lithography step or by a reaction to induce porosity to the ceiling material, for instance,
26 the ceiling material could be amorphous or poly-Si that becomes porous in the CICE etchant.
27 Once the substrate is etched and the catalyst can be removed, deposition of memory film or
28 dielectric filler by methods like atomic layer deposition can be done before removal of the porous
29 ceiling. The ceiling material could also be removed in certain areas or tuned to be non-selective
30 to Atomic Layer Deposition (ALD) thereby preventing the pores from closing and blocking the
31 deposition pathways. After filling the features, the ceiling is etched or polished away. ALD can
32 also be used to close off high-aspect ratio shapes after etch to create deep holes (e.g., apertures,
33 structural voids defined by lithography pattern, etc.) without the use of isolated catalysts.

1 **[00213]** Fig. 25B shows a links-based method of ensuring stability of etched nanostructures
2 with a diamond-shaped cross-section. If the catalyst mesh comprises both lithographic links and
3 gaps, then a linked structure is created by etching. Fig. 26 illustrates a SEM image showing
4 collapse of unsupported features vs supported features after CICE on silicon according to one or
5 more embodiments of the present technology. Fabrication of sub-30nm features with even
6 smaller link connections is extremely challenging, as electron beam lithography can write sub-
7 10nm features but suffers from large overlay, whereas photolithography has superior overlay but
8 poor resolution. Photolithography and imprint lithography (whose masks and templates are made
9 with electron beam lithography) may be used to get the final linked structure that can then be
10 made into a nanoimprint template.

11 **[00214]** In an alternate embodiment, holes can be etched with CICE to create trench
12 capacitor DRAM cells. This architecture can also be designed to be a $4F^2$ layout to minimize area
13 occupied by the DRAM cells. Since the vertical sidewall angle is greater than 89.5° for CICE
14 processes, center-to-center distance between holes can be sub-20nm, sub-15nm, sub-10nm, etc.
15 The arrangement of holes can be hexagonal to create more compact DRAM cells. To enhance
16 etchant diffusion in the holes, electric fields can be used to create one or more layers of porosity
17 along the length of the etched holes, except for the top region. The non-porous top region can
18 be used to create a silicon transistor for the DRAM cell. The one or more porous layers can be
19 selectively oxidized to electrically isolate the trench capacitors. The pores created in the layers of
20 porosity can be sealed after the CICE process using atomic layer deposition of insulating material
21 such as SiO_2 , SiN , SiON etc. Trench capacitors can be created in the high aspect ratio holes by
22 depositing capacitor material such as electrodes (poly-Si, W, TiN , Co, TaN) and high-k dielectrics
23 (HfO_2 , ZrO_2 , Al_2O_3) to create MOS (metal-oxide-semiconductor), MIM (metal-insulator-metal) or
24 MIMIM etc. configuration capacitors.

25 **TRANSISTORS**

26 **[00215]** CMOS scaling has been employed in the semiconductor industry to improve chip
27 performance, reduce power consumption and enhance functionality, typically by increasing the
28 transistor density. This scaling occurs by releasing a new technology node every 18 months to 2
29 years. Transistor density is increased by reducing the dimensions of the transistors such as gate
30 lengths, gate oxide thickness, spacer thickness etc. As the feature sizes decreased, new
31 technologies such as high-k dielectrics, metal gates, strain engineering and low-k spacer
32 dielectrics have been employed with planar or recessed transistors. However, to improve
33 electrostatics despite reduce area per transistor, 3D scaling in the form of FinFETs was introduced.

1 The process of making tall, thin fins with minimal sidewall damage and no collapse has been
2 challenging as the dimensions reduced to sub-20nm. For sub-10nm nodes, innovative methods
3 of improving electrostatics using horizontal nanosheets and nanowires has been proposed.

4 **[00216]** However, for all of these 3D geometries, the stability of the structures coupled with
5 the fabrication challenges has limited the potential of the technology. Taller fins and/or increased
6 number of stacked nanosheets and nanowires can improve the performance of chips and enable
7 scaling for many technology nodes. However, plasma etching for fabrication of fins suffers from
8 etch taper and sidewall damage that affects device performance. High aspect ratio fins with low
9 sidewall damage having sub-10nm critical dimension can be achieved with CICE by eliminating
10 etch taper and thereby decreasing the number of fins required per transistor. Large area control
11 and inline metrology will be incorporated for wafer scale fabrication of the first level of transistors
12 of optimized cross-sections ranging from rectangular fins to circular and shaped NWs. Various
13 embodiments include a novel etch technique, Catalyst Influenced Chemical Etching (CICE) and
14 lithography requirements to enable making high aspect ratio fins with vertical sidewalls with no
15 plasma damage.

16 **[00217]** CICE is a catalyst based etching method that can be used on semiconductors such
17 as Si, Ge, $\text{Si}_x\text{Ge}_{1-x}$, GaN, InP, GaAs, InAs, GaP, InGaS, InGaP, SiC etc. as well as multilayers of
18 the semiconductors. An electric field may or may not be used in conjunction with the catalyst for
19 the etch. An etchant (such as Hydrofluoric acid HF), an oxidant (such as Hydrogen peroxide
20 H_2O_2), and optionally a low surface tension liquid (such as Ethanol) and DI water can etch
21 semiconducting substrates preferentially at the location of a catalyst (such as Ag, Au, Pd, Pt, Ru,
22 Cu, W, TiN, TaN, RuO_2 , IrO_2 , Graphene etc.). Non-aqueous etchants can also be used if needed.
23 Lithography techniques (such as photolithography, electron beam lithography, double patterning,
24 quad patterning, nanoimprint- lithography etc.) are used to define the catalyst features. The
25 resulting substrate with the catalyst mesh is placed in an etchant solution and etched precisely to
26 a certain depth actively controlled by electrical fields and optical imaging systems that can
27 determine the etch depth based on the electrical and optical properties during etch.

28 **[00218]** The final device thus is a finFET with high aspect ratio fins having an aspect ratio >
29 5:1, where the fin structure is extremely vertical and has an angle of $>89.5^\circ$ which is measured
30 using a scanning electron microscope (SEM), TEM, AFM, etc. and then using an image analysis
31 software such as ImageJ. The average taper angle is measured using a straight line
32 approximately conformal using a linear-fit algorithm between any difference in the feature size of
33 the top and bottom of the critical feature. The critical dimensions can be the width of the fin or the

1 width of the trenches between the fins. Since the vertical sidewall angle is greater than 89.5° for
 2 CICE processes, center-to-center distance between critical features such as the fin spacing and
 3 fin width can be sub-20nm, sub-15nm, sub-10nm, etc.

4 **[00219]** In the case of lateral nanowire and nanosheet FETs, the fins are composed of
 5 alternating layers of material, where one of the layers is selectively removed and a dielectric and
 6 gate electrode are conformally deposited to surround the suspended lateral nanowires or
 7 nanosheets. The taper of the nanosheet and lateral nanowire FETs are also measured similar to
 8 the finFETs.

9 **[00220]** Plasma etching for fabrication of fins has a variety of process challenges such as
 10 precision etching, etch taper, collapse, erosion and structural integrity, and sidewall damage. This
 11 affects device performance of the transistors. High aspect ratio and low sidewall damage for sub-
 12 10nm critical dimension fins can be achieved with CICE. The etch taper angle creates further
 13 challenges as it limits the maximum height of the fin at a certain fin width. To increase the height
 14 of the fin, the width of the fin has to be increased, which reduces the transistor packing density.

15 **[00221]** Fig. 27A illustrates a 14nm FinFET with a taper angle of ~85°, and a physical Half
 16 Pitch (HP) of 24nm used in industry. The maximum fin height that can be achieved with such a
 17 taper angle is calculated by $Maximum\ fin\ height = 0.5 * HalfPitch * \tan(TaperAngle)$. By
 18 improving the taper angle, the maximum fin height can be increased for different fin widths and
 19 half pitches (HP). This relationship is plotted in Fig. 27B, showing the maximum height of a fin
 20 that can be etched for a given HP vs. the etch taper angle. This shows the scaling potential for
 21 etch processes that have no taper, such as CICE. This does not consider the structural stability
 22 of fins, which is examined later. 100nm of the fin height is used for Shallow Trench Isolation (STI)
 23 and is thus not a part of the active finFETs.

24 **[00222]** High aspect ratio fins are susceptible to collapse. Collapse of the fins can be
 25 mitigated using connecting links that can be modified or removed once the transistors are made
 26 and the fins are embedded in stabilizing material such as an insulator.

27 **[00223]** Fig. 28 is a plot illustrating a maximum height of a fin with no taper before lateral
 28 collapse along the length of the fin (50nm in this case), without any support/assist features. The
 29 critical height of a fin that is unsupported by any connecting links, for a length of 50nm, is shown
 30 vs its half pitch in Fig. 28. This is calculated by equating the bending energy of the fin due to
 31 collapse with the surface energy required to separate the fins:

$$32 \quad h_{cr_lengthwise} = (18EI_x w^2 / \gamma_{sv} b)^{(1/4)}$$

$$h_{cr_widthwise} = (18EI_y w^2 / \gamma_{sv} a)^{1/4}$$

where E is the elastic modulus of the fin, I is the moment of inertia about the bending axis, w is the deflection of the fin, i.e. half the distance between the collapsing fins, γ_{sv} is the surface energy of the fin material, and a and b are the dimensions of the fin perpendicular to the direction of collapse (lengthwise vs widthwise).

[00224] The collapse occurs along the length of the fin at the shortest height, and is thus the height that is depicted in the graph. Although fins can be much longer based on specific circuit designs, the shortest length of a fin is determined by the contact gate pitch (CGP) of the finFET. For a minimum spacer thickness (t_s) ~5nm and source/drain (S/D) contact length (L_C)~15nm, the contact gate pitch CGP= $L_G + 2t_s + L_C$. This shows that scaling of the transistor depends on the gate length L_G which can vary between 10-25nm. An example case of 50nm is considered to determine the maximum height of a fin of different widths before it collapses laterally onto another fin. A fin pitch of double the fin width is taken as some embodiments can shrink the fin pitch due to no etch taper.

[00225] A major limitation to scaling to smaller fin widths is their structural instability. For FinFETs made with bulk silicon, a major portion of their length is utilized for shallow trench isolation (STI). Assuming the minimum height required for STI is 100nm, only fins of width 10nm and above can be used. Further, the active portion of the fins are much shorter than the initial fin height. This can be alleviated in part by using SOI wafers. However, even in case of SOI finFETs there is a limitation to the maximum height achievable for a fin. An etch taper helps in improving the structural stability of a fin to a certain extent, but eventually limits the maximum height possible as was described in Fig. 27.

FinFET Process Flow

[00226] Various embodiments improve the structural stability of the fins by using connecting links between them to stabilize the fins during and after etch. After further processing of the device, the stabilizing structures are removed or modified. In one embodiment, the connecting links can also be used in the circuit design phase to link sources and drains of adjacent finFETs alongside epitaxial S/D contact formation. An example of a process flow for a finFET is shown in Fig. 29.

1 **[00227]** An embodiment of the CICE finFET process flow is illustrated in Fig. 29, where the
2 process steps are: a) CICE of connected fins and subsequent catalyst material removal; b) STI
3 (Shallow Trench Isolation) fill and etchback, which may involve using Atomic Layer deposition
4 (ALD) of STI material and etch back of the STI material using Vapor HF, Atomic Layer Etching
5 (ALE) or Reactive Ion Etching (RIE). c) Dummy Gate and Spacer patterning and deposition,
6 where Poly silicon is used as a dummy gate and silicon nitride is used as spacers on either side
7 of the dummy gates; d) Oxide fill using ALD and planarization using Chemical Mechanical
8 Polishing (CMP), cut/etch away connecting features (or links), where the connecting features
9 between the fins are etched away using RIE, ALE, selective oxidation and vapor HF etch, etc.
10 and the lithographic mask for etching away the connecting features can be designed to retain
11 certain connections based on the number of fins per transistor and the transistor circuit design.
12 e) Oxide fill and etch back; f) Source/Drain deposition using epitaxial growth of Si or Si and Ge
13 with in-situ doping; and g) Metal Gate replacement and High-k dielectric deposition, where the
14 dummy gate can then be replaced with high-k dielectrics and metal gates between the spacers to
15 form the final high aspect ratio finFETs.

16 **[00228]** In another embodiment, catalyst connecting links may be used in the regions of the
17 fins and the missing portions can be joined using epitaxial growth of silicon. For regions where
18 the connecting links are removed, depending on the location and circuit design, material such as
19 TiN, W, SiO₂, SiN, carbon, Si, Ge, etc. may be deposited based on the required electrical
20 properties of the material, e.g. whether the connection needs to be conducting, insulating, or
21 semiconducting.

22 **[00229]** High Aspect Ratio FinFETs fabricated with CICE have connecting links between the
23 fins to prevent collapse. These links have to be removed during the fabrication process (Fig. 29
24 step (d)) to obtain the required fin design. In one embodiment, the finFET links are removed by
25 first patterning and deposition of dummy gate and spacers after CICE followed by deposition of
26 dielectric in all exposed regions. Photolithography is then done to isolate regions of fin-links that
27 need to be removed, and the fin-links are removed using atomic layer etching, plasma etching
28 etc. Any plasma etch taper that is created during the etch will not affect the fin structures protected
29 by the dummy gate and spacers, and subsequent S/D epitaxy steps may replenish any lost fin
30 material due to plasma etch taper. Alternatively, selective oxidation and removal of the exposed
31 fin-links can be done, and the oxidized fin-links can be removed using vapor HF, plasma etching,
32 wet etching to remove silicon oxide instead of silicon, thereby protecting the silicon fins due to the
33 selective nature of the silicon oxide etch.

1 **[00230]** This method has the advantage of very precise overlay of < 2nm, thereby ensuring
 2 that excess material is not removed from the fins. Spacer patterning can be used to decrease the
 3 width and pitch from a photolithography resolution of 35-40nm line/spaces to 20-25nm line/spaces.
 4 To create cuts both parallel to the fins and perpendicular to the fins, two photolithography steps
 5 can be used with line/spaces at 90 degrees to each other. EUV lithography can be used to create
 6 the same features without additional spacer patterning. Based on the finFET designs for logic
 7 devices, the catalyst pattern for etching of the fins and their connecting links will be designed. For
 8 example, in Fig. 32, the starting CICE catalyst pattern and the pattern after removal of connecting
 9 links is shown.

10 **[00231]** Figs. 30A-30E illustrates an example of FinFET process after CICE according to
 11 one or more embodiments of the present technology. More specifically, Figs. 30A-30E show a
 12 top view of connected fin structures, whose design depends on the application of the finFETs,
 13 such as in SRAM and logic circuitry. In Fig. 30A, the structures etched with CICE are connected
 14 to prevent collapse. Fig. 30B depictS dummy gate and spacer patterns which are designed to
 15 connect multiple fins as needed by the circuit design. In Fig. 30C, lithography is used to expose
 16 the portions to be etched away (connecting links). In Fig. 30D, connecting links are then etched
 17 away using Atomic Layer Etching or Plasma Etching. Further finFET processing steps (not shown
 18 in Fig. 30A-30E) such as Source/Drain epitaxial deposition, gate replacement, and the like can
 19 then be performed to get the final device circuitry. Fig. 30E shows a schematic of underlying fins
 20 in part D that remain after all the finFETs processing steps.

21 **[00232]** Nanosheet FETs are made by etching fins that have alternating layers of
 22 semiconductor material and subsequently removing one of the alternating layers, resulting in
 23 suspended nanosheets. Nanosheet FETs have better electrostatics than finFETs due to their
 24 gate-all-around configuration as opposed to finFET's trigate structure. Similar to the height
 25 limitations of fins discussed in the previous section, the critical height of the alternating layers of
 26 semiconductor in the nanosheet fins limits the number of layers that can be etched using plasma
 27 etching. This limitation is not present in the SiSE process, a subset of CICE which produces
 28 nanostructures with alternating layers instead of bulk-Si. An embodiment of the nanosheet layers
 29 comprises Si and Si_xGe_{1-x}, wherein the new critical height depends on the modified elastic
 30 modulus of the multilayer stacked fins. Considering the thickness of each nanosheet to be 5nm,
 31 and the lower region of the fin that is covered by STI to be Si, the effective elastic modulus can
 32 be calculated by the "slab" model using the inverse rule of mixtures in composites: $\frac{1}{E_{eff}} = \frac{V_f}{E_f} + \frac{V_m}{E_m}$,
 33 where E is the elastic modulus and V is the volume fraction, subscript f denotes the sacrificial

1 nanosheet material, e.g. $\text{Si}_x\text{Ge}_{1-x}$ or porous Si and m is the remaining nanosheet material, e.g.,
2 Si.

3 **[00233]** For a volume fraction of Si ~ 75%-95%, the resulting effective elastic modulus is ~
4 100-150GPa, and the critical heights for nanosheet fins are similar to those of finFET fins. The
5 change in surface energy depends on the material of the surface at the top of the fins that is in
6 contact. In one embodiment, that material is silicon and the influence of the material of the
7 nanosheet is the same as that of a silicon finFET.

8 **[00234]** Alternatively, lateral nanowire FETs can be made in a similar way by reducing the
9 width of the fin. In the SiSE process, the connected fins that are formed for finFETs using
10 lithographic links can also be used on a stack of alternating layers of semiconductors.

11 **[00235]** Nanosheet FETs are similar to finFETs with the fins having alternating layers of
12 material instead of bulk silicon. One embodiment comprises alternating layers of Si and $\text{Si}_x\text{Ge}_{1-x}$,
13 where the $\text{Si}_x\text{Ge}_{1-x}$ layer is removed to give silicon nanosheets. Another embodiment consists of
14 alternating layers of differently doped Si, which produces sacrificial porous Si layers and
15 crystalline Si nanosheets. In a further embodiment, protective layers between the alternating
16 layers are used to ensure the silicon nanosheets are unaffected by sacrificial nanosheet etch,
17 such as by using an alternating stack of low-doped Si/ $\text{Si}_x\text{Ge}_{1-x}$ /high-doped Si/ $\text{Si}_x\text{Ge}_{1-x}$ or low-
18 doped Si/ Ge /high-doped Si/ Ge, where the high-doped Si is converted to porous Si and low-
19 doped Si remains crystalline. SiSE process is tuned to ensure that the morphology changes from
20 porous to non-porous at a specific doping concentration, creating a multilayer stack of porous and
21 non-porous Si. The porous Si can be selectively removed resulting in suspended nanosheets of
22 Si. The etchant composition as well as hole-generation during the process results in alternating
23 films of differing morphologies based on their material and doping concentrations. In another
24 embodiment, the SiSE process is used with a time-varying electric field on bulk Si to create
25 nanosheet fins with alternating layers of porous and non-porous Si. An exemplar process flow is
26 described in Fig. 31.

27 **[00236]** Fig. 31 illustrates an example of a process flow for making nanosheet FETs and
28 lateral nanowire FETs with SiSE according to one or more embodiments of the present technology.
29 The steps include a) SiSE of connected fins and removal of catalyst material; b) Dielectric fill to
30 create STI (Shallow Trench Isolation) using Atomic Layer deposition (ALD); c) Cut/etch away
31 connecting features, where the connecting features between the fins are etched away using RIE
32 or ALE, and the lithographic mask for etching away the connecting features can be designed to
33 retain certain connections based on the number of fins per transistor and the transistor circuit

design; d) deposition of stress liner such as silicon nitride in the cut away areas using ALD; e) dielectric (STI) etch back and selective removal of alternating layers to get suspended nanosheets/nanowires; f) dummy gate and spacer patterning and deposition, where poly-silicon is used as a dummy gate and silicon nitride is used as spacers on either side of the dummy gates. A spacer can be deposited around dummy gate, excess spacer material can be patterned/etched and oxide fill and planarization can be performed; g) S/D deposition where Source and Drain regions are then deposited using epitaxial growth of Si or Si and Ge with in-situ doping; and h) metal gate replacement and High-k dielectric deposition.

[00237] In another embodiment of SiSE for nanosheet FETs, time-varying electric fields can be used along with the catalyst etch to create alternating layers of porous and non-porous Si by using bulk Si instead of alternating epitaxial layers of material as the starting substrate.

[00238] The selective removal of alternating layers of the nanosheets is done using a selective etch process. For example, in a stack of Si/ $\text{Si}_x\text{Ge}_{1-x}$, HCl may be used to selectively remove the $\text{Si}_x\text{Ge}_{1-x}$. In a stack of Si/Porous-Si, etchants such as HF, TMAH, vapor HF, HF and a weak oxidant such as Hydrogen peroxide, etc. can be used. In stacks with multiple alternating materials such as low-doped Si/ $\text{Si}_x\text{Ge}_{1-x}$ /high-doped (porous after CICE) Si/ $\text{Si}_x\text{Ge}_{1-x}$, HF can be used to remove the porous Si and then HCl is used to remove the $\text{Si}_x\text{Ge}_{1-x}$.

[00239] The catalyst is designed for prevention of collapse such that all fins are connected using lithographic links. To further prevent wandering of catalyst in cases where the wandering cannot be suppressed using SiSE and/or electric fields, connected links are made with lithographic links connecting all the catalyst regions while ensuring that all the fins are connected to prevent collapse.

[00240] The critical height of a fin before collapse can be increased by using connecting links at the ends of the fins near the S/D regions. These links can later be removed after stabilizing the fin with gates, spacers and insulating material. Fig. 32 plots the critical heights before lateral collapse for different number of fins along the length and width of the fin structures. For a contact gate pitch (CGP) of 50nm, connecting links of 10nm width are used on both sides of the fins to improve stability. The maximum height of the fins when all of the fins are connected to each other in a square mesh as shown in Fig 32 can be simulated as a thin long plate with 3 fixed sides.

[00241] Fig. 32A provides an illustration of connecting links when number of fins > 1 . For $N=1$, the length b equals the CGP of the finFETs, whereas for $N>1$ the length $b=\text{CGP}+2*(\text{link width})$. In Fig. 32B, the critical heights before collapse along the length of the connected fin

1 structure is shown for different fin widths f and for number of fins ranging from 1 to 10. In Fig.
2 32C, the critical heights before collapse along the width of the connected fin structure is shown
3 for different fin widths f and for number of fins ranging from 1 to 10. To prevent wandering of the
4 catalyst in larger blocks of connected fins, a linked mesh can be utilized as shown below for a
5 block of 6x4 fins. Multiple blocks may be completely separated or connected via links of
6 semiconductor. 32D is a plot illustrating the critical heights before collapse along the width of the
7 connected fin structure is shown for different fin widths f and for number of fins ranging from 1 to
8 10.

9 **[00242]** To create devices from the connected fins etched using CICE, one of the critical
10 steps is dielectric etch back to create shallow trench isolation (STI) regions at the base of fins.
11 This step is necessary for all embodiments of this process other than for SOI (silicon-on-insulator)
12 wafers. The dielectric, such as SiO_x, can be deposited on the high aspect ratio fins of width <
13 15nm using conformal deposition methods such as atomic layer deposition. Timed etch back of
14 the dielectric should ideally create ~100nm thick STI at the base of the fins while not affecting the
15 fins themselves. Plasma etching is typically used for this process. However, the physical
16 component of the plasma etching process can damage the fins. Vapor HF can be used for a
17 purely chemical process to etch back the dielectric without damaging the fins. In one embodiment,
18 a separate material (such as silicon nitride) can be deposited using ALD around the fins before
19 the oxide dielectric deposition. This will create an etch stop on the fins and prevent any damage
20 in a selective chemical etch.

21 **[00243]** The uniformity of such etch-back processes from center-to edge of the wafer needs
22 to be controlled. This can be done using multiple temperature zones in a vapor HF setup. A "send
23 ahead" wafer can be used to optimized the timed etch and map the various regions with
24 discontinuities in the etch rate and depth. The discontinuities can be smoothened by creating local
25 high and low temperature zones to modify the local etch rate to create uniform etch depths.

26 **[00244]** Alternatively, a silicon containing polymer can be dispensed using inkjets precisely
27 on locations with high etch rates, such as the edge of the wafers. The dispensed volumes can
28 be determined using the data from the send-ahead wafers. The substrate is then baked at an
29 optimized temperature to create intentional non-uniform heights of material on the substrate. This
30 will cancel out non-uniform etching by Vapor HF, and thus ensure that the final etch uniformity for
31 creating STI in fins is within specifications.

32 **[00245]** In another embodiment, the bulk Si fins in finFETs and the nanosheet fins in
33 nanosheet FETs can be electrically isolated from each other by creating a porous bottom layer

1 during the SiSE process using electric fields, etchant concentrations and/or doping concentration
2 of the layer to be etched such that the layer becomes porous after the etch. The porous bottom
3 layer may be 100nm thick. The porous layer is then selectively oxidized to create oxidized porous
4 Si at the bottom of the fins which thereby act as Shallow Trench isolation (STI) and electrically
5 isolate the fins. For nanosheet FETs, the alternating porous layers may also be oxidized when
6 the bottom porous layer is oxidized.

7 **[00246]** Various embodiments of the present technology provide techniques for
8 manufacturing FinFETs. For example, in some embodiments, the catalyst can be patterned using
9 lithography, depositing a discontinuous catalyst such as Pt, Pd, Ru, Au, etc. and performing
10 Chemical Mechanical Polishing or Lift-off. Alternatively, selective electrodeposition of catalyst can
11 be done after lithography. After the SiSE process, the catalyst material can be removed using
12 wet etching (e.g. with aqua regia) or it can be isolated from the device layers using an insulator.
13 To create an STI layer, an insulator can be deposited and planarized. Lithography and etch of
14 excess fin connecting structures can then be performed. Then, lithography and deposition of
15 stress liner material can be performed. An etch-back to get shallow trench isolation (STI) may be
16 performed if needed using methods such as timed vapor HF etch. For nanosheet transistors,
17 selective removal of alternating layers to get suspended nanosheets is performed. For example,
18 some embodiments may etch $\text{Si}_x\text{Ge}_{1-x}$ selective to Si, and/or etch porous Si selective to Si. A
19 dummy gate can then be patterned. For example, in some embodiments, lithography for dummy
20 gate pattern may be performed and dummy gate material (oxide, poly-Si) may be deposited. A
21 spacer can be deposited around the dummy gate and pattern/etch excess spacer material. An
22 oxide fill and etch back may be performed. In some embodiments, lithography can be used to
23 expose for S/D region. Then, S/D deposition (e.g. doped epi growth) may be performed. The
24 poly-Si dummy gate can be etched away and replaced with a high-k dielectric and metal gate. An
25 insulator, such as silicon oxide can then be deposited and planarized to complete fabrication of
26 the transistor layers. Further processing is then done to create metal layer contacts, thereby
27 creating a working transistor device, and an oxide fill and planarization of the metal layers can be
28 completed.

29 Conclusion

31 **[00247]** Unless the context clearly requires otherwise, throughout the description and the
32 claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense,
33 as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not

1 limited to." As used herein, the terms "connected," "coupled," or any variant thereof means any
2 connection or coupling, either direct or indirect, between two or more elements; the coupling or
3 connection between the elements can be physical, logical, or a combination thereof. Additionally,
4 the words "herein," "above," "below," and words of similar import, when used in this application,
5 refer to this application as a whole and not to any particular portions of this application. Where
6 the context permits, words in the above Detailed Description using the singular or plural number
7 may also include the plural or singular number respectively. The word "or," in reference to a list
8 of two or more items, covers all of the following interpretations of the word: any of the items in the
9 list, all of the items in the list, and any combination of the items in the list.

10 **[00248]** The above Detailed Description of examples of the technology is not intended to be
11 exhaustive or to limit the technology to the precise form disclosed above. While specific examples
12 for the technology are described above for illustrative purposes, various equivalent modifications
13 are possible within the scope of the technology, as those skilled in the relevant art will recognize.
14 For example, while processes or blocks are presented in a given order, alternative
15 implementations may perform routines having steps, or employ systems having blocks, in a
16 different order, and some processes or blocks may be deleted, moved, added, subdivided,
17 combined, and/or modified to provide alternative or subcombinations. Each of these processes
18 or blocks may be implemented in a variety of different ways. Also, while processes or blocks are
19 at times shown as being performed in series, these processes or blocks may instead be performed
20 or implemented in parallel, or may be performed at different times. Further any specific numbers
21 noted herein are only examples: alternative implementations may employ differing values or
22 ranges.

23 **[00249]** The teachings of the technology provided herein can be applied to other systems,
24 not necessarily the system described above. The elements and acts of the various examples
25 described above can be combined to provide further implementations of the technology. Some
26 alternative implementations of the technology may include not only additional elements to those
27 implementations noted above, but also may include fewer elements.

28 **[00250]** These and other changes can be made to the technology in light of the above
29 Detailed Description. While the above description describes certain examples of the technology,
30 and describes the best mode contemplated, no matter how detailed the above appears in text,
31 the technology can be practiced in many ways. Details of the system may vary considerably in
32 its specific implementation, while still being encompassed by the technology disclosed herein. As
33 noted above, particular terminology used when describing certain features or aspects of the

1 technology should not be taken to imply that the terminology is being redefined herein to be
2 restricted to any specific characteristics, features, or aspects of the technology with which that
3 terminology is associated. In general, the terms used in the following claims should not be
4 construed to limit the technology to the specific examples disclosed in the specification, unless
5 the above Detailed Description section explicitly defines such terms. Accordingly, the actual
6 scope of the technology encompasses not only the disclosed examples, but also all equivalent
7 ways of practicing or implementing the technology under the claims.

8 **[00251]** To reduce the number of claims, certain aspects of the technology are presented
9 below in certain claim forms, but the applicant contemplates the various aspects of the technology
10 in any number of claim forms. For example, while only one aspect of the technology is recited as
11 a computer-readable medium claim, other aspects may likewise be embodied as a computer-
12 readable medium claim, or in other forms, such as being embodied in a means-plus-function claim.
13 Any claims intended to be treated under 35 U.S.C. § 112(f) will begin with the words "means for",
14 but use of the term "for" in any other context is not intended to invoke treatment under 35 U.S.C.
15 § 112(f). Accordingly, the applicant reserves the right to pursue additional claims after filing this
16 application to pursue such additional claim forms, in either this application or in a continuing
17 application.