## ABSTRACT

**SYSTEM AND METHOD OF CONTROLLING POWER IN A MULTI-THREADED PROCESSOR**

A multithreaded processor device is disclosed and includes a plurality of execution units to execute a plurality of program threads and includes a global low power detection circuit. The global low power detection circuit includes an input that is responsive to each of the plurality of program threads. The input indicates an execution activity level for each of the plurality of program threads. The global low power detection circuit further comprises logic to evaluate the activity level of each of the plurality of program threads. The logic provides a power level signal. Additionally, the global low power detection circuit includes an output that is responsive to the power level signal. The output is coupled to one or more global resources within the multithreaded processor and the output selectively controls an amount of power provided to the one or more global resources.

Figure 1