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Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a
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- *as to the applicant's entitlement to claim the priority of the
earlier application (Rule 4.17(iii))*

- (54) **Title:** SEQUENTIAL READ OPTIMIZATION IN A MEMORY SUB-SYSTEM THAT PROGRAMS SEQUENTIALLY

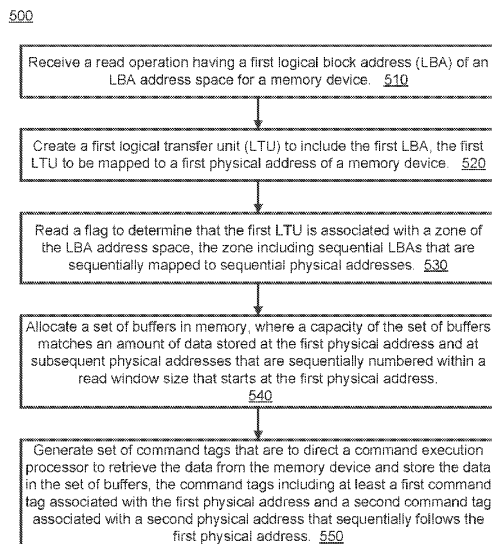


FIG. 5

(57) **Abstract:** A system includes a volatile memory having buffers and a processing device. A command generation processor receives, from a host, a read request with a logical block address (LBA) and creates a first logical transfer unit (LTU), including the first LBA, that is to be mapped to a physical address. The command generation processor reads a flag to determine that the first LTU is associated with a zone of LBA address space, the zone including sequential LBAs that are sequentially mapped to sequential physical addresses. The command generation processor generates command tags that are to direct the processing device to retrieve the data from the memory device and store the data in a set of the buffers, where the command tags include a first command tag associated with the physical address and a second command tag associated with a second physical address that sequentially follows the physical address.

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