CLAIMS

1. A semiconductor device comprising:

a first transistor;

a second transistor over the first transistor, the second transistor including a source electrode and a drain electrode; and

a contact plug penetrating one of the source electrode and the drain electrode of the second transistor so as to reach the first transistor,

wherein the first transistor and the one of the source electrode and the drain electrode of the second transistor overlap with each other.

2. The semiconductor device according to claim 1,

wherein a channel formation region of the first transistor includes silicon, and

wherein a channel formation region of the second transistor includes an oxide semiconductor.

3. The semiconductor device according to claim 1,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and one of the source and the drain of the first transistor overlap with each other, and

wherein the contact plug is electrically connected to the one of the source and the drain of the first transistor and the one of the source electrode and the drain electrode of the second transistor.

4. The semiconductor device according to claim 1,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and the gate of the first transistor overlap with each other, and

wherein the contact plug is electrically connected to the gate of the first transistor and the one of the source electrode and the drain electrode of the second transistor.

5. The semiconductor device according to claim 1, further comprising:

a first insulating layer between the first transistor and the second transistor; and

a second insulating layer over the second transistor,

wherein the contact plug penetrates the first insulating layer, the one of the source electrode and the drain electrode of the second transistor, and the second insulating layer so as to reach the first transistor.

6. The semiconductor device according to claim 5, wherein in a depth direction from the second insulating layer to the first insulating layer, a diameter of the contact plug changes to a smaller value at an interface between the second insulating layer and the one of the source electrode and the drain electrode of the second transistor.

7. The semiconductor device according to claim 1, wherein the contact plug penetrates a semiconductor layer of the second transistor.

8. A method for manufacturing a semiconductor device comprising the steps of:

forming a conductive film over a first insulating layer;

selectively etching the conductive film to form a conductive layer and a first opening penetrating the conductive layer;

forming a second insulating layer over the conductive layer so that the second insulating layer covers the first opening; and

selectively etching the second insulating layer to form a second opening so as to etch the second insulating layer in the first opening,

wherein the first opening and the second opening overlap with each other.

9. The method according to claim 8, further comprising the step of:

selectively etching the first insulating layer using the conductive layer as a mask.

10. The method according to claim 8, further comprising the step of:

forming a contact plug in the first opening and the second opening, the contact

plug electrically connected to the conductive layer.

11. The method according to claim 8, further comprising the steps of:

forming a semiconductor layer including a channel formation region of a transistor;

forming a gate insulating layer over the semiconductor layer; and

forming a gate electrode over the gate insulating layer, the gate electrode overlapping with the semiconductor layer,

wherein the conductive layer is one of a source electrode and a drain electrode of the transistor, and the conductive layer is electrically connected to the semiconductor layer.

12. The method according to claim 11, wherein a third opening is formed in the second insulating layer so that the third opening reaches the gate electrode in the step of selectively etching the second insulating layer.

13. The method according to claim 11, wherein the semiconductor layer includes an oxide semiconductor.

14. A method for manufacturing a semiconductor device comprising the steps of:

forming a first transistor;

forming a first insulating layer over the first transistor;

forming a semiconductor layer of a second transistor over the first insulating layer;

forming a conductive film over the first insulating layer;

selectively etching the conductive film to form a source electrode of the second transistor, a drain electrode of the second transistor, and a first opening penetrating one of the source electrode and the drain electrode of the second transistor;

forming a second insulating layer over the second transistor so that the second insulating layer covers the first opening; and

selectively etching the first insulating layer to form a second opening reaching

the first transistor, and selectively etching the second insulating layer to form a third opening so as to etch the second insulating layer in the first opening,

wherein the first opening, the second opening, and the third opening overlap with one another.

15. The method according to claim 14, further comprising the step of:

forming a contact plug in the first opening, the second opening, and the third opening, the contact plug electrically connected to the one of the source electrode and the drain electrode of the second transistor.

16. The method according to claim 14, wherein a fourth opening is formed in the second insulating layer so that the fourth opening reaches a gate electrode of the second transistor in the step of selectively etching the second insulating layer.

17. The method according to claim 14,

wherein a semiconductor layer of the first transistor includes silicon, and

wherein the semiconductor layer of the second transistor includes an oxide semiconductor.

18. The method according to claim 14,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and one of the source and the drain of the first transistor overlap with each other, and

wherein the second opening reaches the one of the source and the drain of the first transistor.

19. The method according to claim 14,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and the gate of the first transistor overlap with each other, and

wherein the second opening reaches the gate of the first transistor.

20. The method according to claim 14,

wherein a fourth opening is formed in the semiconductor layer of the second transistor, and

wherein the first opening and the fourth opening overlap with each other.

CLAIMS

1. A semiconductor device comprising:

a first transistor;

a first insulating layer over the first transistor;

a second transistor over the first insulating layer, the second transistor including a source electrode and a drain electrode; and

a second insulating layer over the second transistor; and

a contact plug penetrating one of the source electrode and the drain electrode of the second transistor so as to reach the first transistor through the first insulating layer and the second insulating layer,

wherein the first transistor and the one of the source electrode and the drain electrode of the second transistor overlap with each other, and

wherein a radius of a first part of the contact plug in the second insulating layer is larger than a radius of a second part of the contact plug in the first insulating layer.

2. The semiconductor device according to claim 1,

wherein a channel formation region of the first transistor includes silicon, and

wherein a channel formation region of the second transistor includes an oxide semiconductor.

3. The semiconductor device according to claim 1,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and one of the source and the drain of the first transistor overlap with each other, and

wherein the contact plug is electrically connected to the one of the source and the drain of the first transistor and the one of the source electrode and the drain electrode of the second transistor.

4. The semiconductor device according to claim 1,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and the gate of the first transistor overlap with each other, and

wherein the contact plug is electrically connected to the gate of the first transistor and the one of the source electrode and the drain electrode of the second transistor.

5. The semiconductor device according to claim 1, further comprising:

a first insulating layer between the first transistor and the second transistor; and

a second insulating layer over the second transistor,

wherein the contact plug penetrates the first insulating layer, the one of the source electrode and the drain electrode of the second transistor, and the second insulating layer so as to reach the first transistor.

6. The semiconductor device according to claim 5, wherein in a depth direction from the second insulating layer to the first insulating layer, a diameter of the contact plug changes to a smaller value at an interface between the second insulating layer and the one of the source electrode and the drain electrode of the second transistor.

7. The semiconductor device according to claim 1, wherein the contact plug penetrates a semiconductor layer of the second transistor.

8. A method for manufacturing a semiconductor device comprising the steps of:

forming a conductive film over a first insulating layer;

selectively etching the conductive film to form a conductive layer and a first opening penetrating the conductive layer;

forming a second insulating layer over the conductive layer so that the second insulating layer covers the first opening; and

selectively etching the second insulating layer to form a second opening so as to etch the second insulating layer in the first opening,

wherein the first opening and the second opening overlap with each other, and

wherein a radius of the second opening is larger than or equal to a radius of the first opening.

9. The method according to claim 8, further comprising the step of:

selectively etching the first insulating layer using the conductive layer as a mask.

10. The method according to claim 8, further comprising the step of:

forming a contact plug in the first opening and the second opening, the contact plug electrically connected to the conductive layer.

11. The method according to claim 8, further comprising the steps of:

forming a semiconductor layer including a channel formation region of a transistor;

forming a gate insulating layer over the semiconductor layer; and

forming a gate electrode over the gate insulating layer, the gate electrode overlapping with the semiconductor layer,

wherein the conductive layer is one of a source electrode and a drain electrode of the transistor, and the conductive layer is electrically connected to the semiconductor layer.

12. The method according to claim 11, wherein a third opening is formed in the second insulating layer so that the third opening reaches the gate electrode in the step of selectively etching the second insulating layer.

13. The method according to claim 11, wherein the semiconductor layer includes an oxide semiconductor.

14. A method for manufacturing a semiconductor device comprising the steps of:

forming a first transistor;

forming a first insulating layer over the first transistor;

forming a semiconductor layer of a second transistor over the first insulating layer;

forming a conductive film over the first insulating layer;

selectively etching the conductive film to form a source electrode of the second transistor, a drain electrode of the second transistor, and a first opening penetrating one of the source electrode and the drain electrode of the second transistor;

forming a second insulating layer over the second transistor so that the second insulating layer covers the first opening; and

selectively etching the first insulating layer to form a second opening reaching the first transistor, and selectively etching the second insulating layer to form a third opening so as to etch the second insulating layer in the first opening,

wherein the first opening, the second opening, and the third opening overlap with one another, and

wherein a radius of the third opening is larger than or equal to a radius of the second opening.

15. The method according to claim 14, further comprising the step of:

forming a contact plug in the first opening, the second opening, and the third opening, the contact plug electrically connected to the one of the source electrode and the drain electrode of the second transistor.

16. The method according to claim 14, wherein a fourth opening is formed in the second insulating layer so that the fourth opening reaches a gate electrode of the second transistor in the step of selectively etching the second insulating layer.

17. The method according to claim 14,

wherein a semiconductor layer of the first transistor includes silicon, and

wherein the semiconductor layer of the second transistor includes an oxide semiconductor.

18. The method according to claim 14,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the second transistor and one of the source and the drain of the first transistor overlap with each other, and

wherein the second opening reaches the one of the source and the drain of the first transistor.

19. The method according to claim 14,

wherein the first transistor includes a gate, a source, and a drain,

wherein the one of the source electrode and the drain electrode of the

second transistor and the gate of the first transistor overlap with each other, and

wherein the second opening reaches the gate of the first transistor.

20. The method according to claim 14,

wherein a fourth opening is formed in the semiconductor layer of the second transistor, and

wherein the first opening and the fourth opening overlap with each other.