

WHAT IS CLAIMED IS:

1. A mask layout for forming a semiconductor device, comprising:
an active mask pattern forming source and drain regions in a substrate;
a gate electrode mask pattern, disposed to overlap the active mask pattern, forming a gate electrode between the source region and the drain region;
a silicide blocking mask pattern comprising a body region and protruding regions extended from the body region, and disposed to overlap the gate electrode mask pattern and the active mask pattern to form a silicide blocking region in the gate electrode, the source region and the drain region; and
a contact mask pattern, disposed spaced apart from the silicide blocking mask pattern, forming a contact plug on the substrate,
wherein the silicide blocking mask pattern covers the gate electrode mask pattern and extends to the active mask pattern.
2. The mask layout for forming the semiconductor device of claim 1,
wherein the silicide blocking region formed in the gate electrode is larger than a silicide region formed in the gate electrode.
3. The mask layout for forming the semiconductor device of claim 1,
wherein the source region is simultaneously in contact with both a silicide region and the silicide blocking region.
4. The mask layout for forming the semiconductor device of claim 1,
wherein the protruding regions comprise:
a first protruding region disposed in the gate electrode and a portion of the source region to form a first protruding silicide blocking region; and
a second protruding region disposed in the gate electrode and a portion of the drain region to form a second protruding silicide blocking region.

5. The mask layout for forming the semiconductor device of claim 4, wherein the protruding regions further comprise:

a third protruding region protruded towards the drain region and disposed in contact with the second protruding region, and

wherein a horizontal width of the third protruding region is smaller than a horizontal width of the body region.

6. The mask layout for forming the semiconductor device of claim 1,

wherein the silicide blocking region is disposed from a top surface of the gate electrode and extends to a portion of a top surface of the source region.

7. A semiconductor device comprising:

an active region defining an isolation region, a source region, and a drain region in a substrate;

a gate electrode disposed, between the source region and the drain region, to overlap the active region; and

a gate silicide region and a silicide blocking region disposed on the gate electrode, the silicide blocking region comprising a body region and a plurality of protruding regions extended from the body region,

wherein a horizontal width of the body region is greater than a horizontal width of each protruding region.

8. The semiconductor device of claim 7,

wherein the plurality of protruding regions comprises:

a first protruding silicide blocking region disposed in the gate electrode and a portion of the source region; and

a second protruding silicide blocking region disposed in the gate electrode and a portion of the drain region.

9. The semiconductor device of claim 8,
wherein the plurality of protruding regions further comprises a third protruding silicide blocking region protruded towards the drain region, and
wherein the silicide blocking region is disposed in contact with the second protruding silicide blocking region.
10. The semiconductor device of claim 7,
wherein the body region is disposed to overlap the gate electrode, a portion of the source region, and a portion of the drain region.
11. The semiconductor device of claim 7, wherein the body region is disposed to overlap a portion of the gate electrode and the drain region.
12. The semiconductor device of claim 7, wherein an active mask pattern forms the source region and the drain region in the substrate.
13. The semiconductor device of claim 12, wherein a gate electrode mask pattern, disposed to overlap the active mask pattern, forms the gate electrode.
14. The semiconductor device of claim 13, wherein a silicide blocking mask pattern comprising a body region and protruding regions extended from the body region, and disposed to overlap the gate electrode mask pattern and the active mask pattern to form the silicide blocking region in the gate electrode, the source region, and the drain region.
15. The semiconductor device of claim 14, wherein the silicide blocking mask pattern covers the gate electrode mask pattern and extends to the active mask pattern.