

DISPLAY DEVICE AND METHOD FOR POWERING SAME
ABSTRACT

There is provided an SSD display device with reduced power consumption.

5 A selection circuit (400) consists of k selection blocks (410(1) to 410(k)). Each selection block consists of three thin-film transistors. The three thin-film transistors respectively have three phases of selection control signal (CT) provided to their gate terminals. A scanning period (T1) is
10 provided and followed by an idle period (T2). In the idle period (T2), the three thin-film transistors in each selection block are brought into ON state in accordance with selection control signals (CT) at an idle period frequency (f_{ck2}). The
15 idle period frequency (f_{ck2}) is lower than a scanning period frequency (f_{ck1}).

Fig. 5