

Brief description of the invention

Embodiments of the invention seek to provide a method for manufacturing a structure comprising a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, which enables a semi-conductor layer having the required properties for the intended application and which provides a good adhesion between the semi-conductor layer and the first substrate to be obtained, without using a temperature higher than 400 °C.

In an aspect of the invention, it is provided a method for manufacturing a structure comprising a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, characterised in that it comprises the following steps of:

(a) providing a first bonding metal layer on the first substrate, called an acceptor substrate,

(b) providing a second substrate, called a donor substrate, comprising successively:

- a semi-conductor base substrate,

- a stack of a plurality of semi-conductor epitaxial layers, a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$ being located at the surface of said stack opposite to the base substrate,

- a second bonding metal layer,

(c) bonding the first substrate and the second substrate through the first and second bonding metal layers, said bonding step being carried out at a temperature lower than or equal to 400 °C,

(d) removing a part of the second substrate so as to transfer the layer of $\text{Si}_x\text{Ge}_{1-x}$ on the first substrate, said removing comprising at least selectively chemically etching a layer of the second substrate relative to the $\text{Si}_x\text{Ge}_{1-x}$ layer.

Thus, the layer of $\text{Si}_x\text{Ge}_{1-x}$ has both an excellent crystal quality and a mobility of charge carriers which is higher than that of a relaxed single crystal silicon layer. Consequently, the structure formed is optimum for manufacturing tridimensional monolithic integrated circuits for high performance and/or low power applications.

On the other hand, metal-metal bonding provides strong bonding energy even at a temperature not exceeding 400 °C, this energy being substantially higher than that provided by a dielectric-dielectric bonding made at such a temperature. Further, the metal-metal interface has the advantage, unlike a dielectric-dielectric interface, not to be attacked by a hydrofluoric acid solution possibly employed for selectively etching at least one layer of the second substrate.

- epitaxially growing a layer of silicon-germanium with a constant composition over its thickness,

- polishing the layer of silicon-germanium with a constant composition,

- epitaxially growing a layer of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x on the polished layer of silicon-germanium, said layer of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer of silicon-germanium having a constant composition over its thickness,

- epitaxially growing the layer of $\text{Si}_x\text{Ge}_{1-x}$ on the layer of $\text{Si}_y\text{Ge}_{1-y}$,

- depositing the second bonding metal layer.

According to one embodiment, step (b) comprises, between the step of epitaxially growing the layer of $\text{Si}_x\text{Ge}_{1-x}$ and the step of depositing the second bonding metal layer, a step of depositing a dielectric layer.

Step (b) can comprise, after the step of depositing the dielectric layer, a densification annealing of said layer.

Particularly advantageously, step (b) further comprises forming, between the dielectric layer and the second bonding metal layer, a layer of a binary or ternary metal alloy.

According to one embodiment, step (d) comprises withdrawing a part of the thickness of the base substrate by polishing, followed by selectively etching the rest of said base substrate.

Particularly advantageously, etching the base substrate is made with a TMAH, KOH, and/or $\text{HF}:\text{HNO}_3$ solution.

On the other hand, removing the base substrate can be followed by selectively etching the layers of silicon-germanium with a constant composition and a gradual composition by means of a SC1 solution and/or a $\text{HF}:\text{H}_2\text{O}_2:\text{CH}_3\text{COOH}$ solution.

Another aspect relates to a method for manufacturing a tridimensional monolithic integrated circuit, comprising implementing the method described above.

More precisely, this method for manufacturing a tridimensional monolithic integrated circuit, comprises:

- manufacturing a structure comprising a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400°C and a layer of $\text{Si}_x\text{Ge}_{1-x}$ extending on said first substrate by means of the method described above,

- manufacturing at least one other electronic component in or on the layer of $\text{Si}_x\text{Ge}_{1-x}$.

Said method is remarkable in that all the steps implemented on said structure are made at a temperature lower than or equal to 400°C .

Another aspect relates to a structure likely to be obtained by the method described above.

Said structure comprises a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, and is characterised in that said semi-conductor layer is a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$ and in that said structure comprises, between said first substrate and said semi-conductor layer, a metal layer.

According to one embodiment, said structure further comprises a dielectric layer between the metal layer and the semi-conductor layer.

Advantageously, the structure comprises, between the metal layer and the dielectric layer, a layer of a binary or ternary metal alloy.

Said at least one electronic component can comprise a transistor, a memory, a photodetector, a diode, a laser, a switch, an amplifier and/or a filter.

Another aspect relates to a donor substrate intended to be used in the method described above.

This donor substrate successively comprises:

- a semi-conductor base substrate,
- a stack of a plurality of semi-conductor epitaxial layers, a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$, being located at the surface of said stack opposite to the base substrate,
- a bonding metal layer.

According to one embodiment, the donor substrate further comprises a dielectric layer between the layer of $\text{Si}_x\text{Ge}_{1-x}$ and the metal layer.

Said dielectric layer can have a thickness between 10 and 20 nm.

According to one embodiment, the base substrate is a silicon substrate.

According to one preferred embodiment, the stack successively comprises, from the base substrate:

- a layer of silicon-germanium having a composition gradually varying over its thickness,
- a layer of silicon-germanium having a constant composition over its thickness,
- a layer of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x , said layer of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer of silicon-germanium having a constant composition over its thickness so as to make up an etching barrier layer towards the layer of $\text{Si}_x\text{Ge}_{1-x}$,
- the layer of $\text{Si}_x\text{Ge}_{1-x}$.

Brief description of the drawings